ECE4211 HW12 MOS-II COMS Logic, CMOS and CCD Imaging, Nonvolatile Memory F. Jain (4/20/17) **No submission needed for part B**. Solutions attached.

Q.1 (a) Given the width to length ratio (W/L) for a driver transistor to be 20/5 and for the load transistor as 10/10 in an n-MOS inverter. Find the sizing of MOSFETs T1, T2, and T3 used for the NMOS logic gate shown in Fig. 1.

Justification: When there are more than one transistor is in series on the driver side (i.e. below the output), we increase the (W/L) ratio by the number of transistors in series. Two transistors T1 and T3 are in series with size = 2*20/5=40/5.Similarly, T2 and T3 are in series with same sizing.

Q. 1 **(b) Why do we make the W/L** ratio of p-FET 2.5 times larger than the n-FET in a CMOS inverter such as shown in Fig. 2?

The PMOS-FET (W/L) is made 2.5 times larger than (W/L) of NMOS. This is done to charge and discharge the load capacitor C_L (at the output of a CMOS gate). When input voltage goes from low to high, discharging of C_L (which was at VDD) takes place through NMOS FET. Similarly, charging happens through PMOS FET when the input changes from high-to-low.

$$\mu_n * C_{OX} * \left(\frac{W}{L}\right)_{n-MOS} = \mu_P * C_{OX} * \left(\frac{W}{L}\right)_{P-MOS}, \text{Since } \mu_n \cong \mu_p * 2.5, \left(\frac{W}{L}\right)_{n-MOS} = 2.5 * \left(\frac{W}{L}\right)_{P-MOS}$$

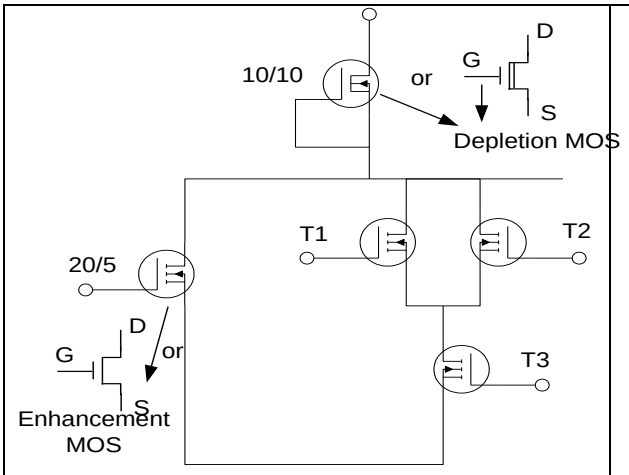


Fig 1. Schematic of an NMOS logic gate. p647

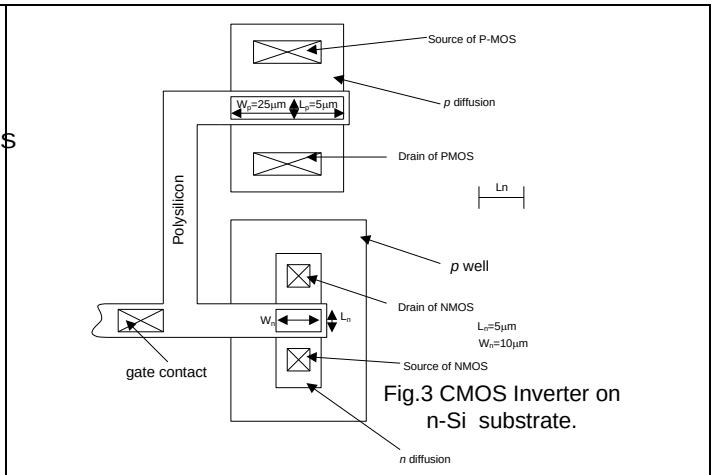


Fig. 2. CMOS inverter top view. **(page 668)**

1(c). Justify the W/L ratios shown for CMOS NOR and NAND gates in Fig.3.

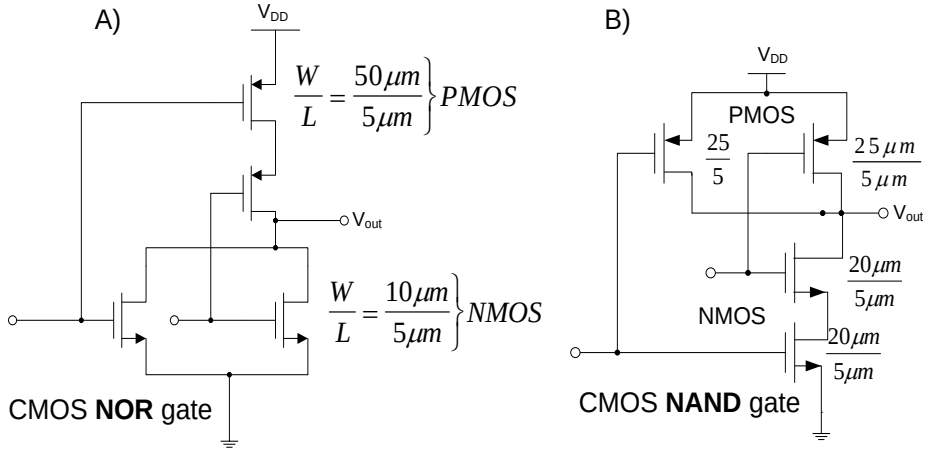


Fig. 3 W/L ratios for CMOS NOR and NAND gates.

NOR gate Fig.3(A). Here two P-MOS FETs are in series. When both are "ON", we need to reduce their total series resistance to equivalent of one transistor.The W/L ratio is multiplied by number of FETs in series.

$(W/L)_{\text{P-MOS when two in series}} = 2*(W/L)_{\text{P-MOS when single}} = 2*(25/5) = 50/5$

Fig.3 (B) is a NAND with two NMOS in series. $(W/L)_{\text{N-MOS when two in series}} = (10/5) * 2_{\#\text{ FET in series}} = 20/5$

Q.2.(a) Outline the steps used in scaling a FET from 1.3 micron to 0.25 micron is described in Baccarani et al (1984 paper distributed in class April 19, see Table I). **Pages 610-623**.

Solution; Design steps: 1. Find the dimensional scaling factor l which is L/L' or W/W' or Tox/Tox'.

2. Find the $\Delta V'_{TH}$ for the new scaled down FET including process variations, masking registration errors, doping changes. Find $V'_{TH}= 4\ \Delta V'_{TH.}$ Find $V'_{DD} = 4 * V'_{TH}$.

Calculate scaling factor for voltages and potentials: $k = V_{TH}/ V'_{TH}$

3. Find $\delta = \kappa/\lambda^2$

4. Compute new substrate doping $N'_A = N_A/ \delta = (\lambda^2/k)\ N_A$

Q2(b) Scale down a 0.25 micron FET to design the 0.025 micron (25nm) transistor following the 10-fold scaling. Given ΔV_{TH} = 0.015V for 25 nm process. Justify the values given in Table I. For 0.025micron FET, use V_{TH} = ¼ of VDD. Assume V_{DD} of 0.4 Volt. Obtain gate oxide thickness, Si doping levels, source and drain thicknesses and doping etc.

Table I Hint set for 25nm FET design

Source and drain resistances are function of junction depth x_j and source and drain length and width. Knowing the resistivity of the source and drain region, we can calculate the resistance of the source and drain regions.

Table I Hint set for 25nm FET design

Parameters	**LATV 1.3micron**	**0.25 micron QMDT* (IBM)**	**25nm SiGe (Home work)**	**Scaling factor**	**Comments**
Channel Length L(μm)	1.3	0.25	0.025	λ=10	
Gate Insulator Oxide t_{ox} (nm)	25	5.0 (SiO_2)	0.5 (SiO_2)	10	0.5($\varepsilon_{HfO2}/\varepsilon_{SiO2}$) = 1.7nm
Junction Depth x_j(nm)	350	70-140	7-14	10	Gives high Rs and Rd
V_{TH} (V) V_{TH} =4x ΔV_{TH}	0.6	0.25 V'_{TH} =4x $\Delta V'_{TH}$ $\Delta V'_{TH}$ =0.06	0.06 V'_{TH} =4x $\Delta V'_{TH}$ $\Delta V'_{TH}$ =0.015	κ=4	ΔV_{TH}=0.015V
$V_{DS} = V_{DD}$ (V) $V_{DD} = 4$ x V_{TH}	2.5	1.0	0.25	κ=4	
Band Bending (V)	1.8	0.8	0.3	?	
Doping N_A (cm^{-3})	$3x10^{15}$	$N'_A = 3\times10^{16}$	$N'_A = 7.5\times10^{17}$	N_A x λ^2/κ=25	
(Rs + Rd)ID IR Drop (mV)	NA	< 10mV	< 1mV	??	How to solve this
RC Delay τ (ps)	Not appl. (NA)	100ps	2-5 ps??	??	How to solve this

Scaled down FET **Original FET**

1. Dimensions

   L', W', T_{ox}' $\Longrightarrow$ $L/\lambda,\ W/\lambda,\ T_{ox}/\lambda$ $\lambda > 1$

2. Voltages

   V_{GS}', V_{DS}' ,V_{TH}' $\Longrightarrow$ $V_{GS}/k,\ V_{DS}/k,\ V_{TH}/k$ $k > 1$

3. Doping Levels

   N_A', N_D' $\Longrightarrow$ $N_A/\delta,\ N_D/\delta$ $\delta < 1$

Since $\delta = k/\lambda^2$ and (1/δ) = λ^2/k, substrate doping N_A' is higher. [Pages 579-580 Notes III]

Q6(b) Scale down a 0.25 micron FET to design the 0.025 micron (25nm) transistor following the 10-fold scaling. Given ΔV_{TH} = 0.015V for 25 nm process. Justify the values given in Table I.

For 0.025micron FET, use V_{TH} = ¼ of VDD. Assume V_{DD} of 0.4 Volt. Obtain gate oxide thickness, Si doping levels, source and drain thicknesses and doping. The design steps for 0.25μm from 1.3μm FET are shown below

1.3 μm channel length L FET	0.25 μm FET channel length L'	Scaling factor
L = 1.3 μm T_{ox} = 25 nm V_{DD} = 2.5 V V_{TH} = 0.6 V	L' = 0.25 μm T_{ox} ' = 5 nm V_{DD} ' = 1 V V_{TH} ' = 0.25 V	L'= $L/_{\lambda,}\ \lambda = {1.3}/{0.25} = 5$ V_{DD}'= $V_{DD}/_{k,}\ k = {2.5}/{1} = 2.5$
Substrate doping N_A Scaling factor δ	$N_A' = N_A \frac{\lambda^2}{k} = N_A / \delta$ $\delta = k / \lambda^2$	$N_A' = N_A \frac{25}{2.5} = N_A * 10$ $N'_A = 3\times10^{16}$ cm^{-3}

These parameters are given in Reference 1, Page 591. Now our task is to scale 0.25μm to 0.025μm FET

0.25 μm channel length L FET	0.025 μm channel length L' FET	Scaling factor
L = 0.25 μm T_{ox} = 5 nm V_{DD} = 1.0 V V_{TH} = 0.25 V $N_A = 3 * 10^{16}$ cm^{-3}.	L' = 0.025 μm $T_{ox}' = {5}/{10}$ =0.5 nm = 5Å V_{DD}' = 0.25V (given). $V_{DD}' = 4* V_{TH}'$ $V_{TH}' = 4\ \Delta V_{TH}'=4*0.015 = 0.06V$ k = V_{DD}/ V_{DD}'= 1.0/0.25 = 4 $N_A' = N_A/\delta$, $(1/\delta) = \lambda^2/k$= 100/4=25. N_A'= 3*10^{16} *25 = 7.5*10^{17} cm^{-3}.	L'= $L/_{\lambda,}\ \lambda = 0.25 / 0.025 = 10$ $V_{DD}'= V_{DD}/_{k,}\ k = {1.0}/{0.25} = 4$ k =4 $N_A' = 3 * 10^{16} * \frac{10^2}{4} = 7.5* 10^{17} cm^{-3}$

Certain issues following scaling: 1). Oxide thickness in 0.25 μm ≈ 50 - 60Å and T_{ox}' in 0.025 μm ≈ 5 A^o is too small and it will cause severe tunneling current. 2). Tunneling from source to drain when L' = 25nm and lower. 3). $I_D * (R_S + R_D)$ voltage drop is < 1 mV.

Q.2(c) Generalized scaling (GS, Table IV) is better than constant electric field (CE) scaling (Table–II) and constant voltage (CV) and Quasi constant voltage (QCV) in (Table-III) as it permits different scaling for voltages/ potential, dimensions (L,W,T_{ox}) and doping. GS is based on preserving Poisson's equation. GS gives relationship for N_A' and N_D' with N_A and N_D multiplied by 1/δ.

Constant electric (CE) field scaling: All dimensions, voltages are divided by k (or scaling factor). Doping levels are multiplied by k.

Quasi Constant Voltage (QCV) Scaling: All dimensions are divided by k (or scaling factor). Doping levels are multiplied by k. The voltages are divided by $(1/k)^{1/2}$ which is less than k.

Constant Voltage (CV) Scaling: All dimensions are divided by k (or scaling factor). Doping levels are multiplied by k. The voltages are not changed.

Most difficult scaling parameters are:

(i) Gate Insulator. Solution is to increase T_{ox}' = 5 A^o by using HfO_2 which has a higher dielectric constant $\varepsilon_{Hf\,O2} \approx 13.7$ and dielectric constant for SiO_2 is 3.9.

T_{ox}' for HfO_2 as gate insulator is $= \frac{\varepsilon\ HfO2}{\varepsilon\ SiO2} * T_{ox}'(SiO2)$,

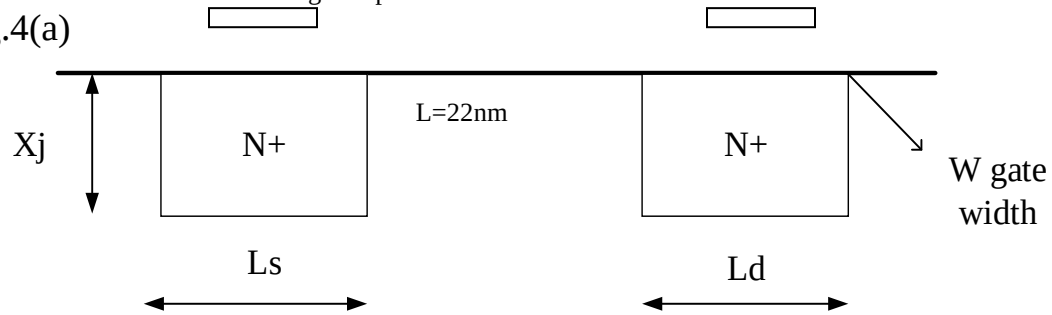
$$= \frac{13.7}{3.9} * 5\ A^o = 17.5\ A^o = 1.75 \text{ nm}$$

E_g for Hf O_2 = 5.7 eV and electron affinity $q\chi_{Hf\,O2}$ = (2.0 ± 0.25) eV

The other parameter is the voltage drop in $R_{S+}R_D$

(ii) Source and Drain resistances and voltage drops for a 25nm FET are calculated below.

Fig.4(a)



X_j for 0.25 µm FET (Baccarani et al Table II) Ls= 22nm (contact) +11nm +11nm=44nm

= 0.07 – 0.14 µm $R_S = R_D = \rho_{n*}\frac{Ls}{X_j * W}$

X_j' for 0.025 µm NanoFET For 10^{20} n+ doping the resistivity ρ_s is

$= \frac{0.07}{10} \rightarrow \frac{0.14\ \mu m}{10}$ $\rho_s = 7 * 10^{-4}$Ω-cm. Given W=44nm,

= 0.007 µm →0.014 µm $R_S = R_D = \frac{7 * 10^{-4} * 44\ nm}{0.007 * 10^{-4} * 44\ nm}$

= 7 nm → 14 nm = 1.0 kΩ

If the drain current is $I_D \approx$ 1mA or 0.1 mA. Taking 0.1mA or 100 microamp, we get $I_D * (R_{S+}R_D) \approx$ 0. 2V =200mV, which is too high.

How can we reduce R_S and R_D ?

Method # 1 Increase the thickness Xj of source or source contact T_{source} above the implanted 14 nm region.

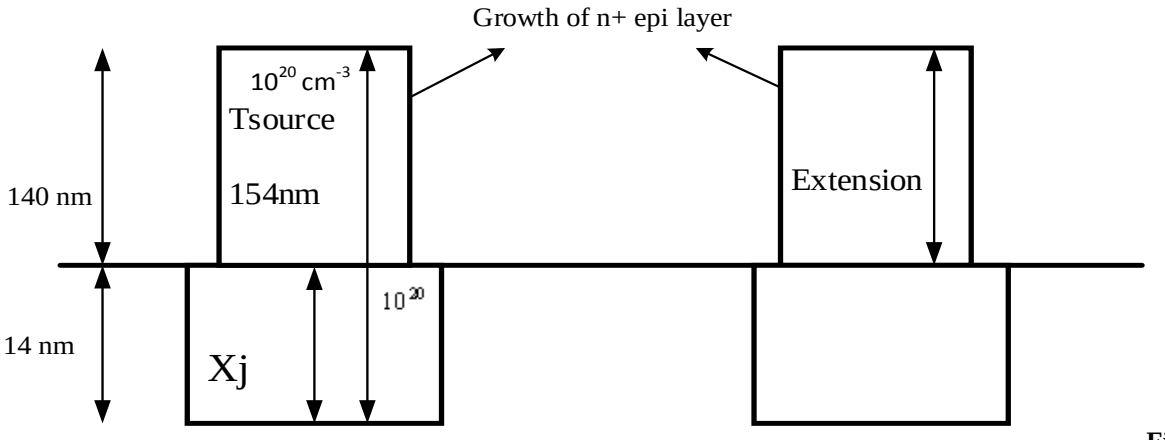


Fig.4b

New source resistance $R_S' = R_s * [X_j/(X_j + T_{source}] = \frac{7 * 10^{-7}}{154 * 10^{-7}} * 1.0\ k\Omega = 45.45\Omega$

The new IR_s' drop is I *R_S' = 100 µA * 45.45Ω = 4.5mV. This value is still higher than 1mV.

Method 2: (a) Increase W of the channel, and (b) further increase thickness of source T_{Source}. Both are not desirable as they increase the area of FET (option a) and make processing difficult when using masks or metal contacts (option b).

Method 3. Use metal silicides for vertical extensions in place of n+ Si which have reduced resistivity.

What is done is to replace T_{source} contact with lower resistivity silicides or TiN or TaN. R_S (with silicides) is reduced by a factor of 10. The new drop is 0.45mV. Reduce R_S from 45.4Ω to approximately 4.5 Ω.

Q3(a) Show that the threshold voltage for N-MOS (n+ poly Si gate, doping $N_D = 1x10^{20} cm^{-3}$) is $V_{TN} = +1.0$ V and for P-MOS (with p+ poly Si gate, doping $N_A = 1x10^{20}\ cm^{-3}$) is $V_{TP} = -1.0$ V.

Notes pages 658-670: Given $Q_{ox} = 1.6x10^{-8}$ Coulombs/cm^2 $\varepsilon_{s,r} = 11.8$

d (Oxide thickness) = 500 Å = $0.05x10^{-4}$cm $\quad$ $n_i = 1.5\times10^{10}\ cm^{-3}$

$\varepsilon_{ox} = 3.9$, T = 300°K $\quad$ $N_A = 3.84x10^{16}\ cm^{-3}$ (Substrate)

$\varepsilon_0 = 8.854\times10^{-14}$ F/cm $\quad$ N-Well doping $N_D = 2x10^{16}\ cm^{-3}$

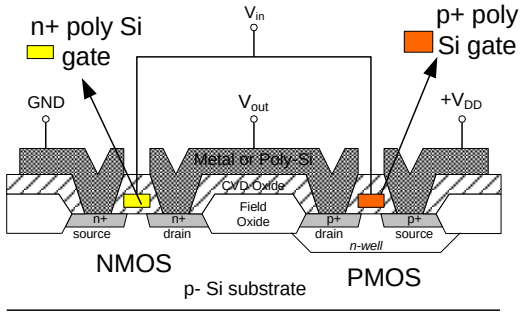


Fig. 5a.Cross Section of CMOS inverter structure.

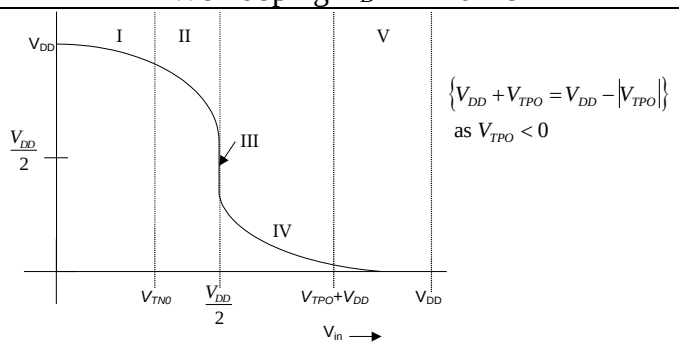


Fig. 5(b). VTC of a CMOS inverter

Solution Q3(a): Threshold Voltage $V_{TH\ NMOS} = V_{TN}$ for NMOS FET with n^+ poly Si (gate)-SiO_2-pSi

$N_{D\ for\ n+\ poly\ Si\ (gate)} = 1*10^{20}\ cm^{-3}$, $N_{A\ for\ pSi} = 3.84*10^{16}\ cm^{-3}$, SiO_2 thickness is 500Å $= 0.05*10^{-4}$ cm

$V_{TN} = V_{TH|NMOS} = ?$

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}}$$

$$\phi_{ms} = \phi_{n\text{-}PolySi} - \phi_{pSi} = (4.15 + 0.55 - \frac{kT}{q} * \ln\frac{N_D}{n_i}) - (4.15 + 0.55 + \frac{kT}{q} * \ln\frac{N_A}{n_i})$$

$$= -\frac{kT}{q}(\ln\frac{10^{20}}{1.5*10^{10}} + \ln\frac{3.84*10^{16}}{1.5*10^{10}}) = -0.968V$$

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}} = -0.968 - \frac{1.6*10^{-8}}{6.906*10^{-8}} = -0.968 - 0.2316 = -1.1996V$$

$$V_{TH} = V_{TP} = V_{FB} - \frac{Q_{sc}}{C_{OX}} + 2\psi_B = -1.1996 + \frac{(1.6*10^{-19}*3.84*10^{16}*1.61*10^{-5})}{6.906*10^{-8}} + 0.764$$

$$= -1.1916 + 1.432 + 0.764 = 0.9964V \approx 1V$$

where, $C_{OX} = 6.906*10^{-8}$ F/cm^2

$$Q_{OX} = 1.6*10^{-8} C/cm^2,\ \psi_B = \frac{kT}{q} * \ln\frac{N_A}{n_i} = 0.0259 * \ln\frac{3.84*10^{16}}{1.5*10^{10}} = 0.382\text{V}$$

$$2*\psi_B = 0.382*2 = 0.764$$

$$Q_{sc} = +q*N_A*W_m = 1.6*10^{-19}*3.84*10^{16}*W_m$$

$$W_m = \sqrt{\frac{2*\varepsilon_r*\varepsilon_o*2\psi_B}{q*N_A}} = \sqrt{\frac{2*11.8*8.854*10^{-14}*|2*0.382|}{1.6*10^{-19}*3.84*10^{16}}} = 1.61*10^{-5} cm$$

Threshold Voltage $V_{TH\ PMOS} = V_{TN}$ for PMOS (on n-well) with p^+ poly Si (gate)-SiO_2-nSi

$N_{A\ for\ p+\ poly\ Si\ (gate)} = 1*10^{20}\ cm^{-3}$, $N_{D\ for\ nSi} = 2*10^{16}\ cm^{-3}$ (n-well doping), SiO_2 thickness is 500Å$=500*10^{-8}$ cm.

Show $V_{TP} = -1.0$ V <= Threshold voltage for P-MOS

$$V_{TP} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}} - \frac{Q_{SC}}{C_{OX}} + 2\psi_B$$

$$\phi_{ms} = \phi_{P\text{-}PolySi} - \phi_{nSi} = (4.15 + 0.55 + \frac{kT}{q} * \ln\frac{N_A}{n_i}) - (4.15 + 0.55 - \frac{kT}{q} * \ln\frac{N_D}{n_i}) = \frac{kT}{q}(\ln\frac{10^{20}}{1.5*10^{10}} + \ln\frac{2*10^{16}}{1.5*10^{10}})$$

$$= 0.5857 + 0.36527 = 0.951V$$

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}} = 0.951 - \frac{1.6*10^{-8}}{6.906*10^{-8}} = 0.951 - 0.2316 = 0.7194V$$

$$V_{TH} = V_{TP} = V_{FB} - \frac{Q_{sc}}{C_{OX}} + 2\psi_B$$

$$= 0.7194 - \frac{\sqrt{2*11.8*8.854*10^{-14}*|2*0.36527|*3.2*10^{-3}}}{Cox} - 2*0.36527$$

$$V_{TP} = 0.7194 - 1.012 - 2*0.36527 = -1.022V$$

We have used the following parameters:

$$C_{OX} = \frac{\varepsilon_r * \varepsilon_{oB}}{d} = \frac{3.9*8.854*10^{-14}}{500*10^{-8}} = 6.906*10^{-8}\,F/cm^2$$

$$\psi_B = -\frac{kT}{q} * \ln\frac{N_D}{n_i} = -0.0259 * \ln\frac{2*10^{16}}{1.5*10^{10}} = -0.36527V$$

$$Q_{sc} = +q * N_D * W_m = q * N_D * \sqrt{\frac{2*\varepsilon_r*\varepsilon_o*|2\psi_B|}{q*N_D}} = \sqrt{2*q*N_A*\varepsilon_r*\varepsilon_o*|2\psi_B|}$$

$$= \sqrt{2*11.8*8.854*10^{-14}*|2*0.36527|*3.2*10^{-3}} == 6.989*10^{-8}C$$

$$\frac{Q_{sc}}{C_{OX}} = \frac{6.989\times10^{-8}}{6.906\times10^{-8}} = 1.012V$$

Q3(b) Explain the five regimes observed in the voltage transfer characteristics of a CMOS inverter (Fig. 5b).

Solution: Q3 (b) Various regions are outlined below. Region I : $V_{IN} < V_{TNo}$, That is NMOS is OFF and PMOS is in saturation. VTNo means no substrate bias. Hence in our case $V_{TN} = V_{TNo}$

Region II : $V_{IN} > V_{TNo}$ and $V_{IN} < \frac{V_{DD}}{2}$ NMOS is ON and in linear.

In this region PMOS remains in saturation region.

Region III: Both in saturation.

Region IV: PMOS is in linear and NMOS remains in saturation region.

Region V: PMOS is OFF and NMOS is in saturation.

Q3(c). Find the CMOS inverter threshold V_{INV} if the NMOS size (W/L) is 5/5 and electron mobility μ_n= 600 cm^2/V-s and PMOS size is (12.5/5) and hole mobility in p-MOS is μ_n= 240 cm^2/V-s. HINT: page 664 Eq. 19 for inverter threshold expression.

$$V_{inv} = \left\{ V_{TN0} + \frac{V_{DD} + V_{TP0} - V_{TN0}}{\left[1 + \sqrt{\frac{K_N' S_N}{K_P' S_P}}\right]} \right\}, \qquad (13)$$

Provided that:
$V_{TN0} = -V_{TP0}$ &
$K_N' S_N = K_P' S_P$
Then:
$V_{inv} = \frac{1}{2} V_{DD}$

$$K_N' = \frac{\mu_n C_{ox}}{2}$$

$$S_N = \left(\frac{W}{L}\right)_{NMOS}$$

Solution: Q3(c) Inverter threshold V_{INV}

Mobility values used $\mu_n = 600\text{cm}^2/\text{V.sec}$, $\mu_P = 240\text{cm}^2/\text{V.sec}$

$$V_{INV} = V_{TNo} + \frac{V_{DD} + V_{TPO} - V_{TNo}}{1 + \sqrt{\frac{K_N' * S_N}{K_P' * S_P}}}$$

$$V_{INV} = 1 + \frac{5 + (-1) - 1}{1 + \sqrt{1.2}} = 1 + \frac{3}{1 + 1.09} = 1 + \frac{3}{2.09} = 2.44V$$

$$K_N' = \frac{\mu_n * C_{ox}}{2} \; and \; K_p' = \frac{\mu_P * C_{ox}}{2}, \; and \; S_N = \left(\frac{W}{L}\right)_N, \; S_P = \left(\frac{W}{L}\right)_P$$

$$\frac{K_N' S_N}{K_P' S_P} = \frac{\mu_n * C_{ox} * \left(\frac{W}{L}\right)_N}{\mu_P * C_{ox} * \left(\frac{W}{L}\right)_P} = \frac{600 * 5/5}{240 * 12.5/5} = \frac{60 * 1}{20 * 2.5} = \frac{3}{2.5} = 1.2$$

Q3(d). Outline a method to calculate the propagation delay τ_p of the CMOS inverter shown in Fig. 5. Assume that it feeds a similar gate as a load. Find the equivalent load capacitance C_L and values of R_{PU} [$=4/\beta_p V_{DD}$] and R_{PD} [$=4/\beta_n V_{DD}$]. HINT: **pages 672--679.**

Solutions: Q3 (d) Outline a method to calculate the propagation delay τ_p of the CMOS inverter shown in Fig. 5. Assume that it feeds a similar gate as a load. Find the equivalent load capacitance C_L and values of R_{PU} [$=4/\beta_p V_{DD}$] and R_{PD} [$=4/\beta_n V_{DD}$]. HINT: **pages 672--676.**

Propagation delay $\tau_p = \tau_r + \tau_f$, for τ_p, we need to find C_{total} (which is also C_L) and resistance of $R_{PU} + R_{PD}$.

C_L is charged via P-MOS $\tau_r = \frac{4 * C_L}{\beta_P * V_{DD}}$, $\beta_P = \mu_P * C_{ox} * \left(\frac{W}{L}\right)_p$ CHARGING

C_L is discharged via N-MOS $\tau_f = \frac{4 * C_L}{\beta_n * V_{DD}}$, $\beta_n = \mu_P * C_{ox} * \left(\frac{W}{L}\right)_N$ DISCHARGING

C_L is total load capacitance or C_{total}. For C_L computation, see pp. 646-654.

$t_{inverter-pair} = t_f + t_r \approx 4\frac{C_L}{\beta_n V_{DD}} + 4\frac{C_L}{\beta_p V_{DD}}$ (page 676), It can be written as

$$t_{inverter-pair} = t_f + t_r \gg 2RC_L \left[\text{if } \beta_n = \beta_p \text{ and } R = \frac{4}{\beta_n V_{DD}} = \frac{4}{\beta_p V_{DD}} \right]$$

$$C_L = C_{eq}\big|_{NMOS} + 2 \text{ or } 2.5 \; C_{eq}\big|_{PMOS}.$$

For NMOS Example#4

C_{DB1} : $C_{BD1} = C_{DB,intrinsic} + C_{DB,junction}$; $C_{GD1} = C_{GD,intrinsic} + C_{GDO}$ (Overlap Capacitance)

C_{BS21} : $C_{SB2} = C_{SB,intrinsic} + C_{SB,junction}$; $C_{GD2} = C_{GD,intrinsic} + C_{GDO}$ (Overlap → Extrinsic)

C_L = Interconnect Capacitance; $C_{Total} = C_{DB1} + C_{GD1} + C_{SB2} + C_{GD2} + C_L + C_{G3}$

For CMOS see Example#6**:**

Q4. (a) Describe anyone of 'write', 'read' or 'erase' operation for a floating gate nonvolatile memory **(pp. 725-730) using the structure shown in Fig. 6 below.**

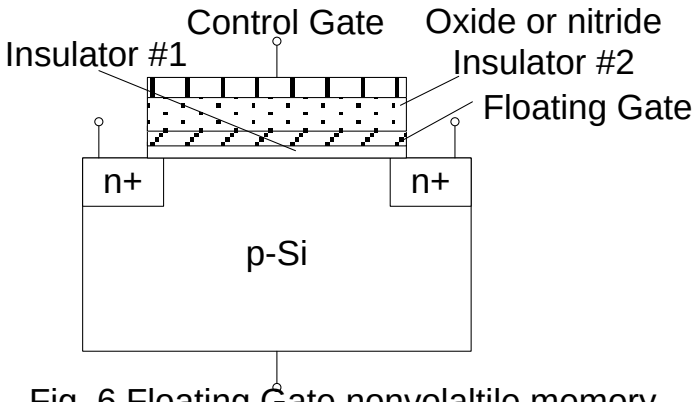


Fig. 6 Floating Gate nonvolaltile memory

Solution Q.4 (a) The Write is done by applying a gate pulse of certain duration. This enables transfer of electrons from the inversion layer to the floating gate. This results in threshold shift. Table II summarizes various operations.

Table II summarizes various voltages during Program/Write, Read and Erase operations.

Table II. Voltages during Program/Write, Read and Erase operations.

Operation	Source voltage V_S	Drain Voltage V_D	Control Gate Voltage V_G
Read	0	1V	~5V
Program	0	5	12V (Vpp)
Erase (source)	12V	Floating	0V
Erase (negative gate)	4V	Floating	-8V

Optional: Note all memory elements are in parallel. The addressing is done by row/ column pixel

Q4(b) An n-channel FET is configured as a floating gate nonvolatile memory.

If the transferred electron charge from the channel to floating gate is $Q_{floating}$ =2x10^{-8} C/cm^2, find the change in threshold voltage following this "write" operation. Assume that this charge is equivalent to 50% of the electron charge at the SiO_2-Si interface.

Al-SiO_2-pSi MOSFET having a threshold voltage V_{TH} = 0.533 V.

Channel length L = 10 μm, channel width Z = 50 μm, temperature T = 300K, and channel mobility μ_n = 650cm^2/V·sec. The intrinsic Fermi level is $E_i \sim E_g/2$. Q_{ox} = 2.103 x 10^{-8} C/cm^2.

Oxide thickness = d = 1000 Å (1 Å = 10^{-8} cm), n_i = 1.5x10^{10} cm^{-3} $q\chi_{SiO2}$ = electron affinity = 0.9 eV, $q\chi_{Si}$ = 4.15 eV, $q\chi_{Al}$ = 4.1 eV, N_A = 10^{16} cm^{-3} ε_{ox} = 3.9, ε_{Si} = 11.8 , ε_o = 8.854x10^{-14} F/cm.

Solution: 4(b) ***Question is:*** **If the transferred electron charge from the channel to floating gate is $Q_{floating}$ =2x10^{-8} C/cm^2, find the change in threshold voltage following this "write" operation**. Assume that this charge is equivalent to 50% of the electron charge at the SiO_2-Si interface.

The MOS transistor is an Al-SiO_2-pSi FET

$$\phi_{ms} = 0.6 - \frac{kT}{q}\ln\frac{N_A}{n_i} = -0.6 - 0.0259 * \ln[\frac{10^{16}}{1.5*10^{10}}] = -0.947\,V$$

$$where\ N_A = 10^{16}cm^{-3}\ \&\ n_i = 1.5*10^{10}cm^{-3}$$

$$V_{FB} = \phi_{ms} - \frac{Q_{OX}}{C_{OX}} = -0.947 - \frac{2.103*10^{-8}}{3.45*10^{-8}} = -1.557V$$

$$where\ C_{OX} = \frac{3.9*8.854*10^{-14}}{1000*10^{-8}} = 3.45*10^{-8}\ F/cm^2,\ d = 1000A^{O}$$

$$V_{TH} = V_T = V_{FB} - \frac{Q_{sc}}{C_{OX}} + 2\psi_B = -1.557 - \frac{(-q*N_A*W_m)}{3.45*10^{-8}} + 2\psi_B$$

$$= -1.557 + \frac{1.6\times10^{-19}\times10^{16}\times3.01\times10^{-5}}{3.45*10^{-8}} + 2*0.347 = -1.557 + 1.3959 + 0.694 = 0.5329 = 0.533\,V$$

$$where\ \psi_B = 0.347V,\ W_m = \sqrt{\frac{2*\varepsilon_r*\varepsilon_o*2\psi_B}{q*N_A}} = 3.01*10^{-5}\,cm$$

The 'write' operation deposits electrons in the floating gate

Q_{OX} is modified to $Q_{OX}' = Q_{OX} - 0.5*2*10^{-8} = 2.103*10^{-8} - 1*10^{-8} = 1.103*10^{-8}\ C/cm^2$

The new flat band voltage after "Write" $V_{FB}' = \phi_{ms} - \frac{Q_{OX}'}{C_{OX}} = -0.947 - \frac{1.103*10^{-8}}{3.45*10^{-8}} = -1.267\,V$

$$V_{TH}' = V_T = V_{FB}' - \frac{Q_{sc}}{C_{OX}} + 2\psi_B = -1.267 - \frac{(-q*N_A*W_m)}{3.45*10^{-8}} + 2\psi_B$$

$$= -1.267 + \frac{1.6*10^{16}*3.01*10^{-5}}{3.45*10^{-8}} + 2*0.377 = 0.822\,V$$

The threshold voltage shift is ΔV_{TH} = 0.822- 0.533 = 0.289 V.

In general threshold shift $\Delta V_{TH} = Q_{FG}/C_{floating\ gate\ and\ control\ gate}$.

$C_{floating\ gate\ and\ control\ gate} = C_{FC} = \varepsilon_{CG}*\varepsilon_o/t_{CG}$ where t_{CG} is the thickness of insulator #2 and ε_{CG} is the dielectric constant.

Q.5 Describe the operation of CMOS imaging pixels shown in Figs. 7 and 8.(**see pp. 745-746**)

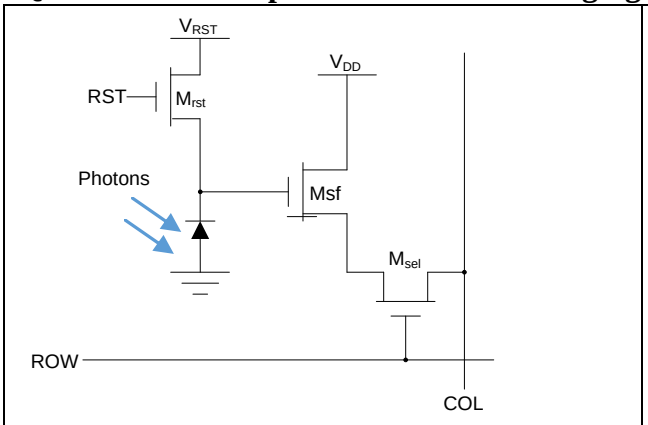


Fig. 7 Photodiode based active pixel.

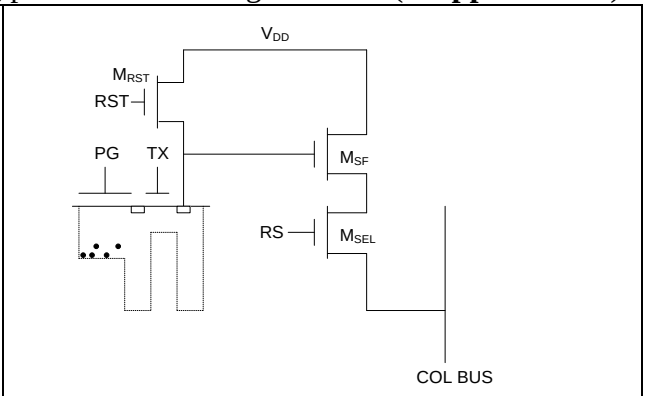


Fig. 8 Photogate based active pixel.

A photodiode based active pixel is shown in Fig.7, and photogate type active pixel is shown in Fig. 8. Fig. 7 shows photodiode based active pixel. The controller via RST signal resets the photodiode potential to V_{RST}. Photons (above band gap of Si) are absorbed by creating electron-hole pairs, reducing the potential across the photodiode. The pixel is read out by row/column select when FET M_{sel} is accessed by Row Select. Here, FET M_{SF} (Source-Follower) buffers the photodiode.

Fig. 8. **Active Pixel:** (p.740): Fig. 4 shows a photogate based active pixel. This scheme integrates x-y readout and CCD type MOS Photogate (PG). The charge generated by photons under the photogate is transferred when FET labeled as TX is enabled by row select RS, and connects it to a column bus. Photogate and TX share a bridging diffusion providing electrical connectivity. The

other end of FET TX is connected to FET M_{RST} which resets the voltage at the drain end of TX FET. There are 5 transistors per pixel. Photogate based active uses poly Si gate to permit photons to be absorbed in Si substrate (for PG FET).

Q6. (a) Forming an inversion channel in a MOS capacitor takes time. If we apply the gate voltage, greater than the threshold voltage, it will take τ_s seconds to form the inversion channel. This time is called the storage time, and is expressed as $\tau_s = AQ_n/I_{db}$ -- Eq. (1). Here, A is the gate area (ZL or WL), and I_{db} is the minority current. **Circle one**

TRUE X FALSE

(b) Find the dark current in the MOS device if Q.2(b) and use this value to fond storage time $\tau_{s,}$.
HINT: See Example 1, page 754. Notes Example 1 uses Al-SiO_2-nSi capacitors.
Dark current $I_{db}= qD_n*n_{po}*A/L_n$, $n_{po}=n_i^2/N_A=2.25*10^4$ cm^{-3} as $N_A=10^{16}$, $D_n=16.8cm^2/s$ (part 4c), L_n is not given, assume it 100 μm (like L_p on page 755 Example 1), $A=1cm^2$. $I_{db}=6.048*10^{-10}A$.

(c) Find the transfer time $\tau_{t,}$ between MOS (Al-SiO_2-pSi) capacitors with separation of 2 microns. Given $\tau_t = [(\text{Gate separation})^2]/2D_n$. $D_n = 16.8$ cm^2/s.

Answer: $\tau_t = [(\text{Gate separation})^2]/2D_n= [(2x10^{-4})^2]/2*16.8=1.19x10^{-9}s$

Q7(a) Fig. 9 shows a NAND architecture of a floating gate memory. Identify the driver transistor, load transistor and floating gate memory elements.

Solution: Figure shows these transistors.

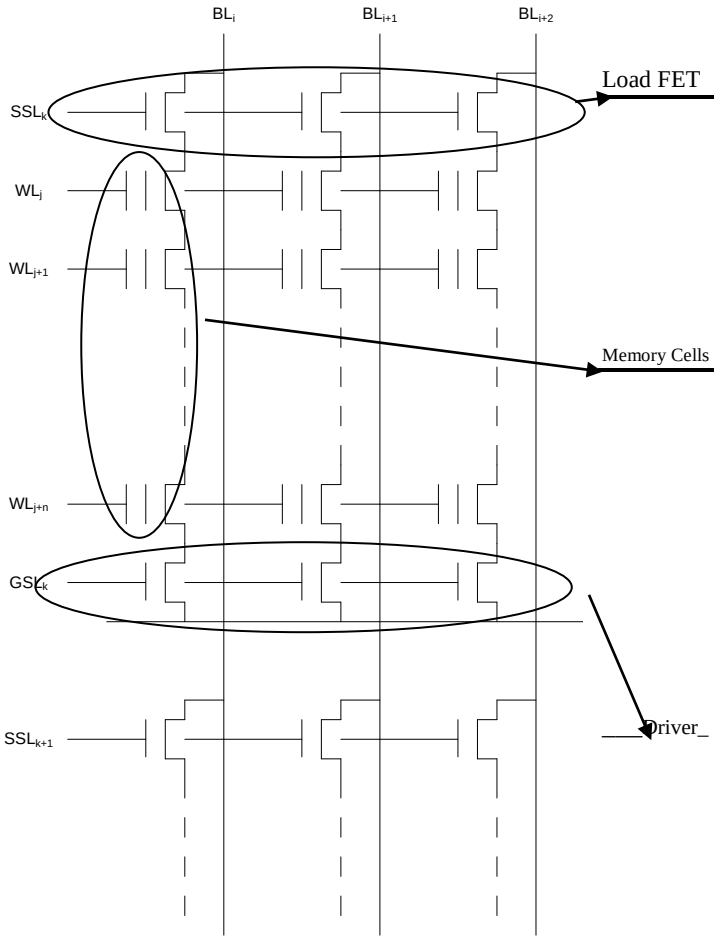


Fig. 9. Floating gate nonvolatile memory NAND architecture. Notes Fig. 11d, page 734.

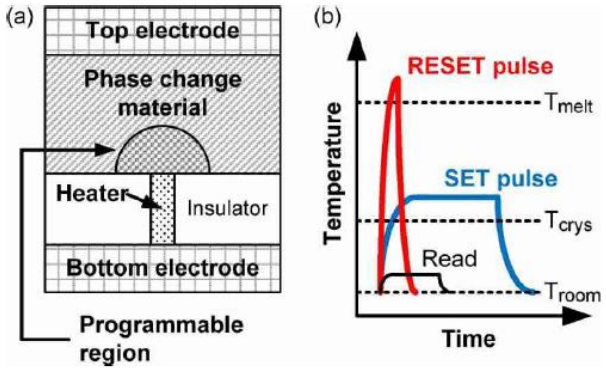


Fig. 10 (Notes Appendix C Figs. 1 and 2, p. 761)

Q7(B) Fig. 10 shows the schematic of a phase change memory cell and its characteristics. Outline its operation.