**UCONN ECE 4211 Solution SET 11MOS-I 04212017 F.Jain**

Q.1. (a) Find the work functions for n and p-type Si for the doping levels given below. Show them in relation to vacuum energy level being zero as the reference.

The electron affinity of Si is qχSi = 4.15 eV.

**p-side**: Acceptor concentration NA=1016 cm-3, τn=10-5 sec. Dn=40 cm2/sec.

Effective mass: electrons me=mn=0.26mo, holes mh=mp= 0.64 mo,

Junction area A=10-3 cm-2, ni (300K) =1.5×1010 cm-3. εr(Si)=11.8, ε0=8.85×10-14 F/cm, εs=εrε0. Assume all donors and acceptors are ionized at T=300 K. Eg = 1.1eV,

Boltzmann Constant k= 8.65x10-5 eV/K.

**n+-side**: Donor concentration ND=1018 cm-3, minority hole lifetime τp=2×10-6 sec.

 Minority hole diffusion coefficient Dp=12.5 cm2/sec.

(b) Compute the work function difference nSi-pSi (=nSi - pSi) and show that it is equal to the built-in voltage.

**Solution Q1(a)** Work function for n-Si is expressed as





**Ef - Ei is obtained from the definition of intrinsic Fermi level Ei:**

, if we take natural log (ln) we get





Work function of p-Si: Doping NA=1016cm-3

Intrinsicconcentration





Taking log (ln) we get, 



Note Ei - Efp = q



Q1(b) Work function difference between p-Si and n-Si is





Vbi is same as we calculated from the well-known Vbi expression for p-n junctions. =0.8139 V

Q.2(a). The threshold voltage is altered by: Circle correct answers

Gate metal charge in the gate oxide source doping substrate doping

(b) For a given metal-oxide-pSi MOS capacitor, which one will have higher threshold? Circle

Al-SiO2-psi or Au-SiO2-pSi

(c) What is the advantage in replacing gate metal by doped poly Si layer as the gate layer?

 Adjustment of threshold voltage,

 Enabling deposition of oxide for gate isolation in integrated circuits.

However, in 22nm and sub14nm FETs, TiN and TaN gate metals are used.

(d) Why in 22 nm FETs poly Si is not used and TaN or TiN metals are used?

 Because of lower threshold (VTH = 0.05V or lower) so that VDD ~0.2- 0.5V.

**Q.3 (a)** Compute the drain current ID for VD = 0.5, 1.0, and 2.5 volts in a n-channel

MOSFET having a threshold voltage VTH = 0.533 V at a gate voltage VG = 2 and 4V. Given: Channel length L = 10 μm, channel width Z = 40 μm,

operating temperature T = 300K, and channel mobility μn = 800 cm2/Volt⋅sec.

 Qox = 2.103 x 10-8 C/cm2 εSi = 11.8

Oxide thickness = d = 1000 Å (1 Å = 10-8 cm) ni = 1.5x1010 cm-3

qχSiO2 = electron affinity = 0.9 eV NA = 5x1016 cm-3

εox = 3.9 qχSi = 4.15 eV

# εo = 8.854x10-14 F/cm qAl = 4.1 eV

 The intrinsic Fermi level Ef= Ei ~Eg/2.

**Scenario I:** In this example, VTH =0.533V is incorrect for a p-Si doping of 5x1016cm-3. So will calculate VTH first which turns out to be 2.4838V. Then, we need to find the saturation voltage VD (set)) ≈ VG-VTH using Case I Approximation for gate voltage of VG=2V and VG=4V. **Scenario II:** We will use VTH =0.533V and compute drain current and gm and gD values.

**Scenario I**







, . The details to compute Wm are shown below. 





**Finding drain current under various VD and VG values.**





VG of 2V is below threshold VTH=2.4838V as a result drain current ID=0. We are neglecting sub-threshold conduction.

However, VG=4V is above VTH=2.4838V, and VD(sat) = VG – VTH = 4.0 - 2.4838=1.5162V.

For VG=4V and VD(sat)=1.5162, at VD = 0.5 we get ID using linear regime equation.



== 0.6989×10-4 A

For VG=4V and VD(sat)=1.5162, at VD = 2.5 we get ID using saturation regime equation.



ID = 1.104\*10-4[(1.5162)2/2] = 1.2689×10-4 A

**Summary Table ID-VD at VTH=2.4838 V**

|  |  |  |
| --- | --- | --- |
| ID | VG | VD |
| 0 subtrheshold | 2V < VTH (VTH = 2.4838 V) | 0.5V |
| 0 subtrheshold | 2V < 2.4838 V | 2.5V |
| 0.6989x10-4A | 4V | 0.5V |
| 1.2689x10-4A | 4V | 2.5V |

**Q.3(b)** Find saturation current and voltage VD(sat) at the VG = 4V. **Answered in part (a).**

For VG=4V and VD(sat)=1.5162, ID(sat)= 1.2689x10-4A

**Q.3(c)** Calculate the channel conductance gD and the transconductance gm at the following drain voltages VD = 0.5 V and VD = 2.5 V.

 gm at VD=0.5 V, VD=2.5 V, VG=4.0 V (likes part b)

Find gd at VD=0.5 V, VD=2.5 V VG=4.0 V

gm for VG =4.0 V:

VD(sat) = VG –VTH = 4.0 – 2.4838 = 1.5162 V.

So, VD=0.5 V will give unsaturated linear regime value.







Drain conductance; 

For VG=4.0, VD(sat)=1.5162 V. So VD=0.5 V, is below saturation (in linear regime).



For VD=2.5V, we are in saturation as VD(sat) =1.5162V.
**Q.3(d)** If the gate is n+ poly Si (ND = 1x1019cm-3), calculate the flat band and threshold voltage assuming the same Qox as in part (a).

Gate is n+ poly Si, ND=1019 cm-3



Note: In Part Q3(a), VFB = -1.5985 V, and in part Q1(d) VFB =-1.5242 V



The parameters used are from Q3(a).



Q3(e) Calculate the transconductance gm in the linear regime. From Q3(c) we have

 = 0.552\*10-4 Mho.

It depends on VD.

Q3(f) What is the cut off frequency fT (= gm/(2 Cg)) of this FET? Cg is the gate capacitance which varies between Cox and Cox/3 depending on the depletion width variations. It also depends on the drain and source to body capacitance.

Using gm =2.76\*10-4 from part Q3(c) at VD = 2.5V, and Cg = Cox/3 = 3.45\*10-8/3=1.15\*10-8 F/cm2. Here we have used the capacitance of unit area (L\*Z = 1 cm2).

fT =1.6738\*10-4/(2 \*1.15\*10-8) = 2316.49 Hz for a 1cm2 gate area FET.

For FET with dimensions L=10 m and Z=40 m,

fT = 2316.49/(10m \* 40m) =5.78\*108 Hz.

 **Scenario II:** Q3(a) We will use VTH =0.533V (it is true when NA = 1\*1016 cm-3) and compute drain current and gm and gD values.

**Q.3 (a)** Compute the drain current for VD=0.5V and VD=2.5V at VG=2V and 4V.

First, we need to find the saturation voltage VD (set) for VG=2V and for VG=4V.




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We use the linear regime ID equation for VD < VD(sat)



 **ID-VD Summary Table when VTH=0.533 V**

|  |  |  |
| --- | --- | --- |
| ID | VG | VD |
| 6.718x10-5A | 2V | 0.5V |
| 1.187x10-4A | 2V | 2.5V |
| 1.775x10-4A | 4V | 0.5V |
| 6.118x10-4A | 4V | 2.5V |