Work function definition

<table>
<thead>
<tr>
<th>Metal</th>
<th>Work function $q\phi_m$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>4.1</td>
</tr>
<tr>
<td>Au</td>
<td>5.0</td>
</tr>
<tr>
<td>Mg</td>
<td>3.35</td>
</tr>
<tr>
<td>Ni</td>
<td>4.55</td>
</tr>
<tr>
<td>TiN</td>
<td></td>
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<tr>
<td>TaN</td>
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</tr>
</tbody>
</table>

Intrinsic Fermi level, $E_i$

Vacuum Level

$Q_{\text{Si}}=4.15$ eV

Conduction band

Valence band

$p$-Si

$n$-Si

Fig. 1 p 556
The semiconductor work function $q\phi_s$ is energy difference between the vacuum/reference level and the Fermi level.

$$q\phi_s = q\chi_{si} + (E_c - E_f)$$  \hspace{1cm} (3)

$$q\phi_s = q\chi_{si} + (E_c - E_i) + (E_i - E_f) = q\chi_{Si} + \frac{E_g}{2} + q\psi_B$$  \hspace{1cm} (4)

$$E_i - E_f = q\psi_B$$  \hspace{1cm} (5)

We can write an expression for the work function difference between metal and p-Si which is $q\phi_{ms}$.

$$q\phi_{ms} = q\phi_m - q\phi_s = q\phi_m - [q\chi_{si} + \frac{E_g}{2} - kT\ln\frac{N_D}{n_i}]$$
Work function difference for Al-SiO$_2$-nSi system

\[ q \chi_{Si} = 4.15 \text{ eV} \]
\[ q \chi_{SiO_2} = 0.9 \text{ eV} \]
\[ \frac{E_g}{2} = 0.55 \text{ eV} \]
\[ q \phi_m = 4.1 \text{ eV for Aluminum} \]

\[ q \phi_{ms} = 4.1 - [4.15 + 0.55 - kT \ln \frac{N_D}{n_i}] = -0.6 + kT \ln \frac{N_D}{n_i} \]

The work function difference increases as $N_D$ is increased.
The magnitude of work function difference increases as $N_A$ is increased.

$$ q \phi_p = q \chi_{Si} + \frac{E_g}{2} + kT \ln \frac{N_A}{n_i} $$

$$ q \phi_{ms} = 4.1 - [4.15 + 0.55 + kT \ln \frac{N_A}{n_i}] = -0.6 - kT \ln \frac{N_A}{n_i} \quad (17) $$

The magnitude of work function difference increases as $N_A$ is increased.

**Work function difference for Al-SiO$_2$-pSi system**

*Fig. 2A p 557*
The work function difference is responsible for band bending in MOS capacitor as the metal is joined to pSi by an external connection or a supply voltage is applied.

Fig. 3(a) shows an Al-SiO₂-pSi MOS capacitor. Here, a positive gate voltage is applied. This leads to some depletion, depending on the magnitude of $V_G$. At equilibrium there is some depletion due to metal-pSi work function difference.

Fig. 3(b) Plot of charge density, electric field, voltage, and electron energy band diagram. As can be seen from Fig. 3b, the gate voltage appears partly across oxide layer (d) and partly across the semiconductor surface. This results in increase in the depletion layer thickness W. From $x=0$ which is the metal-oxide interface, the edge of the depletion layer is at $x=d+W$.

Where, $Q_G =$ surface charge density (per unit area basis), $\rho = q \, N_A^- =$ volume charge density in the depletion region ($N_A^- = N_A$, if all acceptors are ionized)
$$V_T = V_{FB} - \frac{Q_{sc}}{C_0} + 2\psi_B$$

$$Q_{sc} = -q N_A W_m \quad V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

**Fig. 4, p. 561 MOS under threshold**

**Fig. 5 p. 562 MOS under Inversion**
MOS under Accumulation Fig. 6, p 563
Equilibrium vs Flat Band

A) Equilibrium
\[ qV_{ox} + q\psi_s = qV_{FB} \]
Accumulation
\[ qV_G > qV_{FB} \quad \text{or} \quad V_G > |1.557| \] But \( V_G \) is negative voltage.
\[ qV_G > 1.557 \text{ eV} \]

B) Flat Band
We need to apply a negative gate voltage of \( V = V_{FB} = -1.557V \)
Energy band diagram

Fig. 7B Energy band diagram under equilibrium, depletion, threshold and inversion. Page 564
C-V plot

\[ C_{\text{Dep}} = \frac{\varepsilon_s \varepsilon_o}{W} \quad C_{\text{ox}} = \frac{\varepsilon_o \varepsilon_o}{d} \]

Depletion Width \( W \) varies with gate voltage. It is zero under flat band condition, finite under equilibrium, and reaches maximum \( W_m \) at threshold and inversion.

MOS capacitance is made up oxide capacitance \( C_{\text{ox}} \) and depletion capacitance \( C_{\text{dep}} \). Since depletion width \( W \) varies with gate voltage, the depletion capacitance varies. Oxide capacitance remains fixed. The above plot shows capacitance under high-frequency conditions. Since it takes time to form inversion layer, it cannot respond at high frequency. The behavior at low frequency is different.
8.5 Capacitance as a function of gate voltage

Eq. 25 describes the gate capacitance $C_g$ as a series combination of oxide capacitance and depletion capacitance.

$$C_g = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{dep}}} = \frac{C_{ox}}{1 + \frac{W \varepsilon_{ox}}{d \varepsilon_{si}}}, \quad (25)$$

Here, the expressions for oxide $C_{ox}$ and depletion $C_{dep}$ capacitances are:

$$C_{ox} = \frac{\varepsilon_{SiO_2} \varepsilon_0}{d} \quad \text{and} \quad C_{dep} = \frac{\varepsilon_{Si} \varepsilon_0}{W}.$$ 

Here, depletion width $W$ changes as gate bias is applied.