L13 04202017 ECE 4211 UConn F. Jain
Scaling Laws for NanoFETs
Chapter 10 Logic Gate Scaling

Scaling laws: Generalized scaling (GS) p. 610

Design steps p.613

Nanotransistor issues (page 626)

Degradation mechanisms in NanoFETS (p.627-635)

Logic Gate Sizing NMOS

CMOS

Equivalent Circuits, Capacitance calculations

scaled-down potentials/voltages $\phi' = \phi/k$, here, $k > 1$

scaled-down dimensions $(x',y',z') = (x,y,z)/\lambda$, here, $\lambda > 1$

scaled-down concentrations $(n',p',N'_D,N'_A) = (n,p,N_D,N_A)/\delta$, $\delta = k/\lambda^2$,

Parameters	**LATV 1.3micron**	**0.25 micron QMDT* (IBM)**	**25nm SiGe (Home work)**	**Scaling factor**	**Comments**
Channel Length L(μm)	1.3	0.25	0.025	λ=10	
Gate Insulator Oxide t_{ox} (nm)	25	5.0 (SiO_2)	0.5 (SiO_2)	10	$0.5(\varepsilon_{HfO2}/\varepsilon_{SiO2})$ = 1.7nm
Junction Depth x_j(nm)	350	70-140	7-14	10	Gives high Rs and Rd
V_{TH} (V) V_{TH} =4x ΔV_{TH}	0.6	0.25 V'_{TH} =4x $\Delta V'_{TH}$ $\Delta V'_{TH}$ =0.06	0.06 V'_{TH} =4x $\Delta V'_{TH}$ $\Delta V'_{TH}$ =0.015	κ=4	ΔV_{TH}=0.015V
$V_{DS} = V_{DD}$ (V) V_{DD} = 4 x V_{TH}	2.5	1.0	0.25	κ=4	
Band Bending (V)	1.8	0.8	0.3	?	
Doping N_A (cm^{-3})	$3x10^{15}$	$N_A = 3\times10^{16}$	$N'_A=7.5\times10^{17}$	N_A x λ^2/κ=25	
(Rs + Rd)ID IR Drop (mV)	NA	< 10mV	< 1mV	??	How to solve this
RC Delay τ (ps)	Not appl. (NA)	100ps	2-5 ps??	??	How to solver this

Generalized Scaling (Baccharini et al 1984)

Design steps using GS

1. Find dimensional scaling λ from existing channel dimensions and desired scaled- down

2. Using processing parameters, determine threshold variation ΔV_{TH}

Determine V_{TH} ($=\sim 4\ \Delta V_{TH}$) and V_{DD} ($V_{DD} \sim 4 * V_{TH}$)

3. Find the scaling for voltages k

4. Compute the scaling factor δ for doping.

Verification of scaled-down design

1. Is the oxide thickness realistic in terms of gate leakage current?

2. Is supply voltage and threshold realistic in terms of source to drain tunneling?

3. Is the device to device fluctuation in a die and in dies in a wafer acceptable?

4. Is the drive current acceptable? Is the ID-VG and ID-VD characteristics ok in terms of fan-in and fan-out and logic noise margins?

ΔV_{TH}

$$V_T = V_{FB} - \frac{Q_{SC}}{C_o} + 2\psi_B = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} + \frac{1}{C_o} q N_A \sqrt{\frac{2\varepsilon_{sr}\varepsilon_o 2\psi_B}{q N_A}} + 2\frac{kT}{q}\ln\frac{N_A}{n_i}$$

$$q\phi_{ms} = q\phi_m - q\chi_{Si} - \frac{E_g}{2} - kT\ln\frac{N_A}{n_i}$$

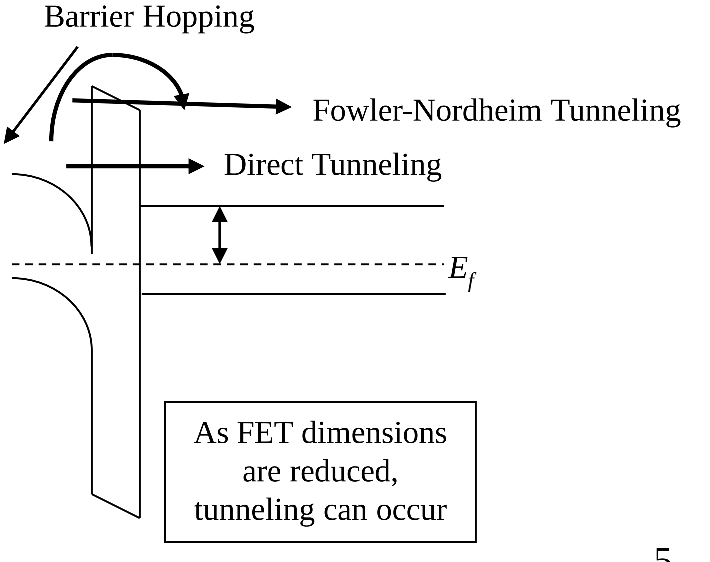
Dopant density variation (due to implant or in substrrate)
Oxide or gate insulator thickness variation
Oxide dielectric constant variation in thin films of 1-2nm
Channel width and length variation,
Oxide charge density variation

Nano-transistor scaling issues p. 626
FET operation as partially depleted or fully depleted

Degradation Mechanisms:

1. Poly-Si gate depletion and increased gate capacitance
2. Source to drain tunneling, loss of gate control
3. Channel to gate tunneling for thin oxides:
   a. Fowler-Nordheim tunneling;
   b. Direct Tunneling
4. Gate induced drain leakage
5. Oxide breakdown

Trapping of channel electron under gate ox

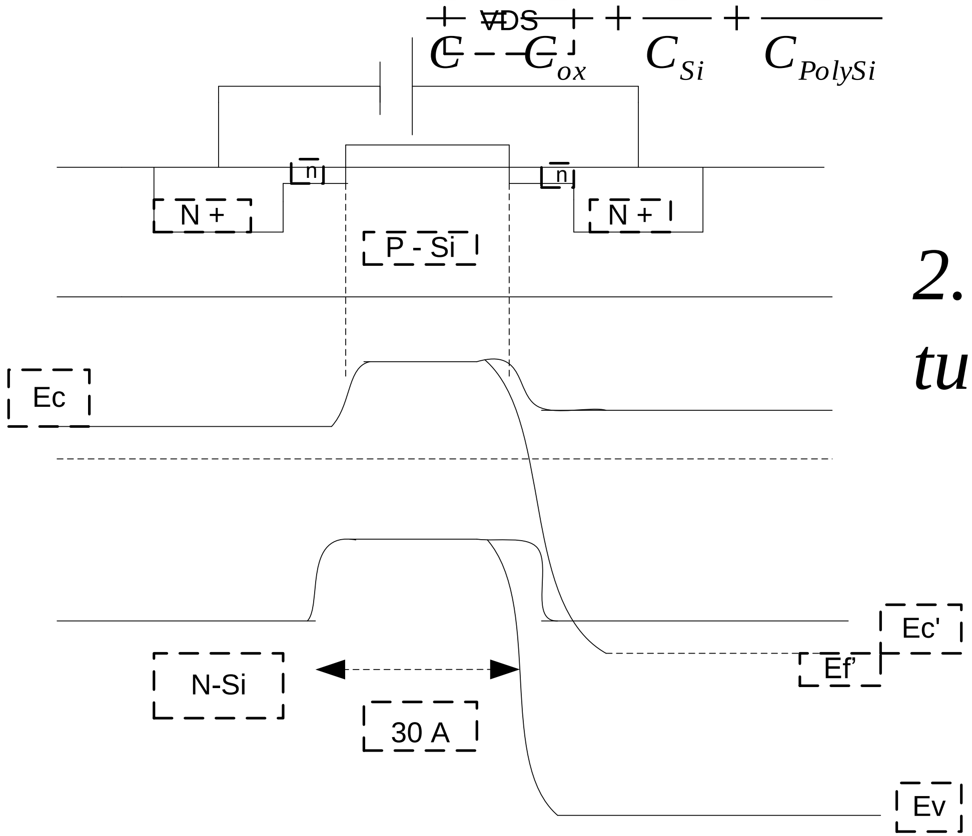


Degradation Mechanisms (627)

1.Poly-Si gate depletion and increased gate capacitance

Poly silicon region: Poly-Si may be implanted during processing using ion implantation. However, with this method, some poly-Si atoms will penetrate through the oxide, causing problems. This damage the gate insulator. The charge in poly-silicon gate depletion represents capacitance.

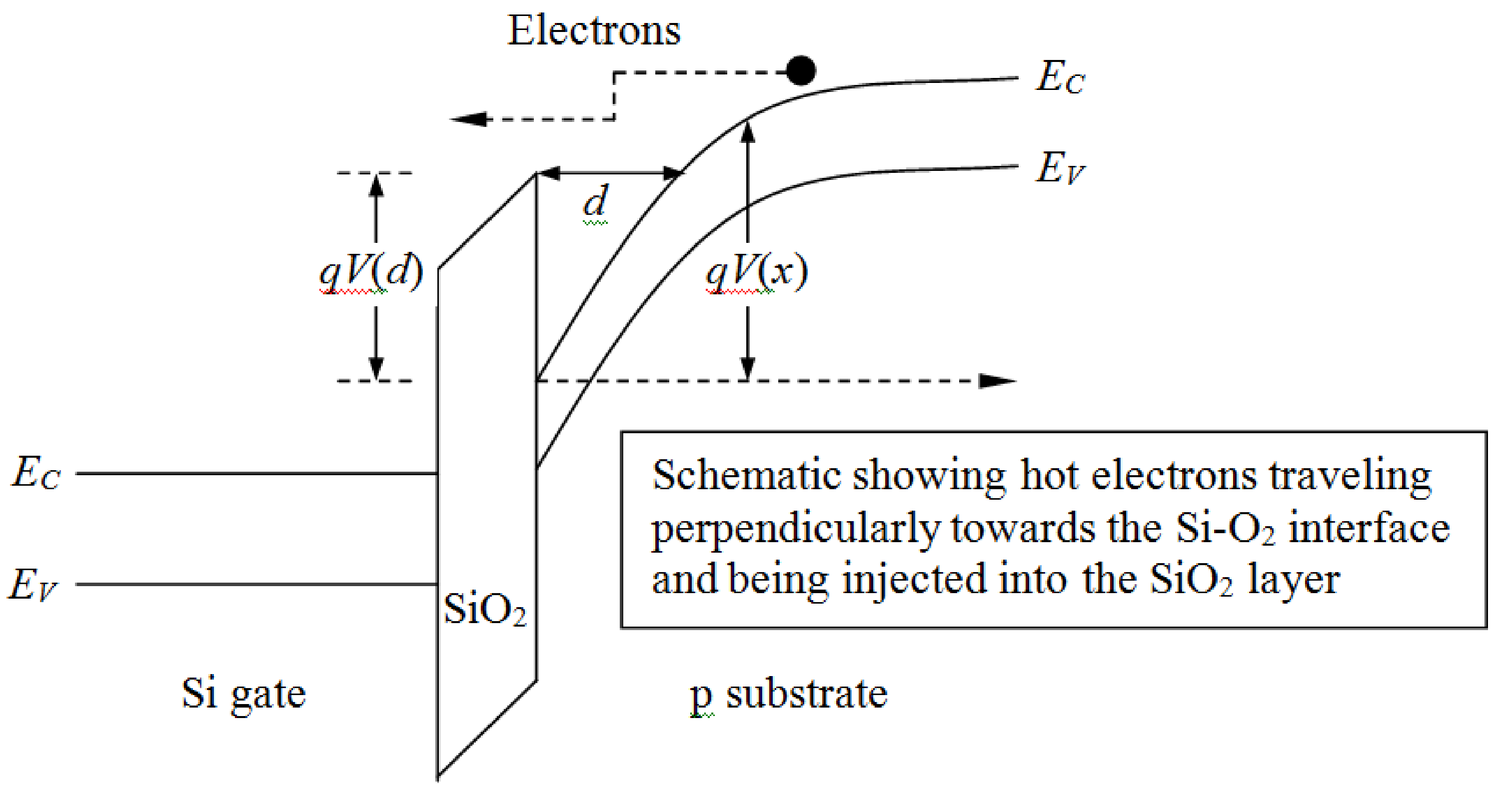
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}} + \frac{1}{C_{PolySi}}$$



2. Source to drain tunneling.

Degradation Mechanisms

3. Channel to gate tunneling.

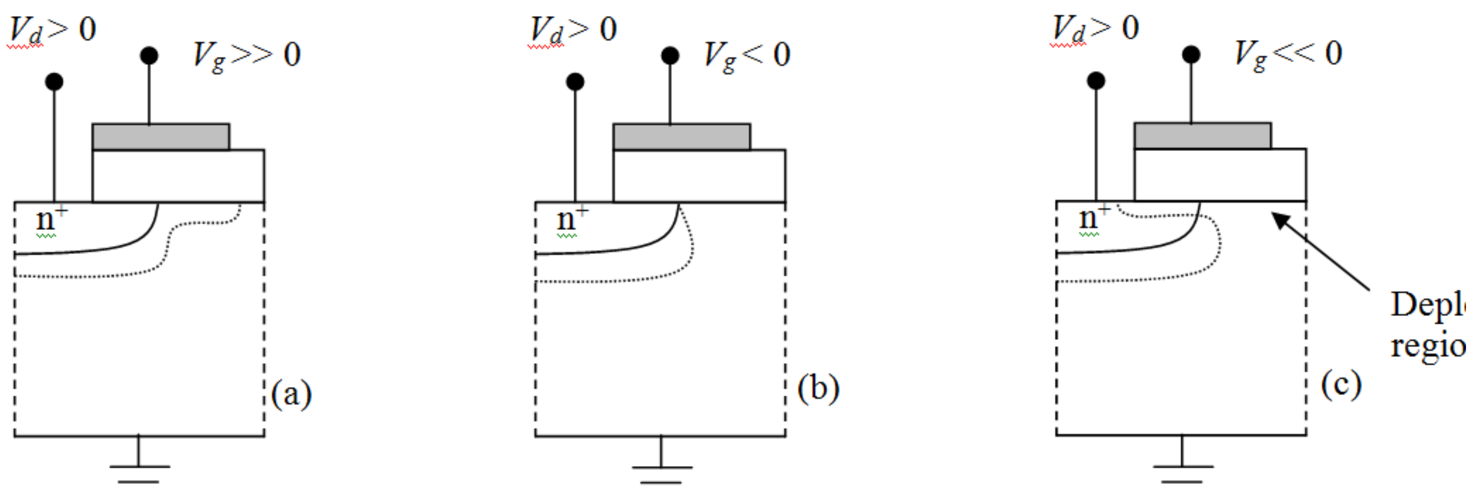


Degradation Mechanisms

4. GIDL.

a. Gate-induced drain leakage (GIDL) current

The narrowing of the depletion layer at or near the intersection of the pn junction and Si-SiO_2 interface caused an increase of the local electric field, called *field crowding* [(b) in fig. below]. Field crowding causes the gate voltage in the drain junction MOSFET to produce increased junction leakage current, called *gate-induced drain leakage*, or GIDL. It is very important to minimize GIDL as much as possible in CMOS devices.



Schematics illustrating a gated n+-p diode when the surface is (a) inverted and (b) accumulated, and (c) when the surface of the n+ regions is depleted or inverted. The

Degradation Mechanisms (p.631)

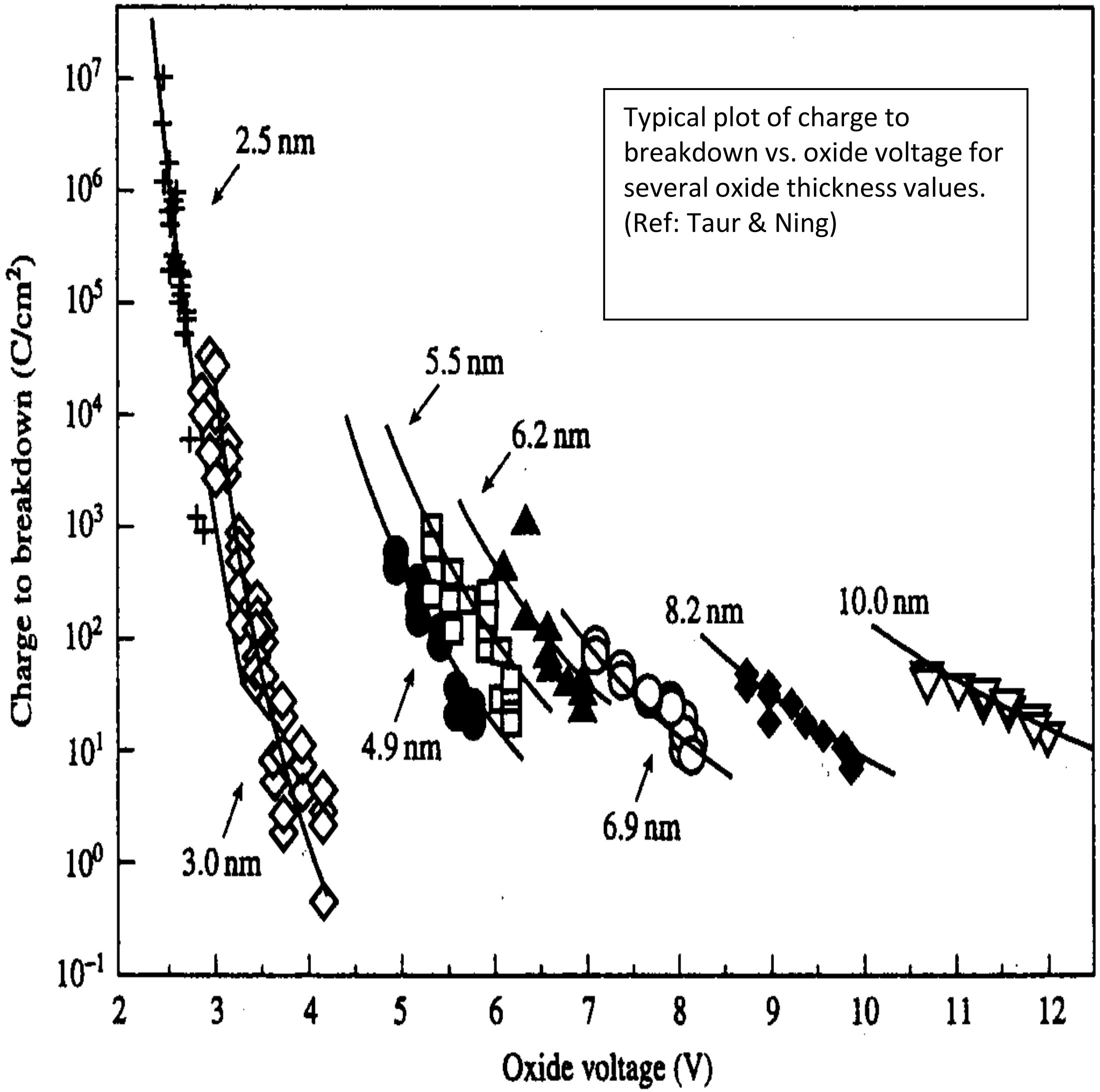
5. Oxide Breakdown

•*Oxide (dielectric) breakdown*

As we have seen, significant electron tunneling can occur when a large electric field is applied across an oxide layer. This tunneling can lead to a condition called *dielectric breakdown*, after which an oxide layer ceases to be a good electrical insulator. Dielectric breakdown can occur either softly (i.e. gradually) or abruptly. The physical mechanisms involved in, and leading to, dielectric breakdown involve:

1. impact ionization in the oxide layer
2. injection of holes
3. creation of electron-hole traps in the oxide
4. creation of sates at oxide-Si interface

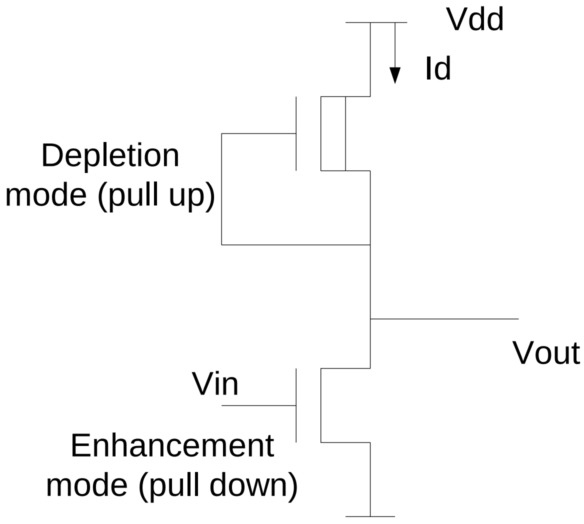
Degradation Mechanisms (631)



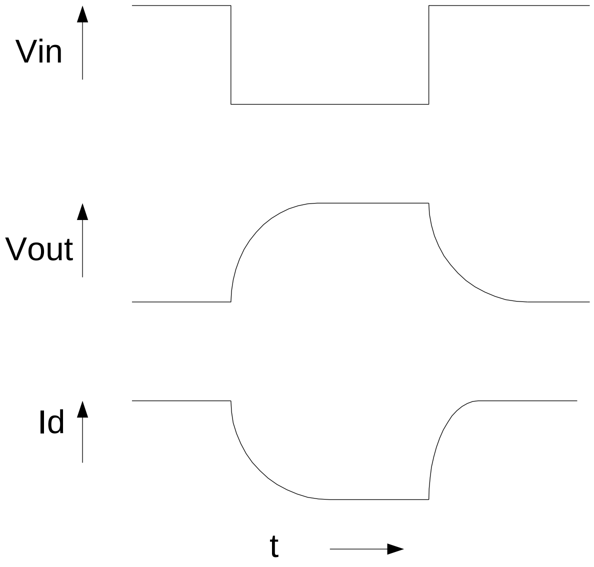
Typical plot of charge to breakdown vs. oxide voltage for several oxide thickness values. (Ref: Taur & Ning)

Chapter 10
NMOS Inverter

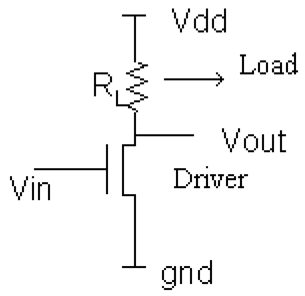
Fig. 1, p. 638

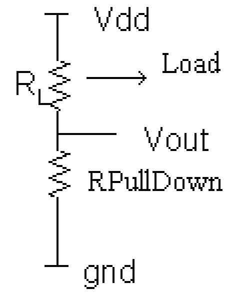


Static or Ratioed Inverter



NMOS Inverter (load and driver resistance ratios) p.639





Rload >> Rpd
>> Rpu

Fig. 2. Inverter with resistive load. Equivalent circuit

i.e. $R_{load} \geq 4-6 * R_{driver}$

or

$R_{PU} \geq 4-6 * R_{Pd}$

$$\left(\frac{L}{W}\right)_{PU} \geq 4-6 * \left(\frac{L}{W}\right)_{Pd}$$

or

$$\frac{\left(\frac{W}{L}\right)_{Pd}}{\left(\frac{W}{L}\right)_{PU}} \equiv \frac{\left(\frac{W}{L}\right)_{driver}}{\left(\frac{W}{L}\right)_{load}} = 6$$

The ratio of $(W/L)_{Pd}$ to $(W/L)_{PU}$ is defined as the inverter ratio β. Some denote it by k.

The choice of W/L ratio determines:

NMOS Inverter Configurations

In an inverter we have basically three choices for load:

a. Resistor R_L

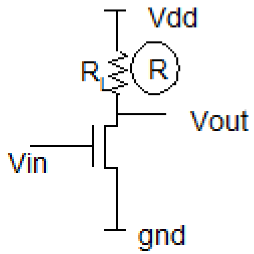


Fig. 3a. Inverter with resistor as load.

b. Enhancement mode transistor as load. Connecting the gates to V_{DD} or a higher voltage make an enhancement mode transistor act as a resistor.

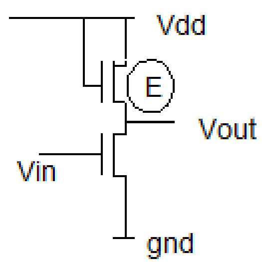


Fig. 3b. Enhancement transistor as the load.

c. Depletion mode transistor as the load.

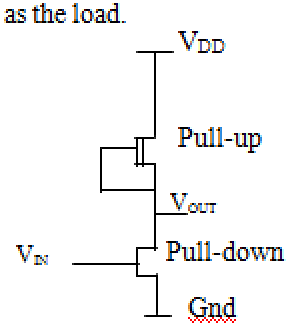


Fig. 3c. Depletion mode transistor as the load.

10.2.2 Device sizing in static (or ratioed) gates/networks

Inverter logic threshold:

$$V_{inv}$$

Important: $V_{inv} \neq V_{TH}$ or V_{TE}

It is the voltage on the input of the enhancement mode transistor that results in an equal output voltage.

i.e. $V_{in} = V_{out} = V_{inv}$

Simplified calculation for V_{inv}:

Assume: Both pull-up and pull-down are in saturation.

$$V_{IN} = V_{INV} = V_{TEo} - \frac{V_{TE,dep}}{\sqrt{(W/L)_{Pd} / (W/L)_{PU}}}$$

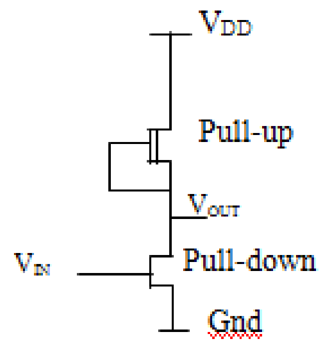
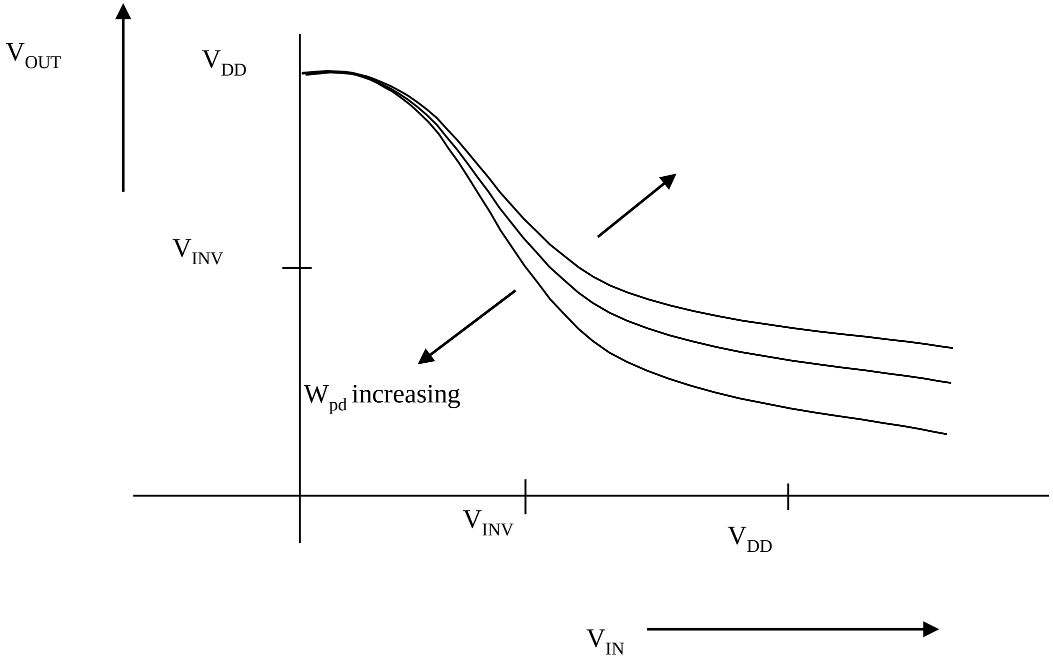


Figure 5. An inverter with pull-down and pull-up devices.

Eq. (8) p. 642

The current in the depletion mode transistor = the current in the enhancement mode

Inverter Gain



The slope of the voltage transfer characteristics

= - Gain (G)

= - G

The gain G increases as W_{Pd} increases

i.e. as $\frac{(W/L)_{PD}}{(W/L)_{PU}}$ increases

Fig. 6. Output-Input voltage characteristics a a function of W_{pd}
The slope of the voltage transfer characteristics

10.2.3 Dynamic logic gates/networks p643

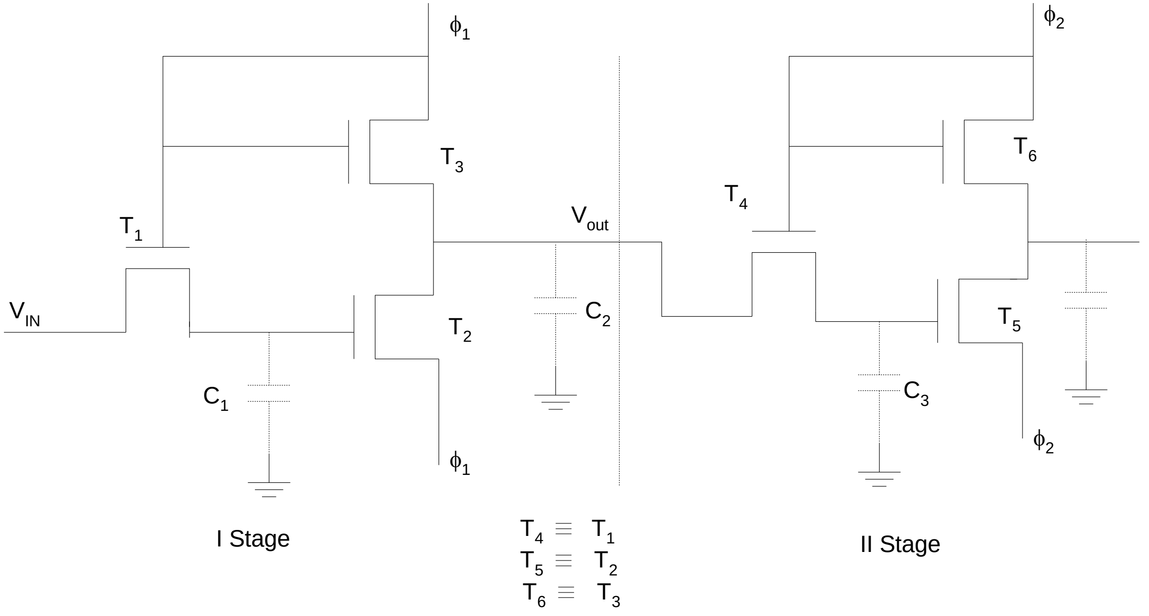


Fig. 7. A dynamic or two-phase ratio-less inverter

Layout of NMOS Inverter

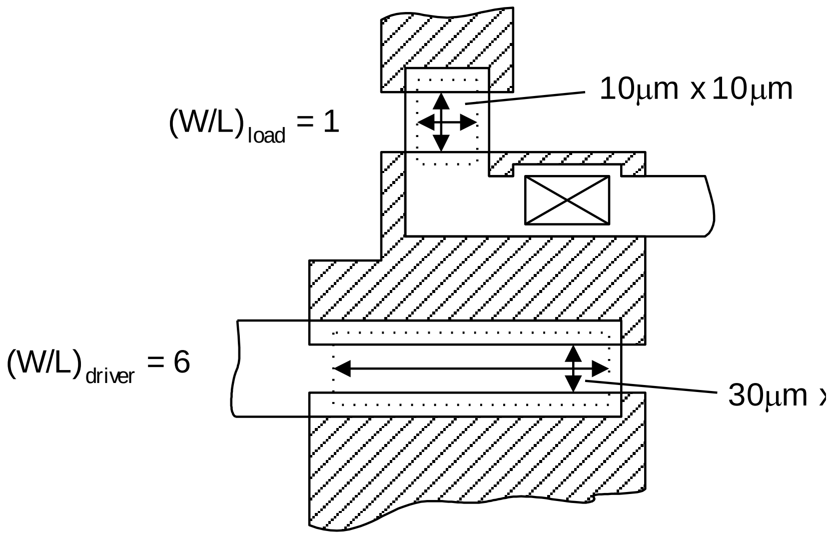


Fig. 10. (b) Schematic and (b) layout an NMOS inverter.

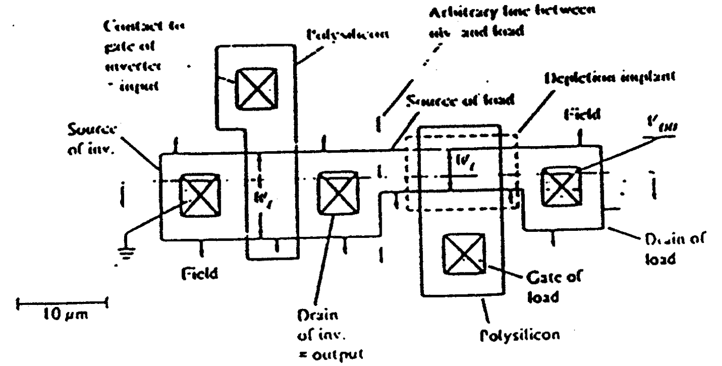
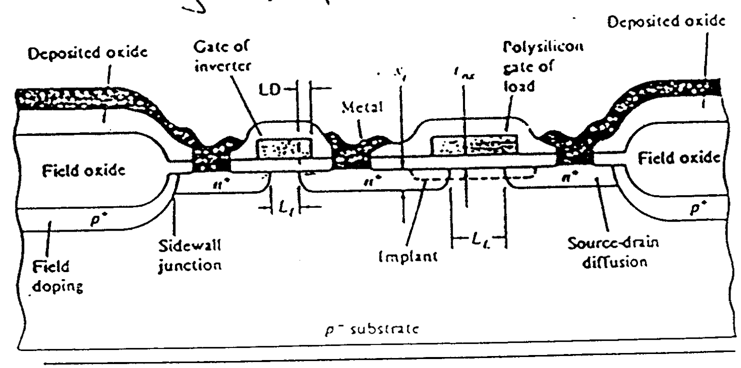


Fig11(a) Top View



Reference: Hodges and Jackson (1983)

Fig11(b) Cross Section

Areas and perimeters are calculated from Fig. 3.6.

Inverter:

Source, drain areas = 10 µm × 10 µm = 100 µm²

Source perimeter = 4 × 10 = 40 µm

Drain perimeter = 10 + 10 + 10 + 5 = 35 µm

Load:

Source area = 5 × 5 = 25 µm²

Drain area = 10 × 10 = 100 µm²

Source perimeter = 5 + 5 + 5 = 15 µm

Drain perimeter = 4 × 10 = 40 µm

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Sizing of FETs in a logic gate (p.647)

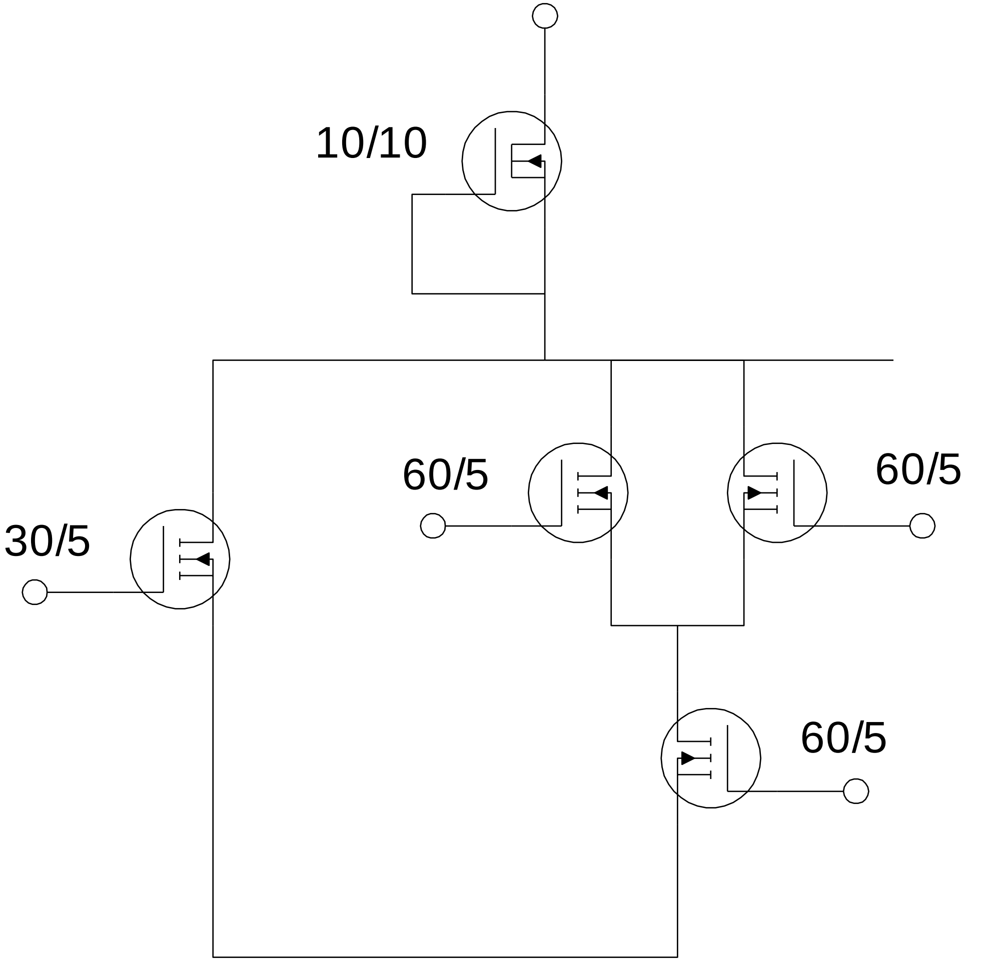


Fig. 11. NMOS gate with W/L ratios of various FETs.

Circuit Model

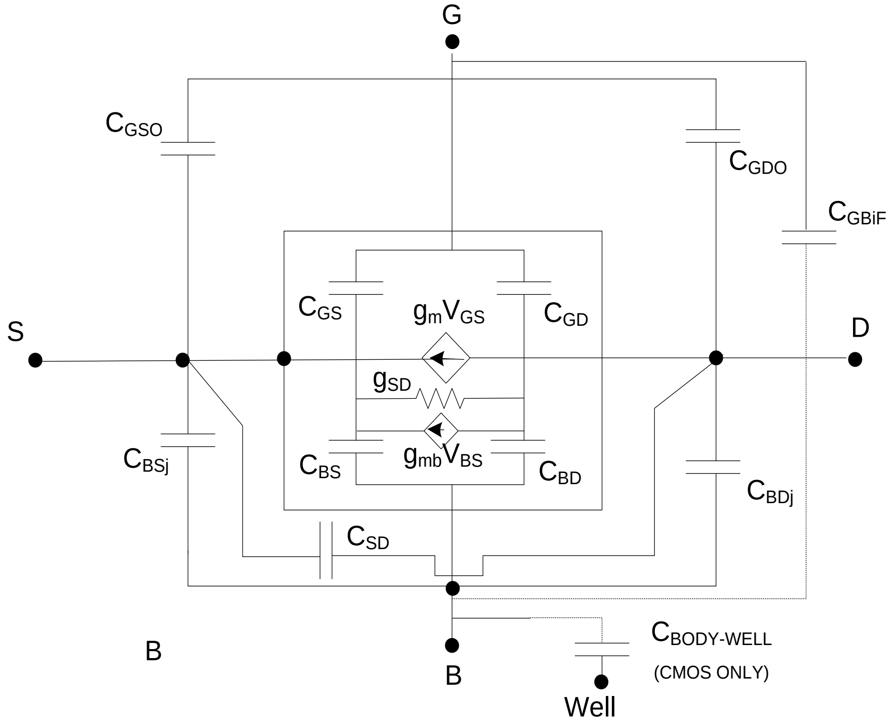


Fig. 14a. Capacitances
Page 650

Fig4 P.24 (Notes)

Extrinsic Model

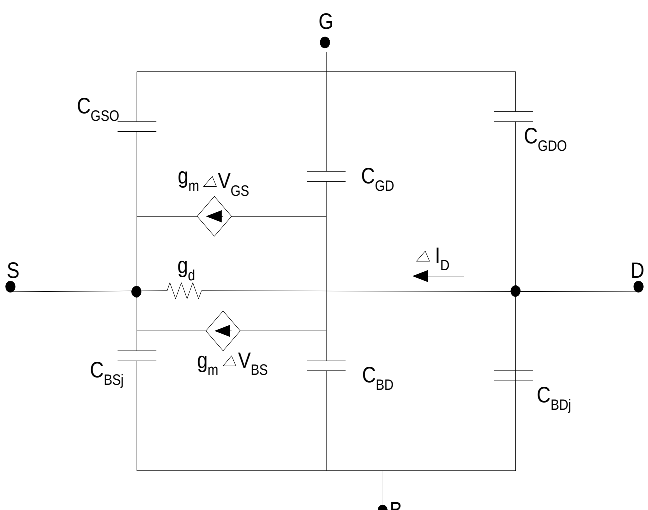
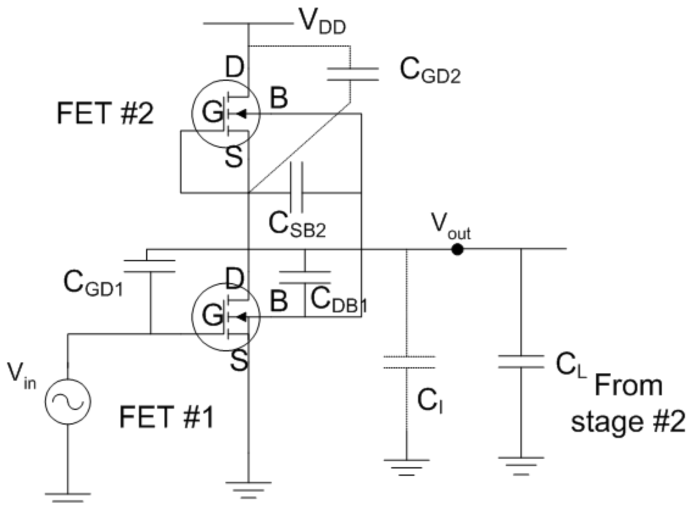


Fig. 14(b) Intrinsic model showing capacitances.

Capacitances are computed to find propagation delay(p. 651-660)



Capacitances from FET #1 and FET #2 and from stage #2.

Fig. 15: Capacitance components (intrinsic and extrinsic) reflected on the output of stage #1.

C_{DB1} :

$C_{DB1} = C_{DB,intrinsic} + C_{DB,junctionz}$

$C_{GD1} = C_{GD,intrinsic} + C_{GDO}$ (Overlap capacitance)

C_{SB2} :

$C_{SB2} = C_{SB,intrinsic} + C_{SB,junction}$

$C_{GD2} = C_{GD,intrinsic} + C_{GDO}$ (Overlap → Extrinsic)

C_I = Interconnect Capacitance

$$C_T = C_{DB1} + C_{GD1} + C_{SB2} + C_{GD2} + C_I + C_{G3} \qquad (9)$$

The bias dependent capacitances include C_{DB1} and C_{SB2}.

inverter pair delay:

$$t_{\substack{inverter\\pair}} = t_p\big|_{HI-2-LO} + t_p\big|_{LO-2-HI}$$

$$t_{inverter} = 2C_L R_{PD} + \left[2R_{PU} C_L \left(t_{off} - t_{in}\right)\right]^{1/2} \quad \text{for } t_{out} < t_{off}$$

or

$$t_{inverter} = 2C_L R_{PD} + R_{PU} C_L + \tfrac{1}{2}\left(t_{off} - t_{in}\right) \quad \text{if} \quad t_{out} \geq t_{off}$$

In summary, the delay depends on the output capacitance of the inverter and the charging and discharging currents through the PU and PD transistors.

p.660 CMOS Inverter

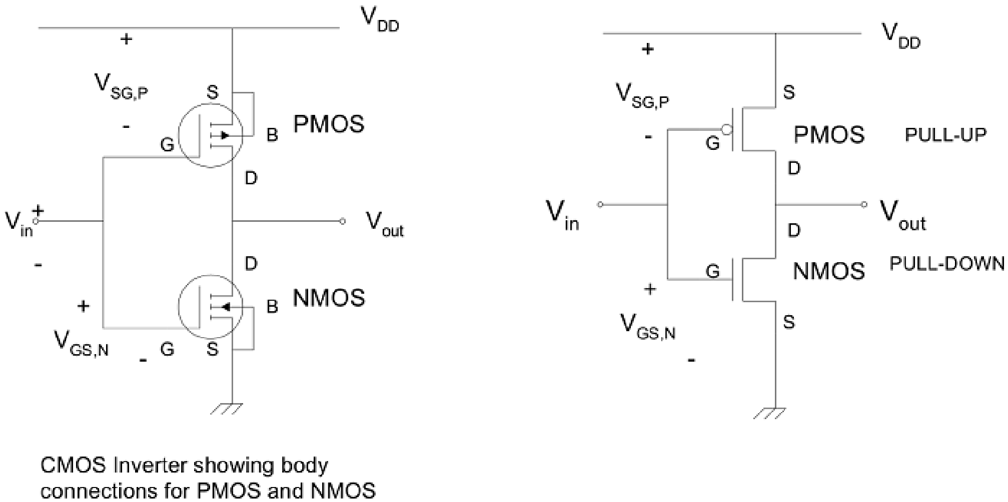
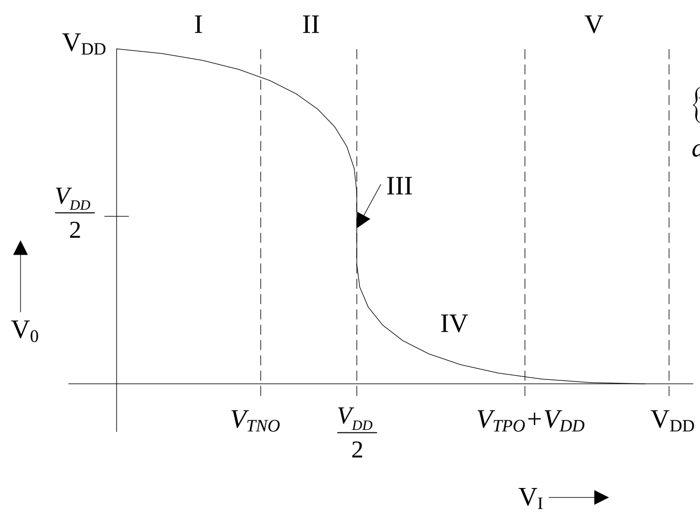
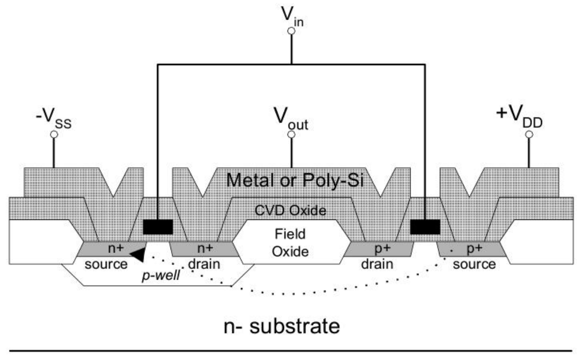


Fig. 19: A CMOS inverter using an NMOS and PMOS FET.



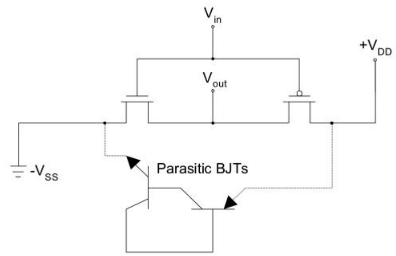
$$\{V_{DD} + V_{TPO} = V_{DD} - |V_{TPO}|\}$$
$$as\ V_{TPO} \langle\ 0$$

p.661 Fig. 21 Voltage transfer characteristic



Cross Section of CMOS inverter Structure

Latch-up Phenomenon



Equivalent Circuit

Fig. 33. Latch up in CMOS inverter (p672)

we need to make:

$$\frac{\left(\frac{W}{L}\right)_{PMOS}}{\left(\frac{W}{L}\right)_{NMOS}} = \frac{\mu_N}{\mu_P} \qquad (15)$$

Generally, μ_N is 2 to 2.5 times higher than μ_P. Therefore,

$$\left(\frac{W}{L}\right)_{PMOS} = [\text{between 2 and 2.5}] \times \left(\frac{W}{L}\right)_{NMOS} \qquad (16)$$

Some authors (Hodges and Jackson) take

$$\left(\frac{W}{L}\right)_{PMOS} = 2.5\left(\frac{W}{L}\right)_{NMOS} \qquad (17a)$$

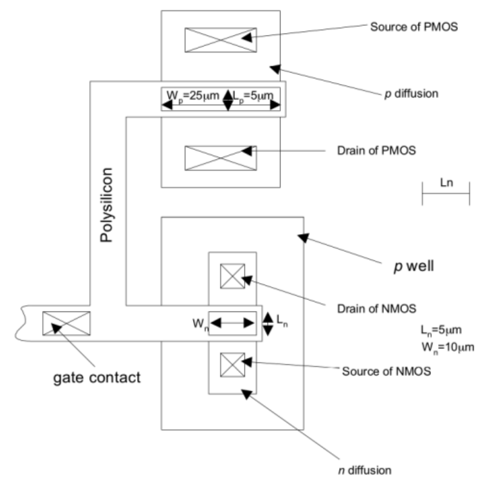
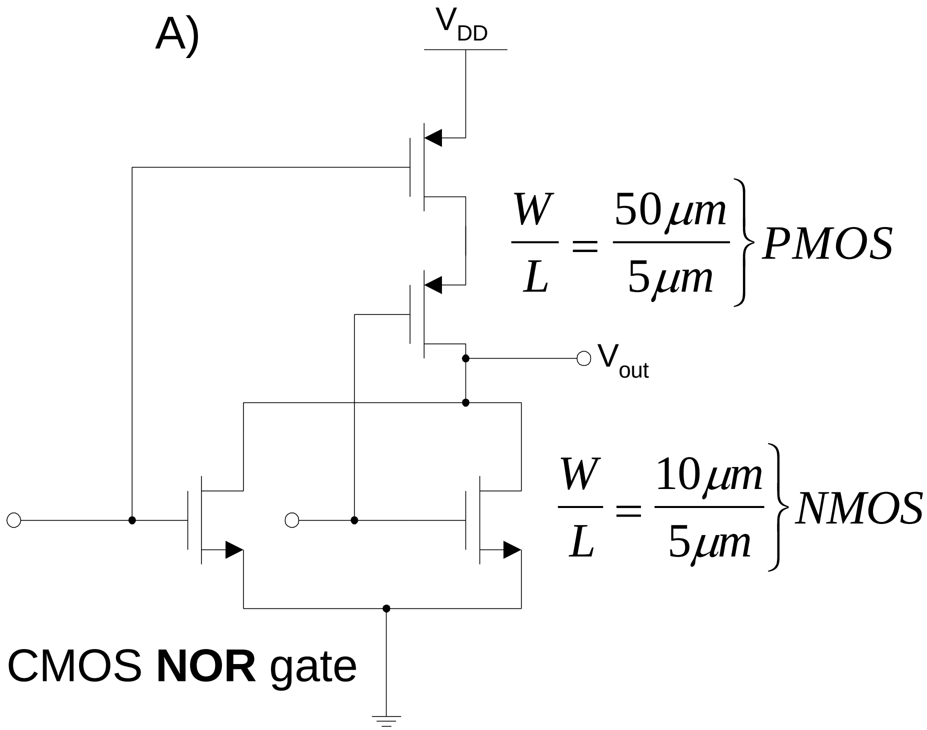


Fig.8 CMOS Inverter
(Ref: Hodges & Jackson)

Fig. 26. Sizing of CMOS transistors (p 668)



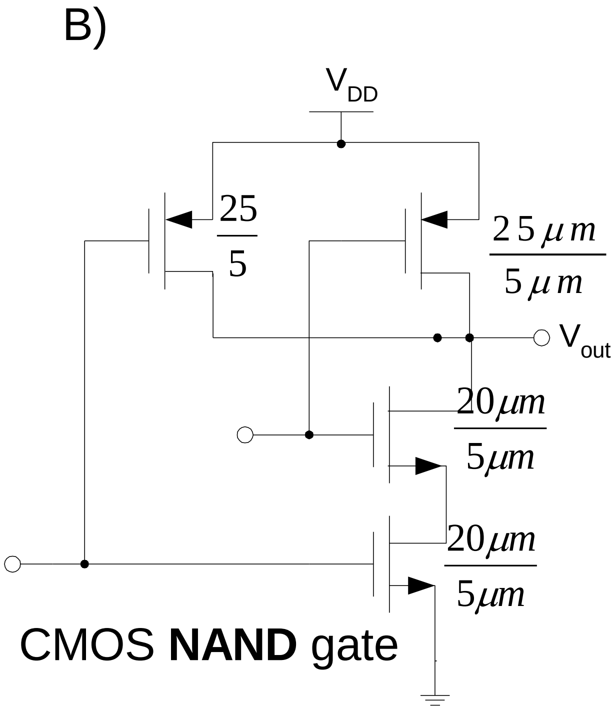
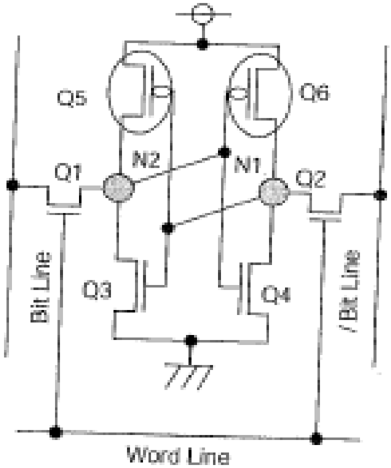
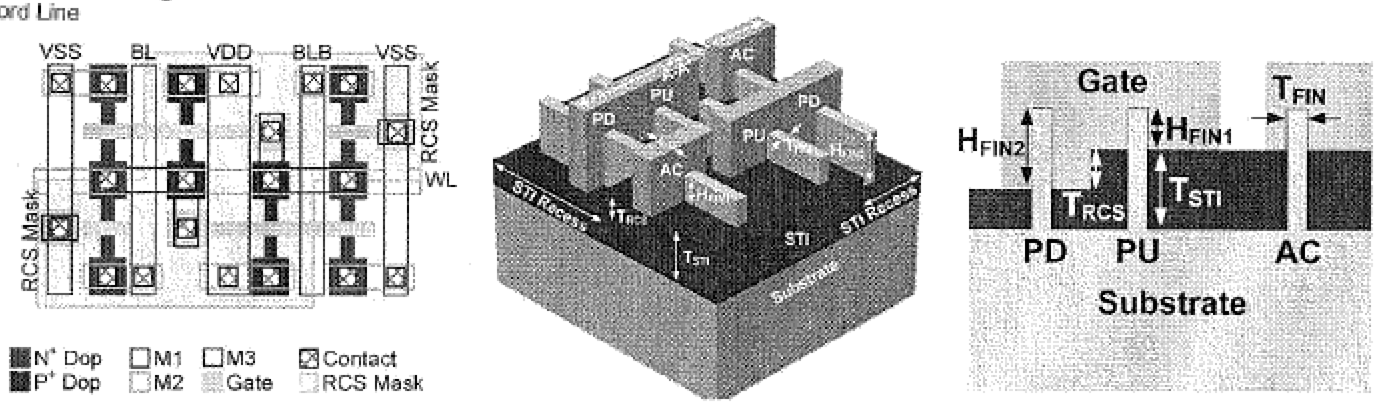


Fig. 27 Sizing of 2-input NOR 2-input NAND CMOS inverter (p668)



FIN-FET Static RAM



(a) (b) (c)

(PD = Pull-Down; PU=Pull-Up; AC=Access)

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Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights

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