**UCONN ENGR\_ECE 4243/6243 HW11 FET-I & Solution 11152016 F. Jain**

**QUIZ 2 part B Take Home will be like Q.6. It will be given on 11/22/16**

Q.1. (a) Find the work functions for n and p-type Si for the doping levels given below. Show them in relation to vacuum energy level being zero as the reference.

The electron affinity of Si is qχSi = 4.15 eV.

**p-side**: Acceptor concentration NA=1015 cm-3, τn=10-5 sec. Dn=40 cm2/sec.

Effective mass: electrons me=mn=0.26mo, holes mh=mp= 0.64 mo,

Junction area A=10-3 cm-2, ni (300K) =1.5×1010 cm-3. εr(Si)=11.8, ε0=8.85×10-14 F/cm, εs=εrε0. Assume all donors and acceptors are ionized at T=300 K. Eg = 1.1eV,

Boltzmann Constant k= 8.65x10-5 eV/K.

**n+-side**: Donor concentration ND=1018 cm-3, minority hole lifetime τp=2×10-6 sec.

 Minority hole diffusion coefficient Dp=12.5 cm2/sec.

(b) Compute the work function difference nSi-pSi (=nSi - pSi) and show that it is equal to the built-in voltage.

**Solution Q1(a)** Work function is expressed as





**Ef - Ei is obtained from the definition of intrinsic Fermi level Ei:**

, if we take natural log (ln) we get



Work function of p-Si: Doping NA=1015cm-3

Intrinsicconcentration





Taking log (ln) we get, 



Note Ei - Efp = q

Q1(b) Work function differences are negative values



Same as we calculated from the well-known Vbi expression for p-n junctions. =0.754V

Q.2 Compute the flat band voltage Vfb and threshold voltage VT (or VTH) for an Al-SiO2-pSi MOS capacitor having the following parameters: T=300K.

 Qox = 2.103 x 10-8 C/cm2 εSi = 11.8

Oxide thickness = d = 1000Å (1Å = 10-8 cm), ni = 1.5x1010 cm-3

qχSiO2 = electron affinity of SiO2 = 0.9 eV NA = 1016 cm-3

εox = 3.9, εo = 8.854x10-14 F/cm qχSi = 4.15 eV (affinity of Si)

# Intrinsic Fermi level is Ei ~Eg/2, Eg (Si) = 1.1eV qAl = 4.1 eV (work function of Al).

 Assume Qox to be located in the SiO2 near the Si interface.

HINT set: VFB= ms – Qox/Cox ( Qox assumed to be located in SiO2 near the SiO2-Si interface).

VFB= ms if there is no oxide charge. ms = m  -s = Al - pSi . Find the work functions and compute ms.

**Solution Q.2**

**Evaluation of Flat Band voltage**: Vfb=VFB=Flat band voltage



and 





Thus, = -1.552V

**Evaluation of threshold voltage** **VTH**:

 where

or 

C/cm2



and V. Substituting in threshold expression, we get



\*\*\*\* \*\*\*\* \*\*\*\* \*\*\*\*

**New** Q.3(a). The threshold voltage is altered by: Circle correct answers

Gate metal charge in the gate oxide source doping substrate doping

(b) For a given metal-oxide-pSi MOS capacitor, which one will have higher threshold? Circle

Al-SiO2-psi or Au-SiO2-pSi

(c) What is the advantage in replacing gate metal by doped poly Si layer as the gate layer?

 Adjustment of threshold voltage,

 Enabling deposition of oxide for gate isolation in ICs

(d) Why in 22 nm FETs poly Si is not used and TaN or TiN metals are used?

 Because of lower threshold so that devices can use VDD ~ 0.5V.

**Q.4 (a)** Compute the drain current for VD=0.5V and VD=2.5V at VG=2V and 4V.

First, we need to find the saturation voltage VD (set) for VG=2V and for VG=4V.

VD (sat) ≈ VG-VTH using Case I Approximation.




**Given: Channel length L = 10 μm, channel width Z = 40 μm, operating temperature T = 300K, and channel mobility μn = 800 cm2/Volt⋅sec., Qox = 2.103 x 10-8 C/cm2, εSi = 11.8, Oxide thickness = d = 1000 Å (1 Å = 10-8 cm), ni = 1.5x1010 cm-3, qχSiO2 = electron affinity = 0.9 eV, NA = 1016 cm-3, εox = 3.9, qχSi = 4.15 eV, εo = 8.854x10-14 F/cm, qAl = 4.1 eV**

**The intrinsic Fermi level Ef= Ei ~Eg/2.**



**CASE I:**













We use the linear regime ID equation for VD < VD(sat)



**Summary Table**

|  |  |  |
| --- | --- | --- |
| ID | VG | VD |
| 6.718x10-5A | 2V | 0.5V |
| 1.187x10-4A | 2V | 2.5V |
| 1.775x10-4A | 4V | 0.5V |
| 6.118x10-4A | 4V | 2.5V |

**Q.4(b)** Find saturation current and voltage VD(sat) at the VG = 4V.

ID(sat) at VG=4.0 V

Using Case-I definition of VD(sat)

VD = VD(sat) = VG – VTH =4.0-0.533=3.467 volts



**Q.4(c)** Calculate the channel conductance gD and the transconductance gm at the following drain voltages VD = 0.5 V and VD = 2.5 V.

 gm at VD=0.5 V, VD=2.5 V, VG=4.0 V (likes part b)

Find gd at VD=0.5 V, VD=2.5 V VG=4.0 V

gm for VG =4.0 V:

VD(sat) = VG –VTH = 4.0 – 0.533 = 3.467 V.

So both VD=0.5 V & VD=2.5 V will give unsaturated linear regime values.



Drain conductance; 

For VG=4.0 , VD(sat)=3.467 V(VD=0.5 V, 2.5 V are below Saturation )



**Q.4(d)** If the gate is n+ poly Si (ND = 1x1019cm-3), calculate the flat band and threshold voltage assuming the same Qox as in part (a).

Gate is n+ poly Si , ND=1019 cm-3



Note: In Part Q4(a), VFB = -1.557 V, and in part Q1(d) VFB =-1.4825 V



The parameters used are from Q4(a).



Q4(e) Calculate the transconductance gm in the linear regime. From Q1(c) we have

 . It depends on VD.

Q4(f) What is the cut off frequency fT (= gm/(2 Cg)) of this FET? Cg is the gate capacitance which varies between Cox and Cox/3 depending on the depletion width variations. It also depends on the drain and source to body capacitance.

Using gm =2.76\*10-4 from part Q1(d) at VD = 2.5V, and Cg = Cox/3 = 3.45\*10-8/3=1.15\*10-8 F/cm2. Here we have used the capacitance of unit area (L\*Z = 1 cm2).

fT =2.76\*10-4/(2 \*1.15\*10-8) = 3819.71 Hz for a 1cm2 gate area FET.

For FET with dimensions L=10 m and Z=40 m,

fT = 3819.71/(10m \* 40m) =9.54\*108 Hz.

**Q.5(a)** The resistance of load transistor is 4 to 6 times higher than of the driver transistor resistance. Resistance is inversely proportional to (W/L) ratio.

As a result, (W/L) Driver = 4 to 6 \* (W/L) Load.



 Fig 1. Schematic of an NMOS logic gate. W/L (or Z/L) ratios are shown. **Justification:** When there are more than one transistor is in series on the driver side (i.e. below the output), we increase the (W/L) ratio by the number of transistors in series. Two transistors T1 and T3 are in series with size = 2\*20/5=40/5.Similarly, T2 and T3 are in series with same sizing.

**Q5(b)** The PMOS-FET (W/L) is made 2.5 times larger than (W/L) of NMOS. This is done to charge and discharge the load capacitor CL (at the output of a CMOS gate). When input voltage goes from low to high, discharging of CL (which was at VDD) takes place through NMOS FET. Similarly, charging happens through PMOS FET when the input changes from high-to-low.



Fig.2 shows the topology of this CMOS inverter.

|  |
| --- |
|  Fig.2 CMOS Inverter on p-Si substrate |

**Q.5(c)** Justify the W/L ratios shown for CMOS NOR and NAND gates in Fig.3.



Fig. 3 W/L ratios for CMOS NOR and NAND gates.

NOR gate Fig.3(A). Here two P-MOS FETs are in series. When both are “ON”, we need to reduce their total series resistance to equivalent of one transistor.

The W/L ratio is multiplied by number of FETs in series.

 (W/L) P-MOS when two in series =2\*(W/L) P-MOS when single =2\*(25/5)=50/5

Fig.3 (B) is a NAND. This gate has two NMOS in series. Therefore,

 (W/L)N-MOS when two in series(NAND) =(10/5) \*2# FET in series =20/5

**Q.6**. NANOFET Design:

(a) Outline the steps used in scaling a FET from 1.3 micron to 0.25 micron is described in Baccarani et al (1984 paper) and shown in Table I below.

**Design steps:** 1. Find the dimensional scaling factor l which is L/L’ or W/W’ or Tox/Tox’.

2. Find the V’TH for the new scaled down FET including process variations, masking registration errors, doping changes. Find V’TH= 4 V’TH. Find V’DD = 4 V’TH.

Calculate scaling factor for voltages and potentials: k = VTH/ V’TH

3. Find 

4. Compute new substrate doping N’A = NA/ = (2/k) NA

**Table I Hint set for 25nm FET design**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameters** | **LATV****1.3micron** | **0.25 micron QMDT\* (IBM)** | **25nm SiGe** **(Home work)** | **Scaling** **factor** | **Comments** |
| Channel Length L(μm) | 1.3 | 0.25 | 0.025 | λ=10 |  |
| Gate InsulatorOxide tox (nm) | 25 | 5.0 (SiO2) | 0.5 (SiO2) | 10 | 0.5(HfO2 /SiO2)= 1.7nm |
| Junction Depth xj(nm) | 350 | 70-140 | 7-14 | 10 | Gives high Rs and Rd  |
| VTH (V)VTH 4xVTH | 0.6 | 0.25V’TH 4xV’TH V’TH =0.06 | 0.06V’TH 4xV’TH V’TH =0.015 | κ=4 | VTH=0.015V |
| VDS = VDD (V)VDD = 4 x VTH | 2.5 | 1.0 | 0.25 | κ=4 |  |
| Band Bending (V) | 1.8 | 0.8 | 0.3 | ? |  |
| Doping NA (cm-3) | 3x1015 | N’A =3×1016 | N’A=7.5×1017 | NA x λ2/κ=25 |  |
| (Rs + Rd)IDIR Drop (mV) | NA | < 10mV | < 1mV | ?? | How to solve this |
| RC Delay  (ps) | Not appl. (NA) | 100ps | 2-5 ps?? | ?? | How to solve this |

**Scaled down FET Original FET**

1. Dimensions

L’, W’, Tox’ $^{L}/\_{λ,} $ $^{W}/\_{λ,}^{T\_{ox}}/\_{λ}$ $ λ>1$

1. Voltages

VGS’, VDS’ ,VTH’ $^{ V\_{GS}}/\_{k,}^{V\_{DS}}/\_{k, }^{V\_{TH}}/\_{k}$ $k>1$

1. Doping Levels

NA’, ND’ $^{ N\_{A}}/\_{δ,}^{N\_{D}}/\_{δ }$ $ δ<1$

Since $δ=^{k}/\_{λ^{2}}$ and (1/= 2/k, substrate doping NA’ is higher. [Pages 579-580 Notes III]

Q6(b) Scale down a 0.25 micron FET to design the 0.025 micron (25nm) transistor following the 10-fold scaling. Given VTH = 0.015V for 25 nm process. Justify the values given in Table I.

For 0.025micron FET, use VTH = ¼ of VDD. Assume VDD of 0.4 Volt. Obtain gate oxide thickness, Si doping levels, source and drain thicknesses and doping etc. The three design steps to obtain 0.25μm FET from 1.3μm FET are shown below

|  |  |  |
| --- | --- | --- |
| 1.3 μm channel length L FET | 0.25 μm FET channel length L’  | Scaling factor |
| L = 1.3 μm Tox = 25 nmVDD = 2.5 VVTH = 0.6 V | L’ = 0.25 μm Tox ’= 5 nmVDD ’= 1 VVTH ’= 0.25 V | L’=$^{ L}/\_{λ,}$ $λ=$ $^{ 1.3}/\_{0.25} $= 5VDD’=$^{ V\_{DD}}/\_{k,}$ $k=$ $^{ 2.5}/\_{1} $= 2.5 |
| Substrate doping NA Scaling factor δ | NA’ = NA$ \frac{ λ^{2}}{k}$ = NA / δδ = k / $λ^{2}$ | NA’ = NA$ \frac{25}{2.5}$ = NA \* 10N’A =3×1016 cm-3 |

 These parameters are given in Reference 1, Pg 591

Now our task is to scale 0.25μm to 0.025 μm FET

|  |  |  |
| --- | --- | --- |
| 0.25 μm channel length L FET | 0.025 μm channel length L’ FET  | Scaling factor |
| L = 0.25 μm Tox = 5 nmVDD = 1.0 VVTH = 0.25 VNA  = 3 \* $10^{16}$cm-3. | L’ = 0.025 μm Tox’=$^{5}/\_{10}$ =0.5 nm = 5ÅVDD’= 0.25V (given). VDD’= 4\* VTH’VTH’= 4 VTH’=4\*0.015 = 0.06Vk = VDD/ VDD’= 1.0/0.25 = 4NA’ = NA/(1/= 2/k= 100/4=25.NA’= 3\*1016 \*25 = 7.5\*1017 cm-3.  | L’=$^{ L}/\_{λ,}λ=$ $0.25⁄0.025 $= 10VDD’=$^{ V\_{DD}}/\_{k,}$ $k=$ $^{ 1.0}/\_{0.25} $= 4k =4NA’ = 3 \* $10^{16}$\*$\frac{10^{2}}{4}$= 7.5\* $10^{17}cm^{-3}$ |

**Certain issues following scaling:**

1. Oxide thickness in 0.25 μm ≈ 50 - 60 $A^{o}$

 Tox’ in 0.025 μm ≈ 5 $A^{o}$ is too small and permits tunneling.

 2. Tunneling from source to drain when L’ = 25nm and lower.

3. ID \* ( R S + RD ) voltage drop is < 1 mV.

**Q.6 (c)** Generalized scaling (GS, Table IV) is better than constant electric field (CE) scaling (Table–II) and constant voltage (CV) and Quasi constant voltage (QCV) in (Table-III) as it permits different scaling for voltages/ potential, dimensions (L,W,Tox ) and doping. GS is based on preserving Poisson’s equation. GS gives relationship forNA’ andND’ with NA and ND multiplied by 1/δ.

**Constant electric (CE) field scaling:** All dimensions, voltages are divided by k (or scaling factor). Doping levels are multiplied by k.

**Quasi Constant Voltage (QCV) Scaling:** All dimensions are divided by k (or scaling factor). Doping levels are multiplied by k. The voltages are divided by (1/k)1/2 which is less than k.

**Constant Voltage (CV) Scaling:** All dimensions are divided by k (or scaling factor). Doping levels are multiplied by k. The voltages are not changed.

**Most difficult parameters are:**

(i) Gate Insulator. Solution is to increase Tox‘= 5 $A^{o}$ by using HfO2  which has a higher dielectric constant ɛHf O2 ≈ 13.7 and dielectric constant for SiO2 is 3.9.

Tox’for HfO2 as gate insulator is = $\frac{ɛ HfO2}{ɛ SiO2}$ \* Tox’(SiO2),

= $\frac{13.7}{3.9}$ \* 5 $A^{o}$ = 17.5 $A^{o}$= 1.75 nm

Eg  for Hf O2  = 5.7 eV and electron affinity qHf O2  = (2.0 ± 0.25 ) eV

The other parameter is the voltage drop in R S + RD

(ii) Source and Drain resistances and voltage drops for a 25nm FET are calculated below.



L=22nm

Xj for 0.25 µm FET (Baccarani et al Table II) Ls= 22nm (contact) +11nm +11nm=44nm

 = 0.07 – 0.14 µm RS = RD  =ρn\* $\frac{Ls}{X\_{j \*W}}$

Xj’ for 0.025 µm NanoFET For $10^{20}$ n+ doping the resistivity s is

 =$\frac{ 0.07}{10}$ 🡪 $\frac{0.14 µm }{10}$ ρs  = 7 \* $10^{-4}$Ω-cm. Given W=44nm,

 = 0.007 µm 🡪0.014 µm RS = RD  =$\frac{7 \* 10^{-4}\*44 nm}{0.007 \* 10^{-4} \*44 nm}$

 = 7 nm 🡪 14 nm = 1.0 kΩ

 If the drain current is I D ≈ 1mA or 0.1 mA. Taking 0.1mA or 100 microamp, we get

 I D \* (R S + RD) ≈ 0. 2V =200mV, which is too high.

**How can we reduce RS and RD ?**

Method # 1 Increase the thickness Xj of source or source contact Tsource above the implanted

14 nm region.



New source resistance RS’ = Rs \*[Xj/(Xj + Tsource]  = $\frac{7 \* 10^{-7}}{154 \* 10^{-7} }$\*1.0 kΩ = 45.45Ω

The new IRs’ drop is

I \*RS’= 100 µA \* 45.45Ω = 4.5mV.This value is still higher than 1mV.

Method 2: (a) Increase W of the channel, and (b) further increase thickness of source TSource. Both are not desirable as they increase the area of FET (option a) and make processing difficult when using masks or metal contacts (option b).

Method 3. Use metal silicides for vertical extensions in place of n+ Si which have reduced resistivity.

What is done is to replace Tsource contact with lower resistivity silicides or TiN or TaN.

RS (with silicides) is reduced by a factor of 10. The new drop is 0.45mV.

Reduce RS  from45.4Ω to approximately 4.5 Ω.