**ECE 4243-6243 Quiz 2 Part-B NanoFET 11/16/16 due in two weeks Name\_\_\_\_\_\_\_\_\_\_\_\_\_**

Use HW11 Q6 as a Hint SET

Q.1(a) Outline the steps used in scaling a FET from 0.25 micron to 0.025 microns.

 Baccarani et al (1984 paper distributed in class November 16) describes scaling of 1.3 micron to 0.25 micron. Table I shows scaling to 0.25 microns.

**(b)** **OUTLINE**: Scaling down of a 0.25 micron (m) FET to design 0.025 micron (25nm) transistor requires 10-fold ( =10) reduction in length L (L’=L/10), width W, thicknesses tox, junction depth of source and drain Xj. In HW11 we provided VTH = 0.015V for 25 nm process. This enables to find voltage scaling factor k.

We used the relationship V’TH 4xV’TH and VTH = ¼ \* VDD. This gave us a value of VDD = 0.24V. Comparing VDD for 0.25 micron FET, we get a value of κ~4.

Knowing κ and  we can find . This gives us new substrate doping N’A = NA x λ2/κ.

Finally, we obtain gate oxide thickness, Si doping levels, source and drain thicknesses (Xj) and other parameters such as oxide capacitance per unit area Cox, channel drain current I, source and drain resistances Rs and RD, and delay or RC time constant(see Table 1 of Baccarini et al.).



**Question (b)** Justify the values of various parameters given for 25nm or 0.025 micron FET in Table I (below, HW Table 1)

***It may be confusing to call both tables as Table 1. We will distinguish by calling them Baccarani table 1 and HW Table 1.***

**Home Work Table I 25nm FET design**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameters** | **LATV****1.3micron** | **0.25 micron QMDT\* (IBM)** | **25nm SiGe** **(Home work)** | **Scaling** **factor** | **Comments** |
| Channel Length L(μm) | 1.3 | 0.25 | 0.025 | λ=10 |  |
| Gate InsulatorOxide tox (nm) | 25 | 5.0 (SiO2) | 0.5 (SiO2) | 10 | 0.5(HfO2 /SiO2)= 1.7nm |
| Junction Depth xj(nm) | 350 | 70-140 | 7-14 | 10 | Gives high Rs and Rd  |
| VTH (V)VTH 4xVTH | 0.6 | 0.25V’TH 4xV’TH V’TH =0.06 | 0.06V’TH 4xV’TH V’TH =0.015 | κ=4 | VTH=0.015V |
| VDS = VDD (V)VDD = 4 x VTH | 2.5 | 1.0 | 0.25 | κ=4 |  |
| Band Bending (V) | 1.8 | 0.8 | 0.3 | ? |  |
| Doping NA (cm-3) | 3x1015 | NA =3×1016 | N’A=7.5×1017 | NA x λ2/κ=25 |  |
| (Rs + Rd)IDIR Drop (mV) | NA | < 10mV | < 1mV | ?? | How to solve this |
| RC Delay  (ps) | Not appl. (NA) | 100ps | 2-5 ps?? | ?? | How to solve this |

 Source and drain resistances RS and RD are function of junction depth Xj and source and drain length and width. Knowing the resistivity of the source and drain region, we can calculate the resistance of the source and drain regions.

**Question (c1)** Summarize in few lines constant electric field (CE), constant voltage (CV), Quasi constant voltage (QCV).

Put the values of various parameters for CE, CV, QCV schemes for scaling a 0.25 micron FET to 0.025 micron.

**Question (c2)** them with Generalized Scaling (GS) schemes. Enter their values.

Table 2 Comparison of CE, CV, QCV and GS (take parameters from Table 1 HW11 above)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Scaled down Parameters  | CE | CV | QCV | GS |
| Channel Length L |  |  |  |  |
| Gate oxide Tox |  |  |  |  |
| VTH |  |  |  |  |
| Substrate doping NA |  |  |  |  |

**Question (d)** what do you think are the most difficult parameters to scale in the design of 25nm channel length FET? **Name them with your reasoning**.

Q.(e) Outline the steps to scale a 0.025 micron (25 nm) FET to 12.5nm (or 0.0125 micron).

Enter your parameters in Table 3.

Table 3 12.5 nm FET parameters of your design

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameters** | **25nm SiGe** **(Home work 11)** | **12.5 nm FET****(Quiz 2-Pt/B** | **Scaling** **factor** | **Comments** |
| Channel Length L(μm) | 0.025 |  | λ= |  |
| Gate InsulatorOxide tox (nm) | 0.5 (SiO2) |  |  |  |
| Junction Depth xj(nm) | 7-14 |  |  |  |
| VTH (V)VTH 4xVTH | 0.06V’TH 4xV’TH V’TH =0.015 |  | κ= |  |
| VDS = VDD (V)VDD = 4 x VTH | 0.25 |  | κ= |  |
| Band Bending (V) | 0.3 |  | ? |  |
| Doping NA (cm-3) | N’A=7.5×1017 |  | 1/=λ2/κ= |  |
| (Rs + Rd)IDIR Drop (mV) | < 1mV |  | < | How to solve this |
| RC Delay  (ps) | 2-5 ps?? |  | ?? | How to solve this |