Laboratory Experiment:
Diffusion of n- and p-type impurity in Silicon Wafer.

Week # 1

(1) **Predeposition using Boron Nitride (BN) source:** Perform a shallow diffusion for about 5 min (two wafers), 10 min (two wafers), and 30 min (three wafers) at 975 °C using BN source and n-Si wafers.

(2) Determine the extent of diffusion (or junction depth) by angle lapping and staining technique; verify the junction depth against the theoretical estimates (for this part of your experiment cut a little portion of your sample using a diamond tipped scribing tool or the wire saw).

(3) Take one wafer each of 5 min, 10 min, and 30 min samples and acid etch their back side to remove any boron doped layer; evaporate contact metal and appropriately alloy it to form ohmic contact. (Vacuum evaporation will be done for you; you should leave your samples clearly marked after the lab period).

Week # 2

(4) Obtain V-I and C-V characteristics under dark and illuminated conditions (photovoltaic effect) on metalized p-n samples.

(5) **Drive-in diffusion of boron:** Perform drive-in diffusion on 10 min and 30 min boron-predeposited wafers at 1150-1175 °C in nitrogen or nitrogen + oxygen ambient; for 30 min wafers perform a 2 hr and 3 or 4 hr diffusions, respectively.

(6) Back etch wafers after drive-in diffusion. Leave the wafers for vacuum evaporation and annealing to form ohmic contacts.

(7) Angle lap (part of sample) and stain to find junction depth in drive-in samples; compare experimental and theoretical results (if time permits).

Week # 3

(8) Measure V-I and C-V characteristics on drive-in p+-n diodes under dark and illuminated conditions.

(9) **Predeposition of phosphorous:** Perform phosphorous predeposition (5 min, 10 min) on p-type Si wafers using phosphoryl chloride (POCl₃) or doped-oxide source; repeat steps (3) and (4). (See the attached sheet for phosphorous processing).
Supplement Notes

Drive in Diffusion

\[ \frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2} \]

Boundary conditions are:

1) \( N(\infty, t) = 0 \)

2) \( D \frac{\partial N}{\partial x} (0, t) = D \frac{\partial N}{\partial x} (\infty, t) = 0 \)

Initial Condition

3) \( N(x, 0) = t_p \quad t=0 \) is used to obtain the profile for \( t = t_p \) (predeposition)

Delta functions approx.

\[ \int N(x, t_p) dx \equiv \lim_{\Delta \to 0} \frac{Q_A}{A} (t_p) \delta(x) \]

The solution of the diffusion equation using the two boundary conditions and an initial condition (3)

\[ N(x, t) = (4\pi D t)^{1/2} \int_0^\infty N(x', t_p) \left[ e^{-\frac{(x-x')^2}{4D t}} + e^{-\frac{(x+x')^2}{4D t}} \right] dx' \]
Using the δ function approximation, we get

\[
N(x,t_d) = \left[ \frac{Q_A(t_p)/A}{\sqrt{\pi D_d T_d}} \right] \cdot e^{-\frac{x^2}{4D_d t_d}}
\]

Let \(1 - \text{erf}(z) = \text{erfc}(z) = \) [Complementary error function]. Equation 8 can be rewritten as

\[
1 - \text{erf}\left( \frac{x_j}{2\sqrt{D_p t_p}} \right) = \text{erfc}\left( \frac{x_j}{2\sqrt{D_p t_p}} \right) = \frac{N_B}{N_O}
\]  

--------- (9)

In equation (9), we know \(N_B (= \text{donor concentration in n-side). And } N_O, D_p \) is computer from table, and \(t_p \) is known. Now \(x_j \) can be calculated.

We can also determine the total number of acceptor (boron) atoms \(Q_A(t_p) \) introduced during the time \(t_p \).

\[
Q_A(t_p) = A \int_0^\infty N_o \text{erfc}\left( \frac{x}{2\sqrt{D_p t_p}} \right) dx
\]  

--------- (10)

\[
Q_A(t_p)/A = \frac{2N_o}{\sqrt{\pi}} \cdot \sqrt{D_p t_p}
\]  

--------- (11)

Here, A is the surface area. [Note that \(Q_A(t_p) = \text{area under plot } t_p \)]

**Diffusion from limited sources:**

The impurities diffused predisposition (using infinite or semi-infinite sources) can be further driven into the substrate by heating it at higher temperature for a long duration \(t_d \). Since the redistribution reduces the impurity concentration, the diffusion coefficient during drive-in \(D_d \) is usually smaller than the predispositions \(D_p \).

These are several approximations which are used to simulate the process of drive-in for instance; a delta-function approximation is the easiest to work with mathematically. In this case all the impurities [i.e. \(Q_A(t_p) \)] are assumed to be confined at the surface in the form of delta function \(\delta Q_A(t_p) \).

The solution of diffusion equation (6) in this case is of the form:

\[
N(x,t_d) = \left[ \frac{Q_A(t_p)/A}{\sqrt{\pi D_d T_d}} \right] \cdot e^{-\frac{x^2}{4D_d t_d}}
\]  

--------- (12)
Equation (11) and (12) give

\[
N(x, t_d) = \frac{2N_0}{\pi} \cdot \frac{D_p t_p}{D_d t_d} \cdot e^{-\frac{x^2}{4D_d t_d}}
\]

However, the profile of impurities can be represented more precisely if the distribution during predeposition is approximated by a concentration step (i.e. a pulse function with pulse width \(x_h\) and pulse height \(N_0\)). Now \(Q_d(t_p) = N_0 x_h\).

The solution of the diffusion equation in this case is (Reference: Howard and Hamilton, pp.40-41)

\[
N(x, t_d) = \frac{N_0}{2} \left[ \text{erf} \left( \frac{x - x_n}{2\sqrt{D_d t_d}} \right) - \text{erf} \left( \frac{x + x_n}{2\sqrt{D_d t_d}} \right) \right]
\]

The figure 11 shows plot of \(\sqrt{D}\) as a function of diffusion temperature for phosphorus and boron in silicon. The solid solubilities of various impurities are given in figure 12.
Carrier Concentration ($cm^{-3}$) versus depth ($\mu$m) in a silicon wafer.
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Reference: Semiconductor Technology Handbook (Trapp et al)

Figure 11. $\sqrt{D}$ vs. Diffusion temperature

Figure 11. Diffusion Coefficient as a function of temperature.
PDS® System

PDS® Phosphorus wafers offer users low cost, in-situ n-type planar sources for silicon diffusions. In-situ PDS sources eliminate the trade off between throughput and uniformity for larger diameter wafers. PH-1025 consists of an active component silicon pyrophosphate (SiP₂O₇) carried on and in an inert substrate. PH-1025 is generally used for sheet resistivities between 2.5 Ω/cm and 2.5 Ω/cm in emitter, collector, polysilicon doping, source/drain, solar cell and other applications.

At diffusion temperatures, the active component, SiP₂O₇, decomposes to form the desired dopant species, P₂O₅ vapor, that evolves from the source by direct volatilization. No corrosive or toxic materials are involved since the side product is SiO₂, which remains on the source wafer.

\[
\text{SiP}_2\text{O}_7 \xrightarrow{\text{Heat}} \text{SiO}_2 + 3\text{P}_2\text{O}_5
\]

In the PDS system, source and silicon wafers are edge-stack in a perpendicular to the tube axis in cross slotted furnace carriers, as shown in Figure 1. Typical loading of the furnace carrier begins with a source wafer followed by two silicon wafers back-to-back followed by another source wafer, etc., ending with a final source wafer at the opposite end of the carrier. This allows most of the source wafers to dope 2 silicon wafers. Source wafers are typically spaced 0.100" to 0.125" (center to center) from the silicon and the back-to-back silicon wafers are usually 0.060" to 0.080" (center to center).

Furnace carriers of quartz, polysilicon and silicon carbide are all used with the PDS system. Those with the lowest thermal masses usually produce the best results.

During the evaluation phase of PDS sources, a full load of dummy silicon wafers is needed to create the boundary layer condition and achieve meaningful results. Typical nitrogen flow rates are 6.0 slpm for 125mm wafers, 4.0 slpm for 100mm wafers, and 2.5 slpm for 5" wafers. Optimization of across the wafer and across the boat diffusion parameter uniformity may require that these flow rates be modified.

A tight fitting end cap or plate should be used on the furnace (see Figure 2, A & B). To achieve good uniformity in all furnace processes, the tube and boat should be centered so they are concentric with the furnace calls. Often, by centering the wafers, the temperature gradient across the wafers is minimized, allowing more uniform diffusion and oxidation. This compact stacking arrangement allows increased furnace utilization.

PDS wafers can be used with automated wafer transfer systems, which help to increase yields.
Wafer Preparation
Wet chemical cleaning of 1H-1025 wafers is unnecessary since they are manufactured under the most exacting quality standards, using raw materials of the highest purity, and are protected from exposure to contaminants both during and after manufacture. Another consideration is that due to the porosity of the composition, cleaning agents are difficult to remove completely.

It is recommended that prior to actual silicon diffusion, new wafers be annealed at 1000-1025°C for four hours. Lower temperatures may require a longer anneal time.

Storage
Wafers should be stored between uses in dry nitrogen at 100-250°C. If wafers have been stored without use for an extended period of time (one week or more), at least a one hour anneal at use temperature is recommended prior to silicon diffusion.

Furnace Loading and Unloading Cycles
For 100mm and larger sizes a slow push (typically 5.0"/min) at 700-850°C is advised. The boats should be allowed to equilibrate for 5-10 minutes under N₂ before ramping to use temperature. A subsequent ramp down to 700-850°C is also recommended. Smaller sizes do not require push/pull or ramping.

Product Performance
Testing indicates that performance should be maintained for at least 100 hours at maximum temperature. At lower temperatures, lifetime is expected to increase.

All testing was performed on 100 p-type silicon of 6-17 ohm-cm resistivity using a quartz boat with 0.100" between source and silicon wafers (center to center). The loaded boat was pushed in at 800°C, then ramped to set temperature at a rate of 10°C/min where it was held for the predetermined time. Ramp down was at 5°C/min to 800°C.

Advantages of the PDS System are:
— Control of sheet resistance within ±1% across individual silicon wafers and within ±2% across the flat zone.
— No capital expense to convert from carrier gas systems.
— eliminates problems of flow stream turbulence, positional and size dependence of silicon wafers.
— Increased stacking density and furnace throughput.
— No damage or safety hazards from corrosive and toxic off-gases.
— Simplified process control. Elimination of controllers, valves, regulators and attendant maintenance problems.
— Reduced risk of operator error.
— No "sticky" furnace tubes; reduced rate of tube devitrification. Lower downtime losses, costs of tube deglazing and replacement.
— Compatible with automated wafer transfer systems.
Device Probing Station: 
**V-I characteristics for diodes, bipolar and field-effect transistors**

The wafer with devices under test is mounted on the chuck and is held by vacuum. The probes can contact ~25x25 μm² pads on the device. For example, in a FET we need gate, source, drain, and body contacts. Body contact is obtained from the vacuum chuck. The other contacts Probes are wired to an interface box, which is in turn connected to the Parametric Analyzer.

![Probing station showing microscope/CCD camera with probes (Signatone) connected to a box (on the right) interfacing with the Hewlett Packard Parametric Analyzer.](image)

Fig. 1. Probing station showing microscope/CCD camera with probes (Signatone) connected to a box (on the right) interfacing with the Hewlett Packard Parametric Analyzer.

Figures 2 and 3 show the details on the box. The box has four connections SMU1 to SMU4. Each of these has a guard ring GD1-GD4. Table below shows the connections for various devices. The details are on the next sheet.

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Table showing connections
Fig. 4. Hewlett-Packard 4145B Parametric Analyzer

We select Option 1 from the main menu (second soft key next the screen). It brings up channel (of the test box) definition screen. We select device configuration (e.g. diode V-I, FET, or BJT). Other details will be provided.

Drain
SMU2

Gate
SMU3

Source
SMU1

HP Parametric analyzer connections for a MOSFET testing
HP Parametric analyzer connections for a BJT testing

HP Parametric analyzer connections for a diode testing
You may have to perform V-I and C-V measurements during the next lab period.

Equipment: Diffusion furnaces for Boron and Phosphorous diffusions, junction determination setup using angle lapping and staining technique, metal contact evaporation (to be done for the group), V-I, C-V measurement setup for electrical characterization under dark and illuminated (solar cell mode) solutions.

Laboratory report on the diffusion experiment should include:

1. Theoretical computation of junction depth $x_j$ for at least one wafer which has undergone drive-in diffusion.

2. Experimental verification of the junction depth (only if the staining part has completed successfully).

3. (a). Comparison of theoretical V-I characteristics against experimental plots, under dark conditions (two devices: one with drive-in diffusion and the other with predeposition).
   
   (b). Determine ideality factor $n$ by fitting your data to $I = I_b (e^{\frac{qV_f}{kT}} - 1)$.

4. Compute substrate doping concentration and built in voltage $V_0$ from the $\frac{1}{C^2}$ Versus V data (one device only). Compare theory and experiment using built in voltage.

5. Compare solar cell parameters against theoretically expected values.

6. Discussion/remarks.

**Diffusion Experiment:**

Familiarity with the following techniques and instruments is essential.

1. Philtec Groover/Sectioner – staining technique pp. 137-140
2. Mesa etch pp.141
3. Back etch pp. 142
4. Dark V-I measurements: HP Parameteric Analyzer pp. 143
5. C-V setup (see SiO₂ setup)  

6. Solar Cell setup (use a probe station)  

**Parametric Analyzer**  
(Instrument used: HP 4145B)

**Procedure to do:**

1. V-I Characteristics of  
   a. BJT's  
   b. MOSFET's  

2. Get Print out  

3. V-I Characteristics of LEDs  

4. V-I Characteristics of SCRs  

Example: Diode I-V Characteristics.
The schematic of a diffusion setup is shown in Fig. 1. It consists of a three-zone furnace, a quartz tube, and a substrate/wafer holder. The quartz tube is purged with high purity nitrogen to maintain impurity free ambient.

Figure 1. Schematic of Diffusion Furnace Setup.
In-lab Procedures

A. Predeposition and Drive-in diffusion

Predeposition is done using boron nitride wafers as the source material. Clean n-Si wafers (for cleaning the procedure is described elsewhere) are loaded in a quartz boat in a manner shown in Figure 2. Precaution should be taken to keep the separation between BN and Si wafers as uniform as possible. The loaded boat is transported into the furnace (with the help of a quartz rod) first in a relatively lower temperature zone (500°-750 °C) to avoid thermal shock. After a period of about 5 minutes the wafers should be transported to the right temperature zone. The temperature and duration of diffusion is determined by the amount of impurities needed to be diffused in Si wafers. The surface concentration is also important as it is related to the solid-solubility of a particular impurity in silicon at a given temperature.

![Figure 2. Boron Nitride and Silicon Wafers arranged in a quartz boat.](image)

Once the diffusion is completed the boat can be pulled out. The process of pulling can again be divided into two stages (1) pulling the boat in the 500-750 °C zone and letting it cool for 5 minutes or so, and (2) moving the boat in the region maintained at room temperature.

The drive-in diffusion is done in a separate quartz tube (as the tube used for predeposition starts acting as a dopant source after a number of runs).

In contrast to predeposition, the drive-in diffusion is generally performed to obtain: (1) deeper junction depths. (2) lower surface concentration (see Eq. 11 in the Section on Theory). A lower surface concentration than obtained by predeposition (limited by solid solubility only) is desired when an additional diffusion of opposite type of impurities is desired such as in the case of n-p-n transistors.

Drive-in diffusion is often carried out in an oxidizing ambient. This procedure results in the growth of an oxide layer in addition to the desired diffusion. The grown SiO₂ layer is used as a mask for subsequent processing steps generally needed in the fabrication of ICs.
Phosphorus Diffusion Using Doped-Oxide Sources

We have discussed the diffusion of impurities from solid sources available in the form of wafers (e.g., BN). Dopants can be introduced by sources in liquid form such as POCl₃ and BBr₃ and gaseous form such as PH₃, AsH₃, and B₂H₆. In addition, doped oxides are also used as sources of both p- and n-type impurities. We will perform phosphorus diffusion using a doped-oxide source. The process is described next.

Phosphorus diffusion using doped-oxide sources

Process:

1. Spin on the emulsion at about 3000 r.p.m for 15 seconds.
2. Prebake the spin-on coating at 150 °C for about 30 minutes (This can be done by keeping the wafers at the mouth of the diffusion furnace.).
3. Perform the diffusion at 1150 °C for 5, 10 or longer duration (in minutes).

Diffused wafers should be back-etched in a silicon etch for about 5 minutes (depending on the potency of the etchants) to remove any phosphorus diffusion. Back etching can be done by wax-mounting the wafers on the quartz slide. Before removing the wafer from the quartz slide, check the conductivity type of the silicon surface to ensure the complete removal of the phosphorus diffusion. A thermoelectric probe may be used for this purpose.

Front surface treatment:

1. Strip the SiO₂ layer by soaking the wafers in buffered HF or diluted HF (5%).
2. Check the complete removal of the SiO₂ film by the thermoelectric probe.

The wafers are now ready for metallization.

Phosphorus Diffusion in p-Si Wafers Using SiP₂O₇ Solid Source

Loading Procedure:

(1) Load the Si wafers in the quartz carrier/boat (try to maintain the separation between source wafers and Si wafers to be about 0.1).

(2) Slide the wafers about 3-4" inside the furnace (using the metal place at the end of the furnace as the reference), and wait for about 5 minutes for preheating.

(3) Push the wafer carrier to the middle of the furnace.

Diffusion: Perform 15-20 minute diffusion (see the attached chart for the junction depth information).
Wafer Pull-Out:

(1) Pull the wafer carrier out to with in 2-3" of the furnace (metal end plate), and allow the wafers to cool for 5-10 minutes.

(2) Pull all the way out in the tapered end joint.

(3) Store the wafers in a glass petri dish.

Etching Procedure:

(1) Since the decomposition of SiP$_2$O$_7$ results in P$_2$O$_7$ formation, the front side of all the wafers should be treated with 10% HF. (Soak the wafers in 10% HF for about 5 minutes without mounting them on quartz slides, and test their conductivity using a thermoelectric probe).

(2) Back-etch wafers, using the standard procedure in Si etch.

B. Angle-Lapping and Staining

The principle behind this method is: (1) to expose the p-n junction by physically removing the p layer from a part of the sample; (2) to use photochemical techniques to delineate p-layer from the n-region. In the presence of light, the reactivity of certain chemicals with Si is dependent on the type of carriers presents (surface photovoltage generated). The jug used for angle lapping is shown in Fig. 3a. It consists of a stainless steel cylindrical block with one face having a 1-3° angle. The sample is mounted on this face, and then polished on a flat surface. The angle-lapped sample is shown in Fig. 3b.

![Figure 3(a) Cross section of an angle-lapping jig.](image)

![Figure 3(b) Angle-lapping sample (cross section).](image)
After lapping the sample is removed from the stainless steel block, and it is mounted on a quartz slide (with angle-lapped side facing up). A drop of the staining chemical is placed on the lapped region to delineate n-layer from the p-type region. The sample is now exposed to tungsten light (ultraviolet source is preferred in some cases) for about 1-3 minutes depending on the intensity used. The staining chemical is washed off, and the stain is observed under an optical microscope. If the stain does not appear, the entire process is repeated. The stain develops either on the n-layer or the p-layer preferentially. This depends on the nature of the chemical used.

* In the laboratory we will be using an automatic sectioner which has a spindle for cutting grooves. Upon staining, we can determine the junction depth.

The sample is now ready for the evaluation of the junction depth. An estimate of the width of the stained region can be made with the help of an optical microscope having a graduated eyepiece. Once the width $d$ and angle $\theta$ are known the junction depth $x_0$ can be computed.

**Junction Depth Measurements:**

1: Philtec Sectioner operating instruction (will be given in the lab) for cutting a groove.

2: Selection of strain
   After the stain is applied, wait for 10-40 seconds under the microscope with illuminator on. (see page 137 under instructions).

3: Determine the junction depth;
   T-Stain marks n-Si Layer Darker than p-Si
   A: Measure $W_1$ & $W_2$ (see pages 138-139)
   B: One of the microscopes has an eyepiece with the scale. Each division of this scale is a millimeter. To get the actual $W_1$, divide the number of divisions by the magnification of the objective lens.
   C: Instructions to use $W_1$ and $W_2$ information in order to get junction depth are given on pages 138-140.

The rest is off the Page...
DESCRIPTION

Stains consisting primarily of metal salts in an electrolyte which have been used extensively to stain the more n-type regions in silicon. This characteristic holds consistent with p on p⁺ being darkened. Repeatable results are achieved by control of light intensity and staining time. Five compositions are available to permit selection of the most appropriate stain.

Overstained regions often require no refinishing, they are merely wiped with a dampened paper towel and restained. The chemical composition of this stain does not necessitate extraordinary safety precautions during its use. Minimal experience and technique are needed to stain junctions with Philtec Safe-T-Stain because a unique stain composition is available for most junction impurity concentration ranges.

Note: For applications where wafers will be going through further diffusions, the stain can be removed by using Ammonium Persulfate (NH₄)₂S₂O₇.

FEATURES

- Greatly reduces staining operation hazards to the operator.
- Sharply and rapidly delineates diffused and epitaxial layers in materials with a wide variety of deposits, concentrations, and layer depths.
- Eliminates the need for a fume hood, and does not corrode surrounding equipment.
- Does not etch out layers to be measured, most noticeable when measuring thin layers.
- Minimally affects oxide on the surface of a wafer when it is present.
- Enables observation of the staining through a microscope while it is taking place, without damaging the optics.
Measurement of Denuded Zones in Silicon

This measurement is of significance when evaluating the effects of oxygen precipitation on device yields. For this test application the following factors must be controlled:

- the exposed surface of the layer must have a strain free surface finish,
- the etch or stain applied to the exposed layer must display the true nature of the material,
- the measurement instrument must be able to accurately measure the depth of the defect.

Etches commonly used to display the precipitated sites are Sirtyl, Wright, and Seeco (Philetic has a Wright etch, Kit # 1 SNZ-W). The resultant appearance of a denuded wafer is an accumulation of etch pits towards the bottom of the groove and a clear (denuded) layer close to the surface. (See photo)

![Image of etch pits and denuded layer]

The Philetic Arcuc method of layer measurement is used to measure denuded zone depth. A measurement is made of the total groove width ($W_1$); then a second measurement is made across the groove at the point where the etch pits disappear ($W_2$). These measurements are made with a calibrated microscope at 50X and 100X. Philetic supplies an optional, specially fixtured, microscope. These two measurements are easily converted to depths ($d_1$ and $d_2$). Philetic supplies conversion charts or optional calculator and digital filar measurement systems. The difference between $d_1$ and $d_2$ is the thickness of the denuded zone. Typical dimensions are shown in Figure 2.

![Diagram showing measurements]

$W_1 = 750 \mu m \Rightarrow d_1 = 3.497 \mu m$

$W_2 = 400 \mu m \Rightarrow d_2 = 0.947 \mu m$

Junction Depth $t_j = 2.559 \mu m$

WHEN ORDERING - Specify the model of your 2015 Sectioner, and the approximate depth of the layer to be measured, in order to get the correct type of spindles. The kit contains two spindles, polishing solution and supplies sufficient for more than 1000 tests.

FOR FURTHER INFORMATION CALL:

Philetic
INSTRUMENT COMPANY

SYSTEMS FOR MICRO-ANALYSIS

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5.2.3. Turn to the Depth index in the instruction manual. Look up the recorded $w_1$ measurement in the width column of the Index, the record the adjacent number from the depth column ($d_1$).

5.2.4. Look up the recorded $w_2$ measurement. Record the corresponding number ($d_2$) directly under the first recorded depth column number.

6.0 Junction Depth Measurement on Patterned Wafers (not applicable)

6.1 Determining junction depths on patterned wafers can be hampered by not knowing when the groove is through the pattern junction. To eliminate this from occurring, load the wafer in the chuck with the device patterns at an angle to the chuck opening (see Fig. G6.1). A side view is shown in the same figure. Notice that the groove reaches below the pattern, and the pattern edge becomes parallel to the groove's axis in Fig. G6.2. This is interpreted as the junction depth.
5.0 Junction Depth Measurement Using Depth Index

5.1 Discussion of Concept

To understand the basic concept, it will be assumed that dopant material is uniformly diffused into the top surface of a substrate. Assume that after staining to expose the layer, two dark bands appear at the top edges of the groove. The substrate region will remain uncolored.

5.2 Instructions for Measuring Junction Depth Using Depth Index

5.2.1 Measure perpendicular to the groove length from one upper edge of the groove across to the other \( w_1 \) as in Fig. G5.1, and record the measurement on paper.

5.2.2. Without changing location along the axis of the groove, measure the distances between the two stained junctions \( w_2 \) as in Fig. G5.1, and record that measurement under the \( w_1 \) measurement.

NOTE: To simplify measuring with a reticle eyepiece, one side of the groove may be aligned with zero. When measuring \( w_2 \) the edge of the junction can be moved to zero as long as measurement is only perpendicular to the groove axis.

\[ W_1 = 750 \mu \Rightarrow d_1 = 3.497 \mu \]
\[ W_2 = 400 \mu \Rightarrow d_2 = 0.947 \mu \]

Junction Depth \( x_j = 2.550 \mu \)
C. Ohmic Contacts and Mesa Structure Formation.

The diffusion of impurities is followed by metallization and ohmic contact formation. This enables attaching leads to perform electronic measurements on the devices (e.g. p+n, n+p diodes). Since the impurities diffuse in Si from both exposed faces of the wafers, the diffusion process results in the formation of p-n-p structures on n-type wafers (see Fig.4). We should etch p-layers from the back of the wafer to obtain p-n device structures.

![Diagram](image)

Figure 4. (a) Sample before Diffusion (Width polished side up)  
(b) Sample after Diffusion (p-type)  
(c) Sample after back etch of p-Si diffused Layer.

The wafers are next loaded in a vacuum evaporation/sputtering system to deposit thin films of metals which form nonrectifying/ohmic contacts on nSi and pSi, respectively. For instance, Al is deposited (1000-2000 Å) on pSi to form ohmic contacts. Evaporation is followed by heat treatment under controlled ambient to form a eutectic of Al and Si to ensure low-resistance contacts. The substrate side of the wafer is generally metallized completely. The front surface (in the present case) is pSi and it is deposited with Al to form ohmic contacts. The pattern in which aluminum is deposited depends on the device structure desired. We will deposit Al through a metal mask which allows a dot pattern. The nSi side is evaporated with Au-As or Au-Sb layers. Gold forms a eutectic with Si at about 420 °C, and the As or Sb act as n-type dopants creating an n⁺-region wherever gold diffuses in nSi. The formation of ohmic contacts is followed by device testing. Since all the diodes are connected by a common p-type top layer, the individual devices must be separated from each other. This can be achieved by scribing and separating the individual dices (or chips). This process is schematically shown in Figure 5.

![Diagram](image)

Figure 5. Dicing and Mesa Formation
In Fig. 5(a) shows a Si wafer with both sides metalized. An individual dice, separated from the wafer in Fig. 5(a), is sketched in Fig. 5(b). The process of dicing damages the sides of the dice, and these damages cause a leakage current when the device is biased electrically. However, the damages can be removed by simply etching around the junction. Fig. 5(c) shows the formation of a mesa structure on the front surface. It may be added that a mesa structure can be obtained by selectively masking (with wax, for example) and etching the p-Si layer around the ohmic contact.

**Wafer back-etch procedure following oxidation or diffusion**

**Oxidation**

1. Evaporate the metal gate electrode (e.g. Aluminum).

2. Mount the wafer (front face down) on a quartz slide with the help of the photoresist or paraffin-wax. Care should be exercised in melting the wax and in placing the wafer on it. We do not want the wax to flow over to the surface we want to etch. At the same time we would like to wet the entire face in contact with the wax.

3. Remove any excess wax from the top surface with the help of a cotton swab dipped in hot TCE.

4. Soak the wafer in buffered HF or dilute (5-10%) HF for requisite time to dissolve the SiO₂ layer.

5. Rinse the quartz slide in de-ionized water. Blow dry with N₂ stream.

6. Heat the quartz slide and remove the wafer. Remove the wax in boiling TCE (twice) Use the standard cleaning procedure after this (methanol, isopropyl etc.).

7. Evaporate the contact metal on the back side of the wafer.

8. Heat treatment to form the ohmic contact.

**Diffusion**

9. Follow steps 2-6. Use silicon etch during step 4 in place of HF.

10. Evaporate the contact metal having higher annealing temperature on either the front or back surface as the case may be.

11. Heat treat to form ohmic contacts.
12. Evaporate on the other side and heat treat.

D. Voltage-Current (V-I) and Capacitance-Voltage (C-V) Measurements on p+n, n+p diodes.

D.1. V-I and C-V Characteristics under Dark Conditions

Determine the V-I characteristics using the set-up of Fig. 6. Vary the current (e.g. InA, 2nA, 5nA, 10nA...1mA) and measure the voltage. Determine both forward and reverse V-I characteristics.

![Measurement circuit and Shielded probe station](image)

(a) Measurement circuit  (b) Shielded probe station

Fig. 6. Voltage-current measurement setup.

C-V characteristics can be determined by using the Boonton (72AD) meter. This meter has a provision for applying external bias. The C-V setup is shown in Fig. 7

![Figure 7. C-V Measurement Setup](image)

The reverse C-V plot yields information about carrier concentration (Fig. 8) in the
substrate. For instance, in an abrupt p+n junction.

\[ C_j = A \left[ \frac{q\varepsilon_e\varepsilon_o \cdot N_A N_D}{2(V_O - V) \cdot N_A + N_D} \right]^{1/2} \]

If the nSi substrate is much lightly doped than the p-diffused layer, \( N_A \gg N_D \).

Or \[ \frac{C_j}{A} = \left[ \frac{q\varepsilon_e\varepsilon_o N_D}{2(V_O - V)} \right]^{1/2} \]

Alternatively,

\[ \frac{1}{(C_j/A)^2} = \frac{2V_O}{q\varepsilon_e\varepsilon_o N_D} - \frac{2V}{q\varepsilon_e\varepsilon_o N_D} \]

Note that the slope is \[ -\frac{2}{q\varepsilon_e\varepsilon_o N_D} \]

D.2. V-I and C-V Characteristics with Illumination

A shallow diffused p+n junction behaves as a solar cell when the p⁺ side is illuminated. Fig. 9 shows the test circuit as well as the V-I Characteristics. The V-I plot yields information on the solar-cell performance.

(a) Solar Cell Test Circuit (b) V-I Characteristics with increasing illumination

Figure 9 Solar cell test setup and V-I characteristics

The temperature of the sample should not be allowed to increase during V-I measurements.
E. Theory of diffusion

Dopant impurity such as boron and phosphorus are used to make p-n and n-p junctions on n and p Si substrates, respectively. These impurities are generally introduced by any one of the following three techniques:

- Diffusion
- Epitaxial growth
- Ion implantation

The flux density $J$ of the diffusion species is simple expressed by the Fick’s Law.

$$ J = -D \cdot \nabla N $$

Or

$$ J = -D \frac{\partial N}{\partial x} \quad \text{(in one-dimensional cases)} $$

Here $D$ is the diffusion Coefficient of the impurity, and $N$ is the concentration at a point $x$. Diffusion coefficient is dependent both on the temperature and concentration for the given system. (Generally, the dependence of $D$ on $N$ is ignored. However, it becomes important as the dimensions of the devices become relatively small). Distribution of dopant $N(x,t)$ is determined by solving the Continuity equation.

$$ \frac{\partial N}{\partial t} = -\nabla \cdot J $$

Using the equation 1 & 2

$$ \frac{\partial N}{\partial t} = \nabla \cdot (D \nabla N) = D \nabla^2 N + N \cdot (\nabla \cdot D) $$

if $D$ is assumed to be independent of spatial variation (i.e. $D$ is not a function of $N$)

$$ \frac{\partial N}{\partial t} = D \nabla^2 N $$

Simplifying equation 5 for the one-dimensional case

$$ \frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2} $$

The solution of equation 6 depends on the boundary conditions, and the initial conditions.
**Diffusion from an infinite source: Predeposition.**

An infinite source maintains a constant impurity concentration at the surface of the Si sample all the times. The surface concentration \( N_O \) is

\[ N_O = N(x = 0, t) = \text{Solid solubility of impurity at a given temperature of diffusion.} \]

The other boundary condition being

\[ N(\infty, t) = 0 \]

Initial condition - \( N(x, t = 0) \equiv 0 \)

Under above boundary conditions & initial condition, the solution of Eq. 6 is

\[ N(x, t) = N_O \left[ 1 - \text{erf} \frac{x}{2\sqrt{Dt}} \right] \quad \text{(7)} \]

The table of error function [erf z] is attached at the end of this write-up. \( N_O \) is evaluated using solid-solubility tables. \( D \) is also computed using the \( D \) versus \( T \) plots/tables. Eq. 7 is plotted in Fig. 10.

In the case of a p-type diffusion in nSi (e.g. Boron, Gallium, Indium), the junction will form at \( x = x_j \) when \( N(x_j, t_p) = N_B \). That is, for a diffusion duration of \( t_p \) seconds,

\[ N(x_j, t_p) = N_B = N_O \left( 1 - \text{erf} \frac{x_j}{2\sqrt{D_p t_p}} \right) \quad \text{(8)} \]