Homework 3
Due February 22nd

1. Implement the following logic functions in a single CMOS logic gate. Draw out the entire schematic showing the nMOS and pMOS transistors

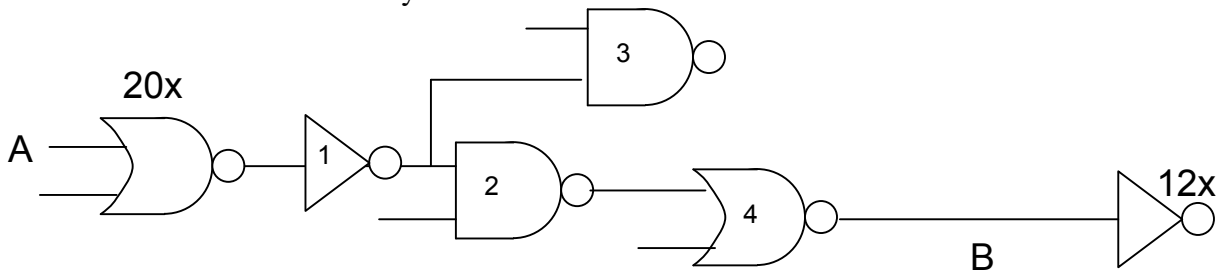
$$Z = \overline{A} + \overline{B} + \overline{C} + \overline{D}$$

$$Z = \overline{AB}\left(\overline{C} + \overline{A}\overline{B}\right) \quad .$$

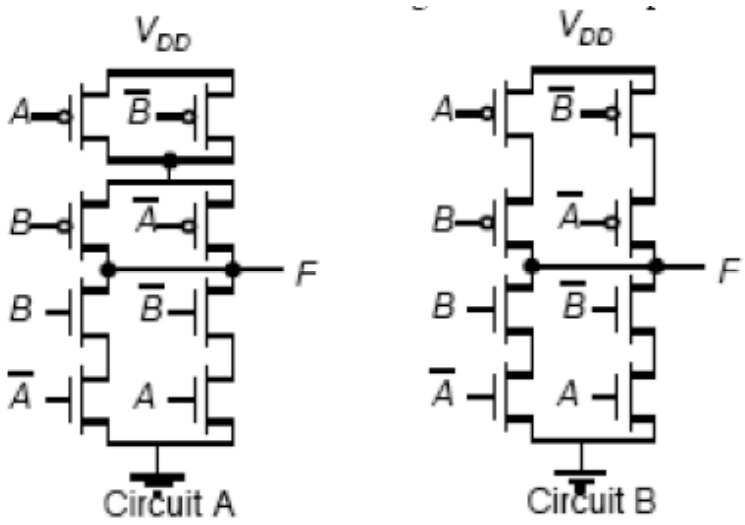
$$Z = \overline{ABC + D}$$

2. Design a 4:1 mux
   a. Using a combination of transmission gates and logic gates
   b. Using only CMOS logic gates
   c. Which is more efficient in terms of transistors used? in terms of delay?

3. Given the following circuit, using logical effort methods, find the optimal sizing for the gates 1,2, and 4 to minimize the path from point A to B. You can assume that gate 3 will be sized by the same factor as gate 2. Also, the input NOR gate has been sized by a factor of 12.



4. a. What functions do the following two circuits implement?



b. Circuit B does not have a dual as the pull-up circuitry. Will this logic gate actually work? Why or Why not?
c. Is there any advantage to the B topology versus A?