# ECE 249 Lab 1

Spring 2005

Adapted from

"Short Tutorial on Cadence", Z. Tao and M. Keramat, UCSN-0300-ZBT-03, March 2000 "Symbol Creation of Sub-Circuits in Cadence," Z. Tao and M. Keramat, UCSN-0700-ZBT-10, July 2000

## Cadence Software Fundamentals

#### 1 Introduction

This lab aims at introducting you to the Cadence software on the Sun workstation. First, a list of basic UNIX commands is given, and then followed by setting the UNIX environment for the Cadence design tools. Finally, a simple example of simulating a CMOS Inverter is presented.

#### 2 Basic Unix Commands

Some basic UNIX commands that you need to know are listed in Table I.

#### Table I. Basic Unix commands

List the files in the current directory:		
Ls	Displays the name of the files in the directo	ory.
ls -l	Displays additional information (eg. permis about the files in the directory.	sions)
ls -a	Displays all files in the directory, including hidden files.	
ls -al	Combines the previous two options.	
Change (or move between) directories:		
<b>cd</b> <directory></directory>	Moves to the directory specified by direct	ory
cd	Moves up a directory - two periods represen parent directory.	nt the
cd ~	Moves to your home directory – tilde repres your home directory.	sents
Make a new directory:		
mkdir <directory></directory>	Makes a new directory called directory	
Display the (path of the) current directory you are in:		
pwd	Displays the name of the current directory y in.	ou are
Copy a file or directory:		

<b>cp</b> <existing file=""> <newfile></newfile></existing>	Creates a new file identical to <i>existingfile</i> but with the name <i>newfile</i>
<b>cp</b> -R <existing dir=""> <newdir></newdir></existing>	Creates a new directory identical to <i>existingDir</i> but with the name <i>newDir</i>
Rename or move a file:	
mv <oldfile> <newfile></newfile></oldfile>	Renames <i>oldfile</i> to <i>newfile</i> within the same directory.
<pre>mv <oldfile> <directory newfile=""></directory></oldfile></pre>	Moves oldfile to a different directory with the name of newfile
Remove (delete) a file:	
<pre>rm <file></file></pre>	Deletes <i>file</i> . The file cannot be recovered.
Change password:	
yppasswd	Change current password.

#### **3** Setting up an Account to Run the Cadence Tools

You need to login a UNIX workstation and set up your UNIX environment to run the Cadence software. Depending on when your account was created, you may be using csh as your default login shell. The current recommended shell for ECS users is bash. To check if you are using, type "echo \$shell" at the shell prompt. If the reply is "/bin/csh", you will need to change to use the bash shell by typing "exec bash" at the shell prompt. Once you have established that you are using bash, proceed with the following steps to setup the Cadence tools.

Step 1:> mkdir cadence

Step 2:> mkdir cadence/models

Step 3:> mkdir inbox

**Step 4:** The following command will overwrite your .bashrc file in your home directory. If you have something important in your .bashrc file, save it to a temporary copy.

> bash /apps/ecs-apps/software/ece/cdssetup/cdsupdate2005

Add in your .bashrc changes if necessary.

Step 5:> source .bashrc

#### 4 Starting Cadence Software

**Step 1:** > cd ~/cadence (current directory must be cadence)

#### **Step 2:** > icfb &

A Command Interface Window (CIW) window appears on the screen, shown in Fig. 1.

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File Tools Options			Help	1
END OF SITE CUSTOMIZATION Loading corners.cxt Loading oasis.cxt				
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Fig. 1. Main window of Cadence tools.

#### 5 Creating Inverter Schematic

**Step 1:** In the *CIW* window, go to *File... \rightarrow New... \rightarrow Library* 

A New Library window appears. Fill out the pop-up form according to Fig. 2, and click OK.

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ок	Cancel	Apply	Hel
Library			
Name	ece2	249	
Path:	Ĭ		
Fechno	logy Libr	ary will not contain physical docian	(i.e., lovout) data you do not need a tach library
Other Choos	wise, yo se option	will not contain physical design ou must either attach to an exis :	ting tech library or compile one.
	🔷 No te	ch library needed	
	<ul> <li>Attac</li> <li>Comp</li> </ul>	h to existing tech library> ile tech library	AMI U.6Uu C5N (3M, 2P, high-res) -
Misc.			
	I/O Pa	d Type: 🔶 Perimeter 🔷 An	ea array

Fig. 2. Creating a new library.

**Step 2:** In the *CIW* window, go to *File... \rightarrow New... \rightarrow Cellview* 

A Create New File window appears, in Fig. 3. Fill it out and click OK.

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Cell Nam	e I	ми	
View Na	me s	chematid	
Tool	Ca	omposer-Scher	natic 💷
Library p	ath file		

Fig. 3. Creating a new file.

Then a new Virtuoso Schematic Editing window appears as in Fig. 4.

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Cmt	l:	Se	l: 0																	3
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Fig. 4. The Virtuoso Schematic Editing window.

### **Step 3:** In the *Virtuoso Schematic Editing* window, go to *Add...* → *Instance* ...

An *Add Instance* window will appear. Click *Browse*, and a *Library Browser* window appears as shown in Fig. 5.

### OOO 🛛 🖾 Library Browser - Add Instance

Library	Cell	View	
	I	I	
CSU_Analog_Parts CSU_Digital_Parts CSU_Sheets_8ths tanford_layout S_8ths S_10ths hdlLib mi05Layout mi05Layout mi05PadLayout mi05StdLayout mi05TechLib nalogLib asic dsDefTechLib dsSpice ce249 unctional eneralLib sipper ample heets tanfordTechLib smc018Layout smc018Layout smc018StdLayout smc018TechLib			
same035Lib			

Fig. 5. Instance window.

Step 4: Select *ami05Lib* in *Library*, *pmos4* in *Cell*, and *symbol* in *View*. The Add instance window should now have the pmos information filled in as in Fig. 6. Stamp a *pmos* device symbol in the *Virtuoso Schematic Editing* window, as shown in Fig. 7.

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Hide	Cancel	Defaults				Help
Library	ami05Li	म्			Brow	se
Cell	pmos4į́					
View	symbol					
Names	I					
Array		Rows	ľ	Column	s l	
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Effective	e Width		iPar("m	ı")*iPar(	"w") MĮ́	
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Fig. 6. Add instance window.

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Fig. 7. Stamping *pmos* device.

- Step 5: Repeat step 3–4, but adding an *nmos4* transistor.
- **Step 6:** In the *Virtuoso Schematic Editing* window, go to *Add...*  $\rightarrow$  *Pin*. Name the pin 'A'.
- Step 7: Repeat step 11 for a pin named 'B'.
- **Step 8:** Repeat step 11 for a pin named 'vdd'.
- Step 9: Repeat step 11 for a pin named 'gnd'.
- Step 10: In the Virtuoso Schematic Editing window, go to Add... → Wire and connect the instances as shown in Fig. 8.

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11 A.																		11.

Fig. 8. Inverter schematic

Step 11: In the Virtuoso Schematic Editing window, go to Design... → Check and Save. You should have no errors or warnings.

### 6 Symbol Creation of Sub-Circuits in Cadence

If a design is complicated, generally we use the top-down design method, or hierarchy structure. In this case, it is very beneficial to assign each sub-circuit a corresponding symbol (or icon) to represent that module. This step largely simplifies the schematic representation of the overall design. Thus, the "symbol" view of a circuit module is an icon that stands for the collection of all components within the module.

## Step 1: In the Virtuoso Schematic Editing window, go to Design... → Create Cellview → From Cellview, the following window will pop up.

000	9		X Cellvi	ew From Cellview		53 1
ок	Cancel	Defaults	Apply			Help
Library I	Name	ece249				Browse
Cell Nam	ie	INV				
From Vie	ew Name	schematic	-	To View Name	symbol	
				Tool / Data Type	Compose	r-Symbol 😑
Display	Cellview					
Edit Opt	ions					11

Fig. 9. "Cellview From Cellview" form.

- Step 2: Check the view names and click *OK*. Make sure that the target view name is symbol, which is indicated in "*To View Name*".
- **Step 3:** In a new window, a symbol is automatically generated. The default shape of the symbol icon is a rectangle as shown in Figure 10.

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	>																			1.

Fig. 10. Automatically generated inverter symbol.

- **Step 4:** Editing the shape of the symbol icon. You can do the following operations on your symbol:
  - (1) Deleting/replacing some existing parts
  - (2) Adding new geometric shapes
  - (3) Changing the locations for pins and instance name
  - (4) Adding new labels

Figure 11 is an example for a manually created inverter symbol, which was obtained by editing the symbol shown in Fig. 10.

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Fig. 11. The inverter symbol after modification.

Step 5: In "*Virtuoso Symbol Editing*" window, go to *Design… → Check and Save.* Thus, you have created your own symbol for future use.

#### 7 Simulation

Now we are going to simulate the inverter we just created to confirm that it operates as we expect.

**Step 1:** In the *CIW* window, go to *File... \rightarrow New... \rightarrow Cellview* 

A Create New File window appears, in Fig. 12. Fill it out and click OK.

ОК	Cancel	Defaults	Help			
Library 1	lame _	ece249				
Cell Name View Name		testinv				
		schematid				
Tool	a	Composer-Schematic ==				
Library p	ath file					

Fig. 12. Creating a new file.

Then a new Virtuoso Schematic Editing window appears as in Fig. 4.

Step 2: Add an instance of the new *INV* symbol that we just created as shown in Fig. 15.

000	9	🔀 Add Instan	ice		
Hide	Cancel	Defaults		Help	
Library	ece249			Browse	
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View	symbol			J	
Names	Ĭ			Ī	
Array		Rows	Columns	Ĭ	
Rotat	te	Sideways		Upside Down	

Fig. 13. Adding inverter instance

Step 3: Add a *vpulse* instance from the *analogLib* library with properties as shown in Fig. 14.

000	)	X	Add Insta	nce			
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Library	analogI	प्रम्			Browse		
Cell	vpulįse						
View symbol					-		
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Rise time	B		3n aj				
Fall time			3n aļ				
Pulse wi	dth		3n a				
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Fig. 14. Properties of *vpulse*.

**Step 4:** Add a *vdc* instance from the *analogLib* library with properties as shown in Fig. 15.

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Library	analogI	ıң		Browse
Cell	vdď			
View	symbol			
Names	X			
Array		Rows 1	Columns	Ĭ
Rota	te	Sidewa	ays	Upside Down
AC magn AC phase DC volta	iitude e ge e name	)             	<u>I</u>	

Fig. 15. Properties of vdc.

- **Step 5:** Add an output pin named **Vout.**
- Step 6: In *Virtuoso Schematic Editing* window, go to *Add...* → *Wire*, connecting all the components as shown in Fig. 16. The vdd and gnd symbols are in the analogLib library.



Fig. 16. The completed testinv schematic.

- Step 7: In the Virtuoso Schematic Editing window, go to Add... → Wire Name, and name the input wire to the inverter Vin.
- Step 8: In the *Virtuoso Schematic Editing* window, go to *Design... → Check and Save*. Correct any errors in your schematic figure.
- Step 9: In the Virtuoso Schematic Editing window, go to Tools... → Analog Environment, an Analog Circuit Design Environment window appears as shown in Fig. 17.

000 X	Cadence® Analog Design Environment (1)	
Status: Ready	T=27 C Simulator: spectr	e 5
Session Setup Analyses	Variables Outputs Simulation Results Tools	Help
Design	Analyses	÷Ę
Library ece249	# Type Arguments Enable	⇒ AC F TRAN ⇒ DC
View schematic		
Design Variables	Outputs	Œ,
# Name Value	# Name/Signal/Expr Value Plot Save March	ø
		8
>		$\sim$

Fig. 17. Analog Circuit Design Environment window.

Step 10: In the Analog Circuit Design Environment window, go to Setup... → Model Libraries..., a Model Library Setup window appears. Click the Browse... button and then choose the models directory and then choose the ami05.scs model. Click Add, as in Fig. 18 and then click OK.



Fig. 18. Adding model path.

Step 11: In the Analog Circuit Design Environment window, go to Analysis... → Choose..., and fill out the form according to Fig. 19.

ок	Cancel	Defaults	Apply			Help
Analy	ysis	<ul> <li>tran</li> <li>xf</li> <li>pz</li> <li>pac</li> <li>psp</li> <li>qpnoise</li> </ul>	<ul> <li>✓ dc</li> <li>✓ sens</li> <li>✓ sp</li> <li>✓ pnoise</li> <li>✓ qpss</li> <li>✓ qpxf</li> </ul>	<ul> <li>◇ ac</li> <li>◇ dcmatch</li> <li>◇ envlp</li> <li>◇ pxf</li> <li>◇ qpac</li> <li>◇ qpsp</li> </ul>	◇ noise ◇ stb ◇ pss	
		Tra	ansient Analy	/sis		
Stop Accu	Time racy Det conserv	[12n] faults (ern ative n	preset) noderate	liberal		
Enab	led 🔳				Options.	

Fig. 19. Setting up transient analysis.

Step 12: In the Analog Circuit Design Environment window, go to Outputs... → To be Plotted... → Select on Schematic. Then go back to the testinv schematic window and select the Vin and Vout wires. Note, the wires should change color, and the signals should be added in the outputs window, as in Fig. 20.

Status: Selecting outpu	ts to be plotted T=27 C Simulator: spect	re
Session Setup Analyses	Variables Outputs Simulation Results Tools	Help
Design	Analyses	Ł
Library ece249	# Type Arguments Enable	⇒ AC F TRA ⇒ DC
View schematic		II I T X Y Z
Design Variables	Outputs	Ū₽.
# Name Value	# Name/Signal/Expr Value Plot Save March	4
	1 Vin yes allv no	Y
	2 Vout yes allv no	

Fig. 20. Analog Circuit Design Environment ready for a simulation.

Step 13: In the Analog Circuit Design Environment window, go to Simulation...→ Netlist and Run. The plot of the simulation should appear in a Waveform Window, like Fig. 21.



Fig. 21. testinv simulation result.

Step 14: In the Waveform Window, go to Axes... → Xaxis and change Plot vs independent variable to Plot vs 1/Vin, like Fig. 22, and click OK. The final plot should look like Fig. 23.

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ок	Cancel	Defaults	Apply		Help
Label 🗍 Style 🔺	Auto	Linear 🛆	Default	time ( s )	
Range 4	Auto		LUG		
<	/ Min-Max	÷.,			
Plot vs.	1	/Vin			7

Fig. 22. Axis form.

Step 15: Exit the *Analog Circuit Design Environment Simulation* window, and exit the *Virtuoso Schematic Editing* window.

**Step 16:** In the *CIW* window, go to *File... \rightarrow Exit*.

#### 8 Homework

- 1. What is the switching threshold of the inverter that you just created? Use the point at which Vin=Vout on the lower hysteresis curve to determine the switching threshold. Hand in Cadence Vout vs. Vin plots for this configuration and mark the switching threshold point.
- 2. What values of W or L for the pMOS transistor would change the switching threshold to exactly 2.5V? What does this tell you about  $\rho$  the ratio between the k's for the two transistors? Hand in Cadence Vout vs. Vin plots for this configuration.
- 3. What values of W or L for the nMOS transistor would give a switching threshold of 1.5V? Hand in Cadence Vout vs. Vin plots for this configuration.



Fig. 23. Output voltage vs input voltage for a CMOS inverter.