ECE 249 Lab 2

Spring 2005

1 Introduction

This lab will introduce you to concepts of performance characterization of VLSI circuits.

2 Create Parameterized Symbol

You are now going to modify the symbol from Lab 1 so that it can be parameterized so that you can modify the transistor parameters at the symbol level. This will allow you to change transistor parameters without having to descend into the hierarchy and also removes the need to create multiple inverters for different sizing requirements.

Step 1:> Start **icfb** and in the **CIW** window go to ***Tools…→ CDF…→ Edit.*** An **Edit Component CDF** window will open up. Fill it in as shown in Figure 1. The Cell Name should be the same as the name you used in Lab 1.

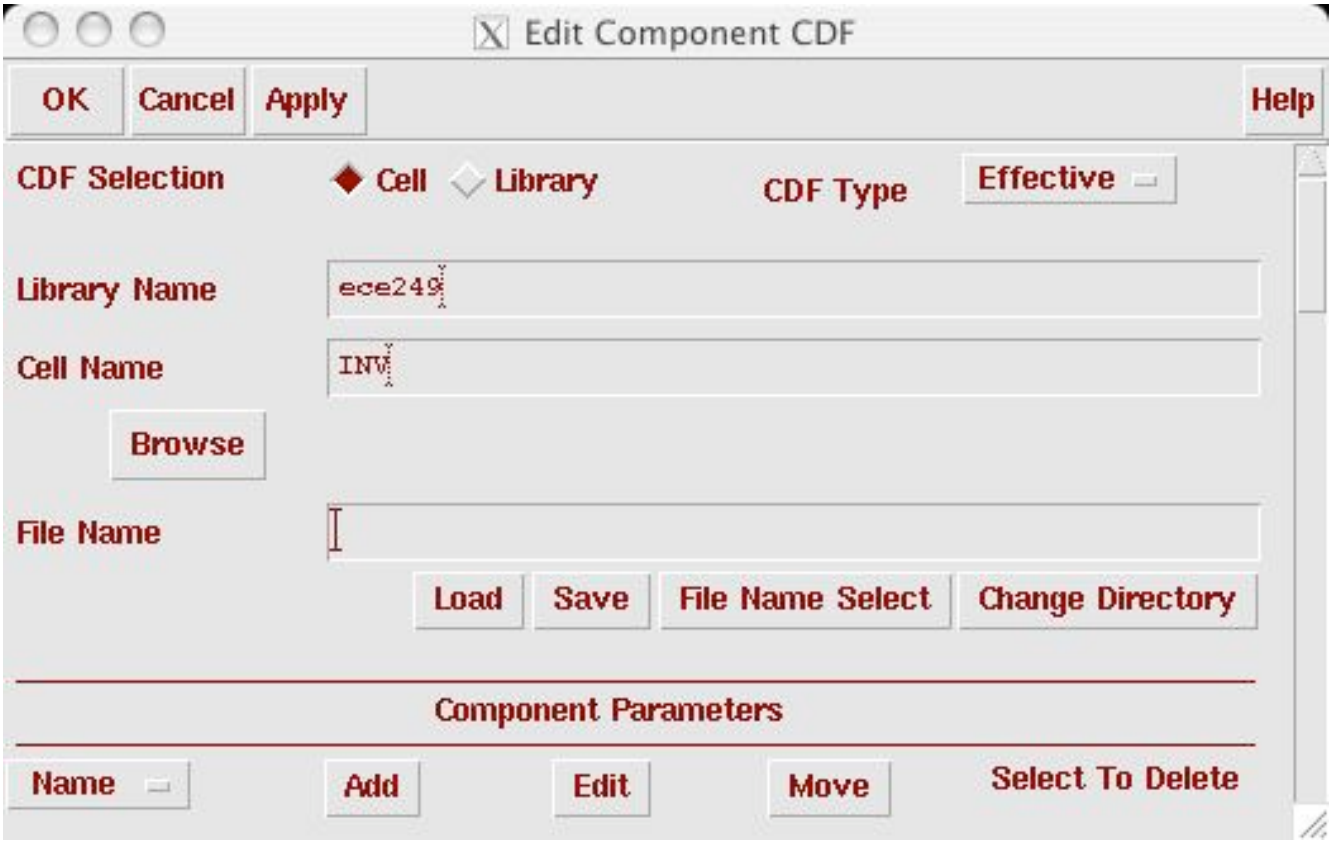

Figure 1. Edit Component CDF window

Step 2:> Click the **Add** button under **Component Parameters**, and the **Add CDF Parameter** window will appear. Fill in the window as shown in Figure 2 and then click **OK.**

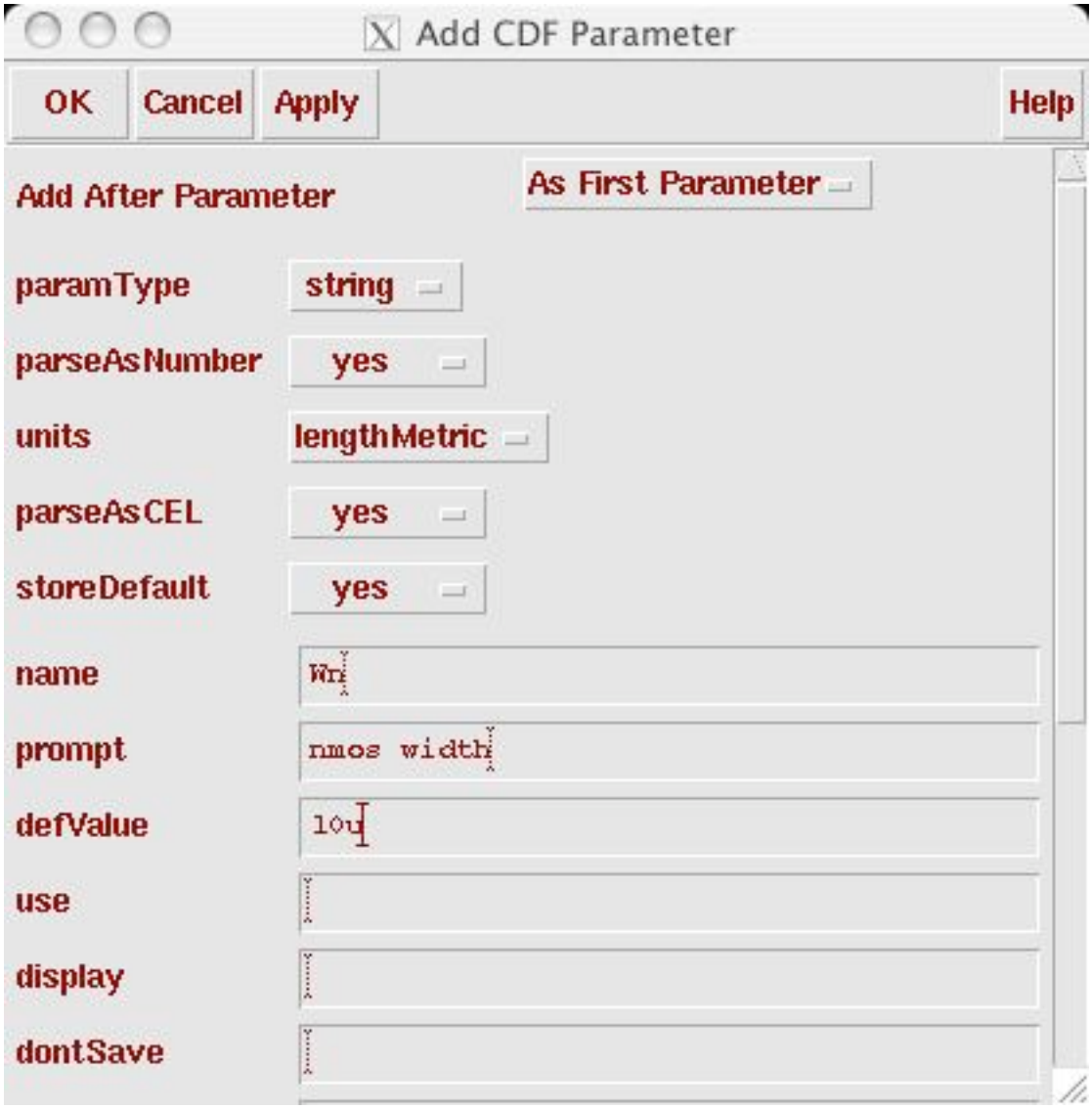

Figure 2. Add CDF Parameter window

Step 3: Repeat Step 2, to add a parameter named **Wp** and a prompt of "pmos width".

Step 4: Click **OK** in the **Edit Component CDF** window. From the **CIW** window, open the INV schematic from Lab 1.

Step 5: Select the nMOS transistor and edit its width property as shown in Figure 3. The **pPar** function will retrieve the parameter value from CDF parameter we created in Step 2.

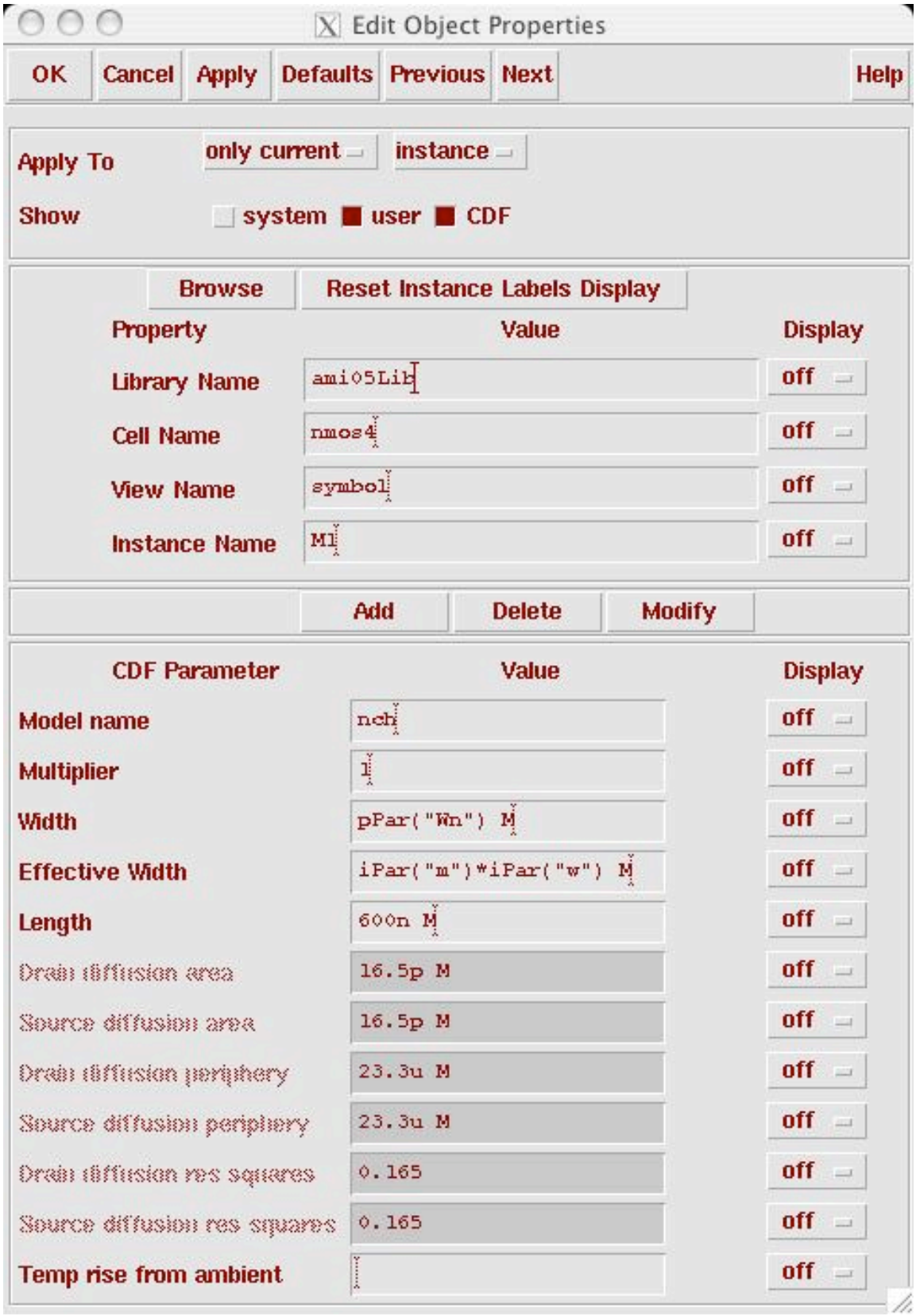

Figure 3. Edit nMOS properties

Step 6: Repeat Step 5, to change the pMOS width property to **pPar("Wp").**

3 Delay Measurement

Step 1: Create a new cellview schematic in the **ece249** library named **lab2.**

Step 2: Create the following schematic as shown in Figure 4. It should be similar to the **testinv** schematic from Lab 1. Set the properties of the ***vpulse*** to make a 5V square wave. You will need to change the fall and rise times to 1f s. Also change the pulse width to 6 ns.

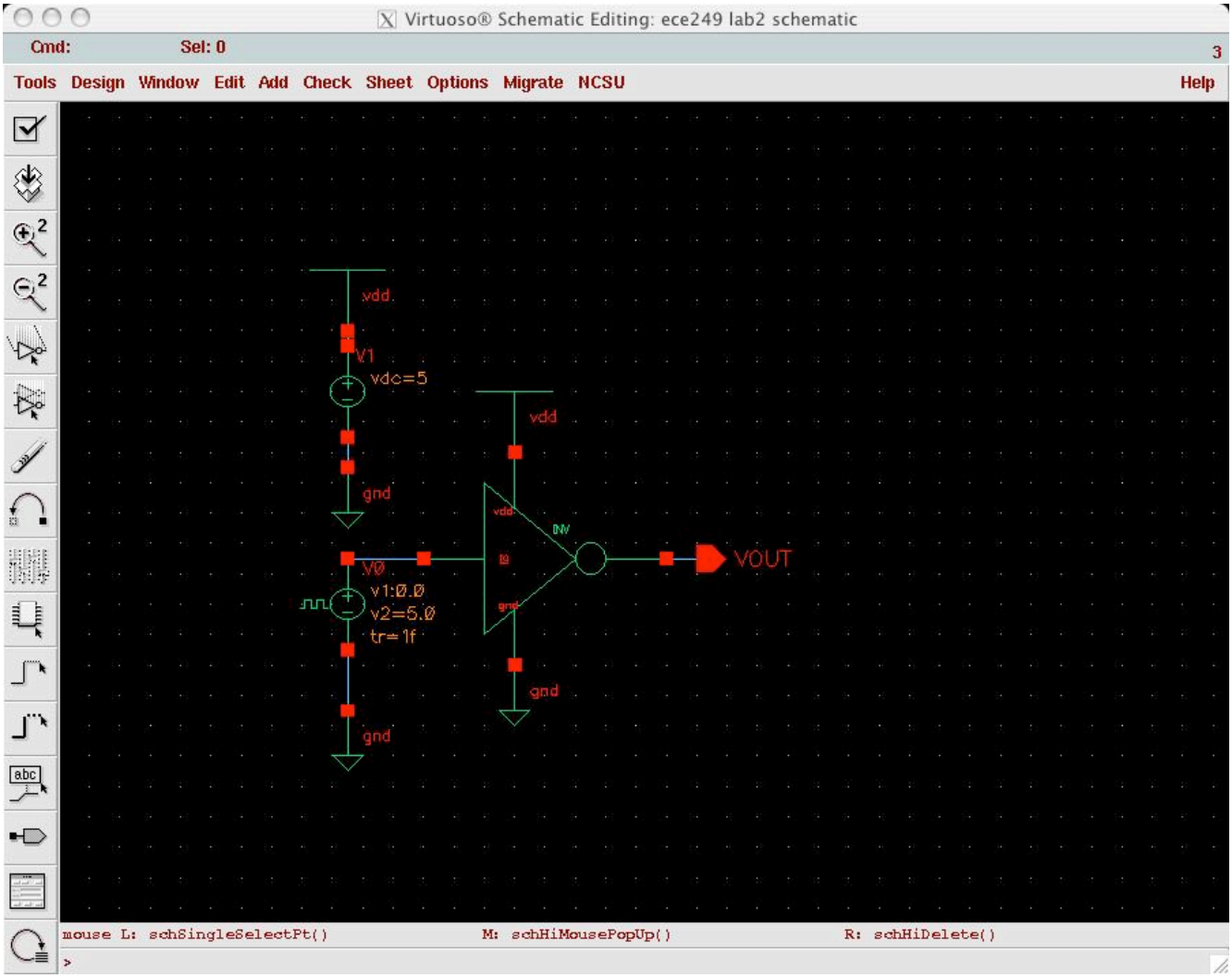

Fig. 4. Single inverter.

Step 3: Using **Analog Environment**, plot the input and output waveforms.

HANDIN (Due February 10, 2005)

1. Measure the rising and falling delay times from the **vpulse** to **VOUT**. Remember that the delay time is the time from 50%input to 50% output. Hand in a printout of the waveform for one period of the input along with the delay measurements.

Step 4: Add a 1pF capacitor from the **analogLib** library to the output as shown in Figure 5.

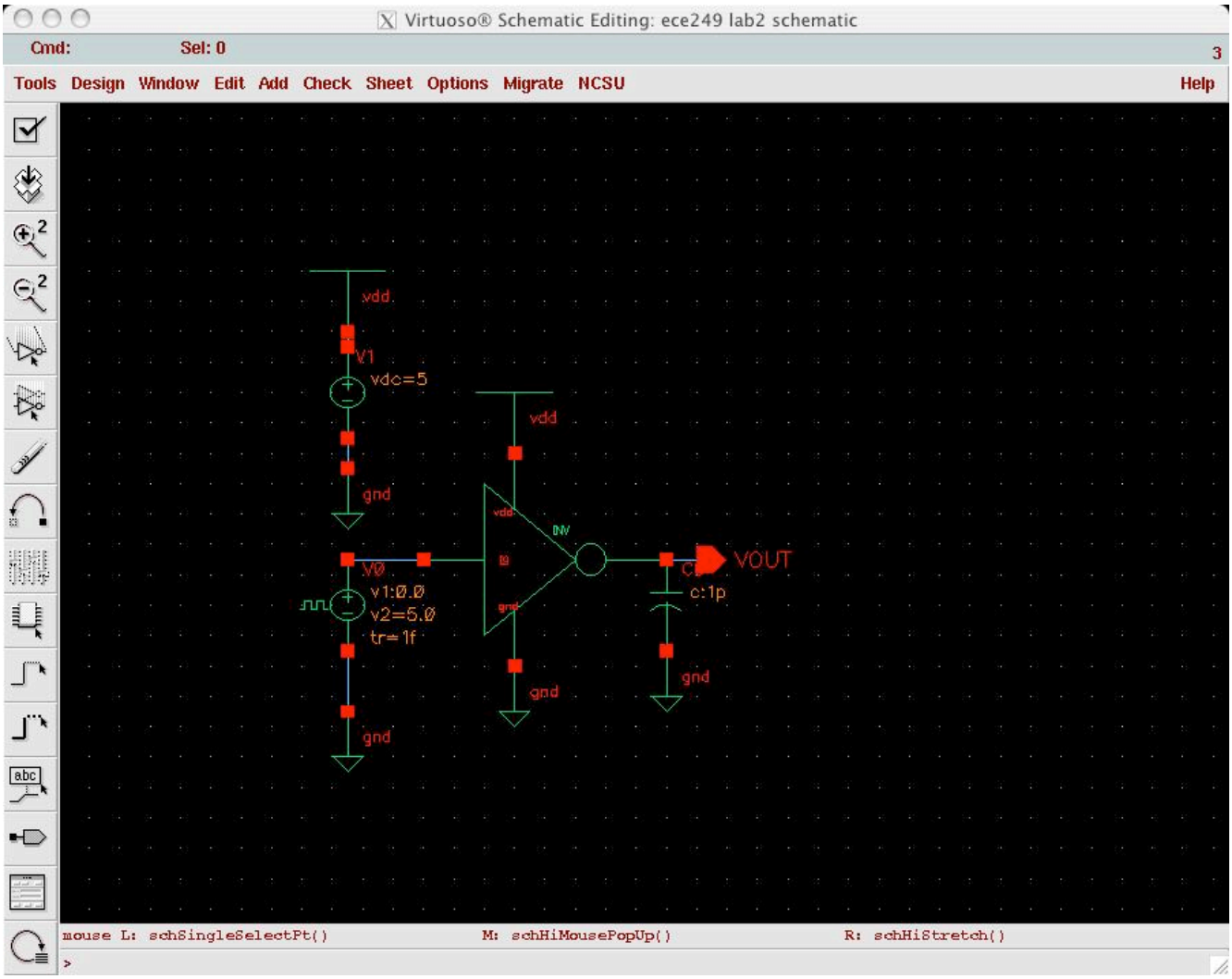

Fig. 5. Single inverter with capacitor.

Step 5: Using **Analog Environment**, plot the input and output waveforms.

HAND IN (Due February 10, 2005)

2. For the inverter with a capacitor, measure the rising and falling delay times from the **vpulse** to **VOUT**. Hand in a printout of the waveform for one period of the input. Mark clearly the delay measurements.

3. Comment on why the delay times changed?

4. Why are the rising and falling delay times different?

5. What should be the width of the pMOS transistor so that the delay times are equal? Show how you arrived at that value. Hand in a printout of the output waveform for this balanced inverter. Mark clearly the delay measurements.

Step 6: Add a second inverter as shown in Figure 6. For both inverters, adjust the pMOS width to the value you arrived at above so that both inverters are balanced.

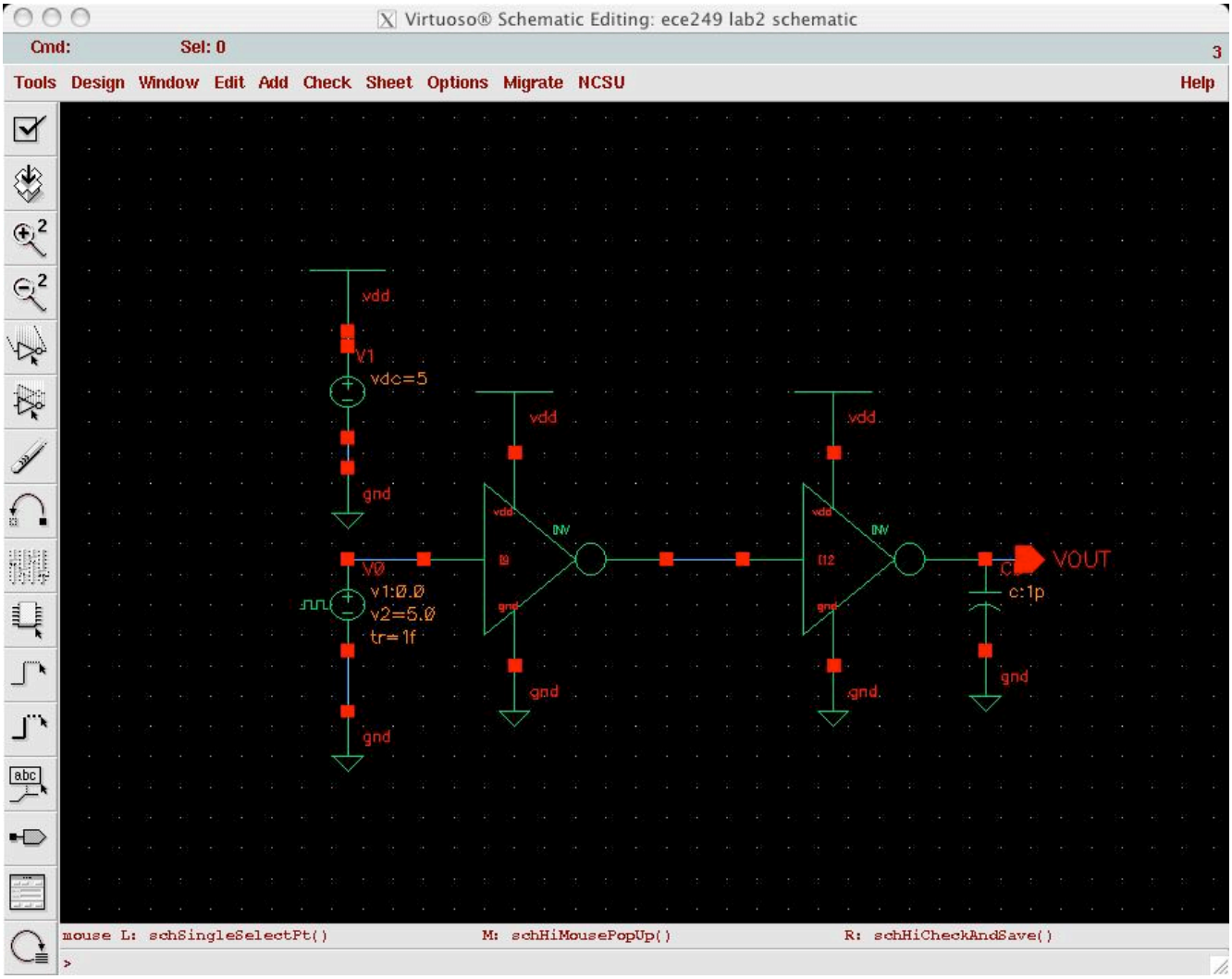

Fig. 6. Two inverters with capacitor.

HAND IN (Due February 10, 2005)

6. For the two-inverter configuration, measure the rising and falling delay times from the **vpulse** to the input of the second inverter. Hand in a printout of the waveform for one period of the input. Mark clearly the delay measurements.

7. Why has the delay time changed for this single inverter?

8. For the two-inverter configuration, measure the rising and falling delay times from the **vpulse** to **VOUT**. Hand in a printout of the waveform for one period of the input. Mark clearly the delay measurements.

9. Change the capacitor to 10pF.

10. How has this changed the delay from **vpulse** to **VOUT**? Will the circuit work as expected? Hand in the output waveform.

11. Adjust the size of the second inverter to minimize the delay of the two inverters and show how you arrived at that value. You must keep the inverter balanced. Hand in the output waveform for the minimum delay.

12. Is it possible to size the second transistor to equalize the delay to the 1pF case? Why or why not?