ECE 249 Lab 3
Spring 2005

The figure below shows the schematic diagram for a NAND gate with Wn = Wp = 2μm, and L for both NMOS and PMOS = 0.6μm .

(i) Draw the schematic for this circuit on Cadence.
(ii) Make a symbol for this circuit.
(iii) To test your circuit, plot the input output characteristics.

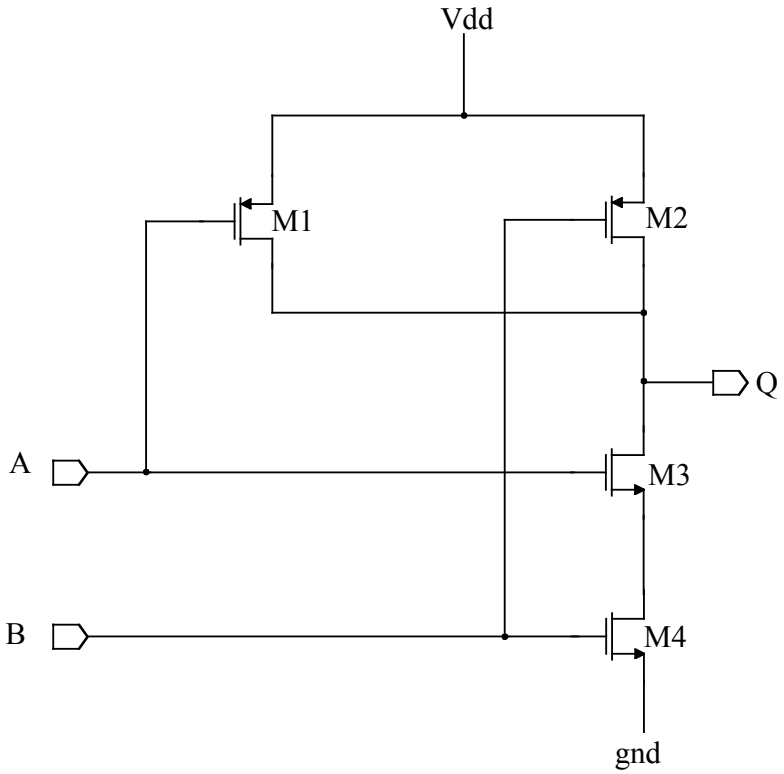

Fig. 1 Schematic diagram of a NAND gate.

HAND IN

1. Schematic for the above NAND gate
2. Input/output waveform showing all possible inputs for A & B
3. What is the worst-case propagation delay and on what input line?.