ECE 249 Lab 4

Spring 2005

Adapted from

"Short Tutorial on Cadence Layout", Z. Tao and M. Keramat, UCSN-0300-ZBT-04, July 2000

Cadence Software Fundamentals --- Layout

1. Introduction

This lab will introduce you to the Cadence layout tools. You will layout a CMOS inverter using AMI 0.5 μm technology.

2. Starting Cadence Layout Software

Step 1: `> cd cadence`

Step 2: `> icfb &`

A Command Interface Window (CIW) will appear.

Step 3: In the *CIW* window, go to ***Tools…→ Technology File Manager…*** and a *Technology File Tool Box* will appear. Click ***Attach…*** and a *New Technology Library* window will appear as in Fig. 1. Choose your **ece249** *Design Library* and the **NCSU_TechLib_ami06** *Technology Library*.

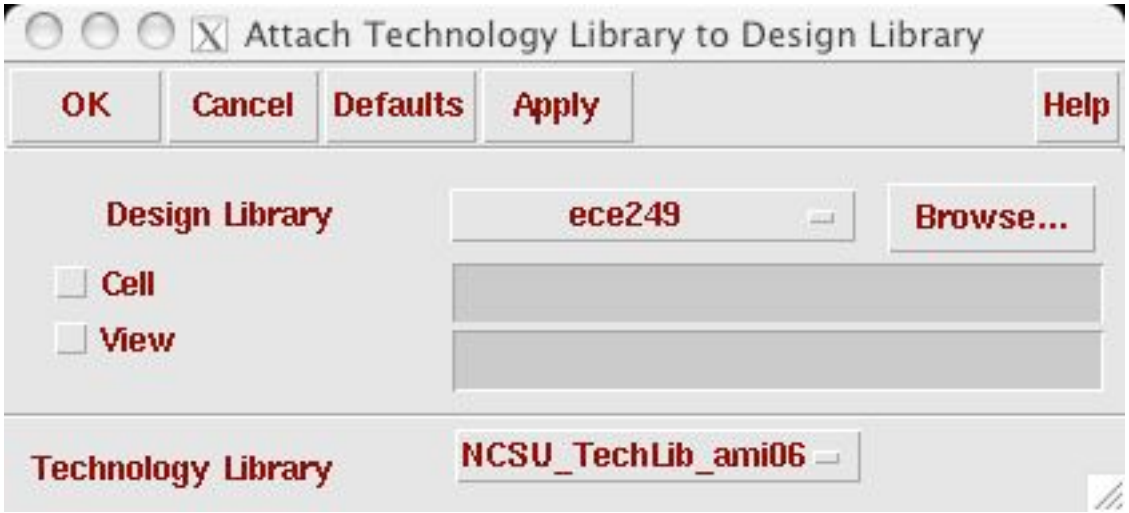

Fig. 1. Attach Technology Library window.

Step 4: In the *CIW* window, go to ***File…→ New…→ Cellview…*** and a *CreateNew File* window appears. Set the *Library Name* to *ece249,* your design library name, and *Cell Name* to *INV*. For *Tool*, choose *Virtuoso*, and the *View Name* of "*layout*" iwill be automatically added for you. Finally, click on *OK*.

At this time, you will see two windows appear, one is the *Layer Selection Window (LSW)*, and the other is the *Virtuoso Editing* window, shown in Fig 2.

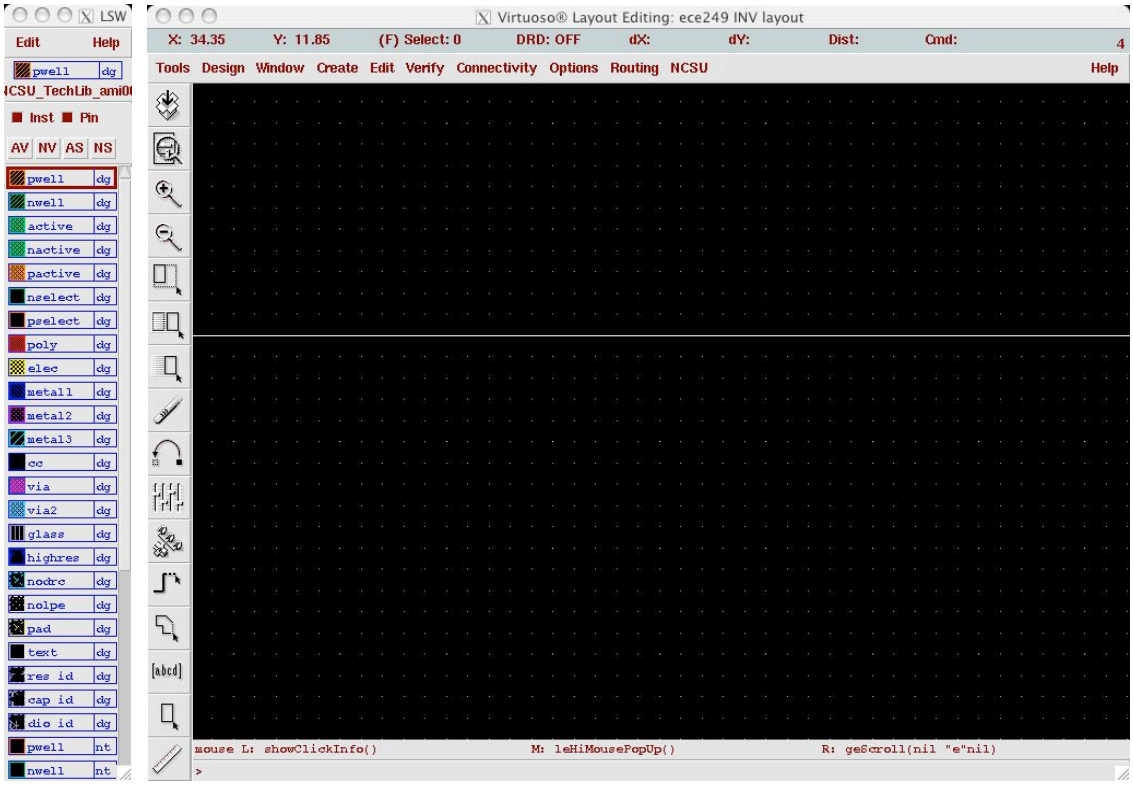

Fig. 2. LSW and Virtuoso windows.

Step 5: Drawing the N-diffusion (Active).
Select "*active*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing a box as shown in Fig. 3. When creating the rectangle for this step and for all subsequent steps, you will need to follow the AMI 0.5 design rules available at http://www.engr.uconn.edu/~chandy/ece249/SN05_Rules.pdf. You should periodically check that you are conforming to the design rules by going to *Verify* → *DRC*.

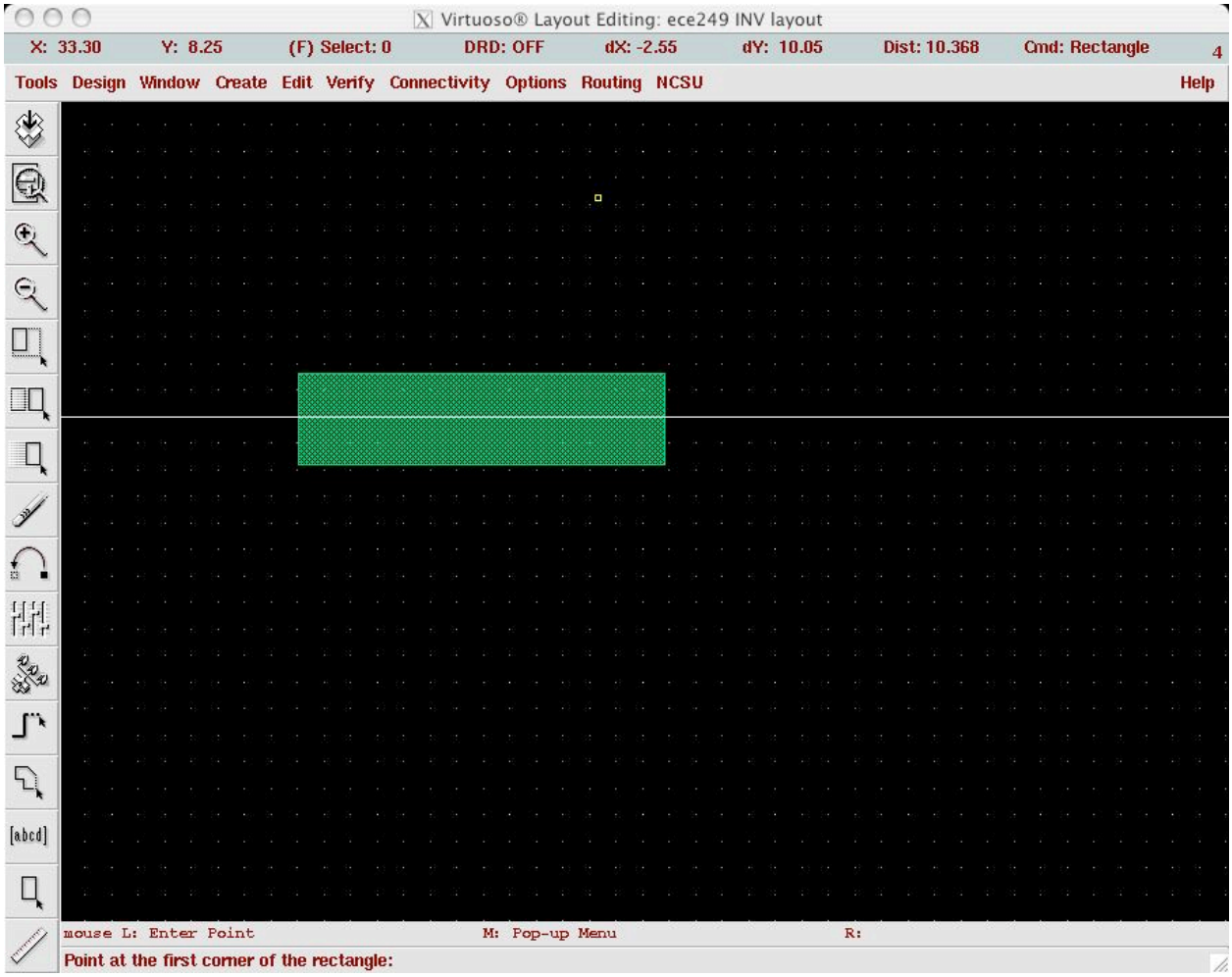

Fig. 43 The N-diffusion (Active) Box.

Step 6: Drawing the Gate Poly.
Select "*poly1*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing a gate box as shown in Fig. 5.

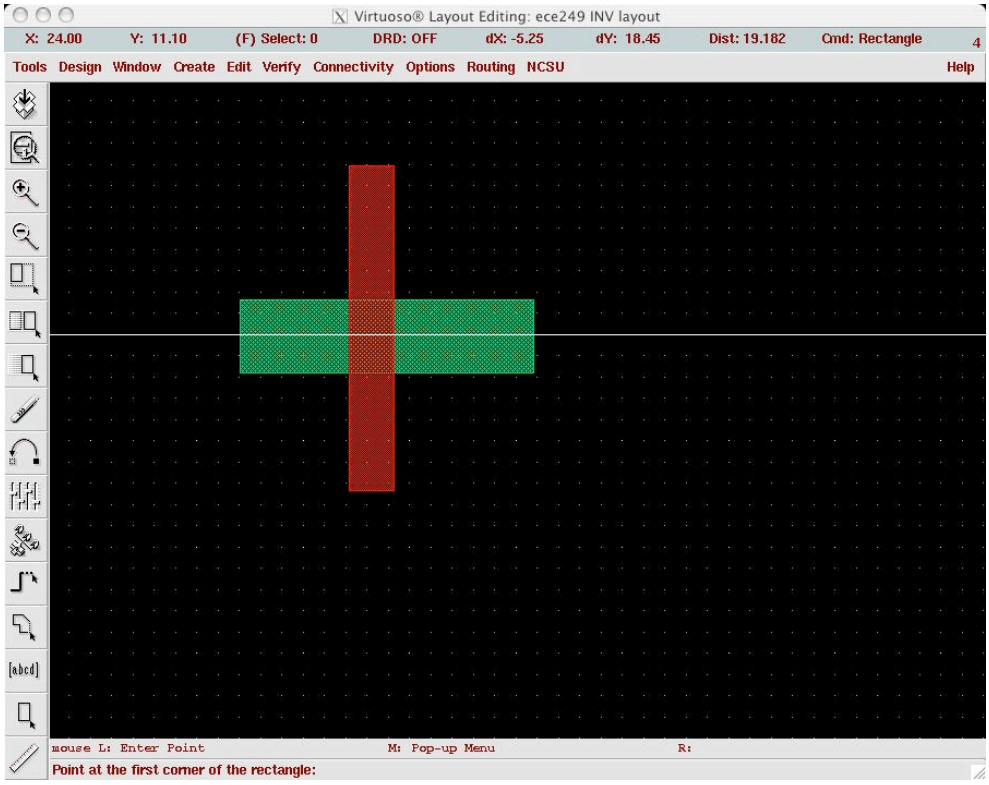

Fig. 4. Gate Poly Rectangle.

Step 7: Making Active Contacts.
Select the "*cc*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing two contact squares as shown in Fig. 5. The contacts must be exactly 0.6um by 0.6um.

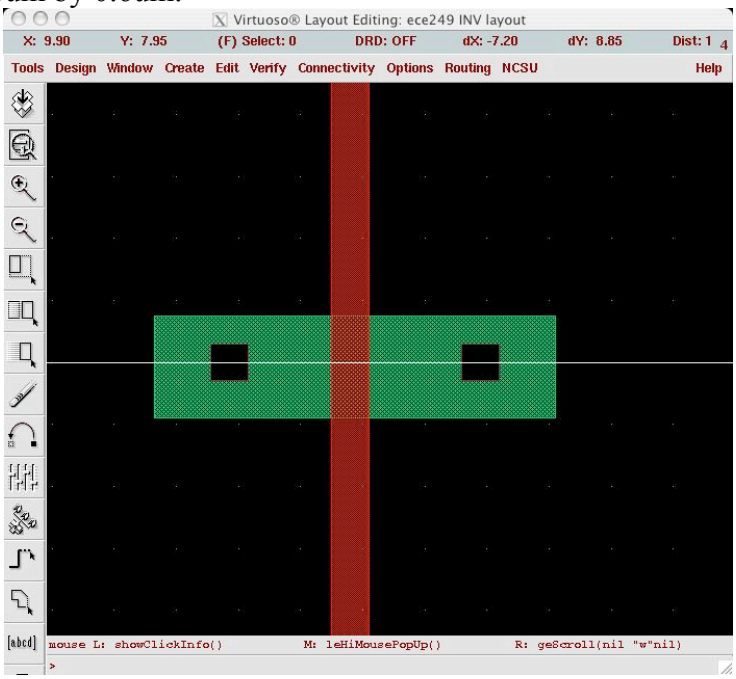

Fig. 5. Active Contact Blocks.

Step 8: Covering Contacts with Metal-1 and drawing an "Nselect" layer.
Select "*metal1*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing two metal-1 covering boxes. Then select "*nselect*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing a rectangle extending over the active region by 0.6 μm in all directions, as shown in Fig. 6.

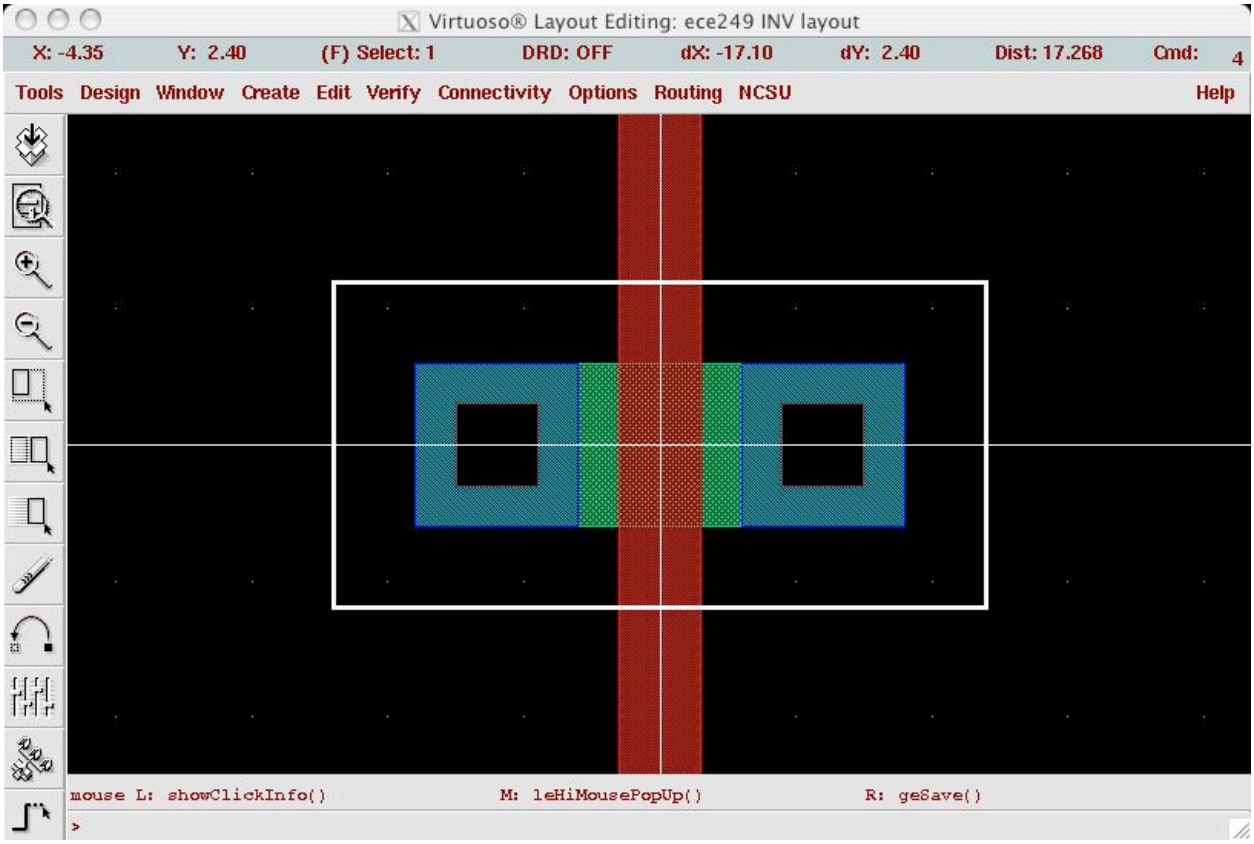

Fig. 6. NMOS layout.

Now you have finished the layout of a NMOS transistor.

Step 9: Drawing a PMOS transistor.
Repeat Steps 5-8 to draw a PMOS transistor., using a *pselect* layer instead of a *nselect* layer. You should end up with a layout as shown in Fig. 7. The pMOS transistor is above the nMOS transistor.

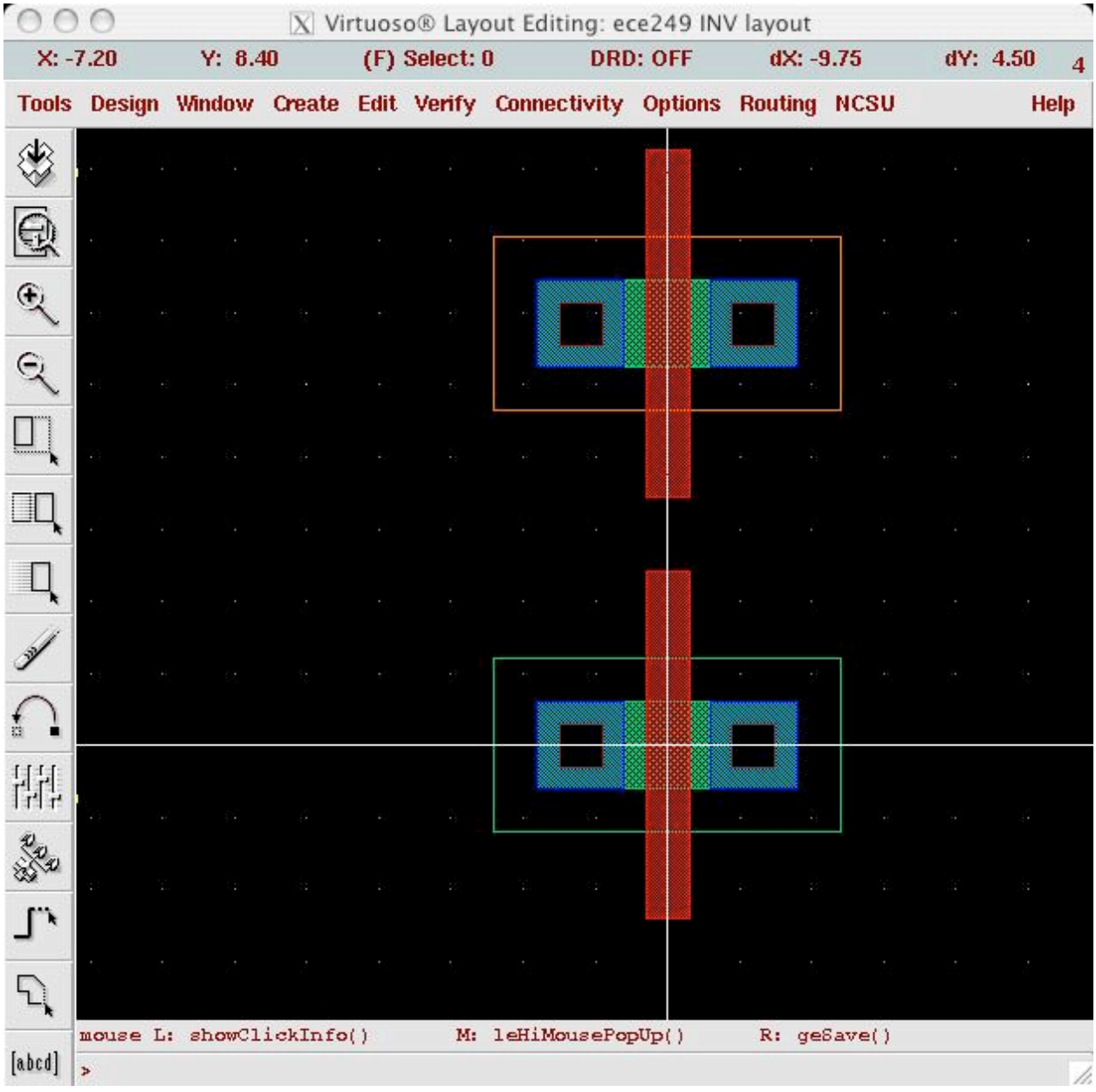

Fig. 7. Drawing the layout of PMOS.

Step 10: Drawing the N-Well.

Select "*nwell*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing a N-Well square as shown in Fig. 8.

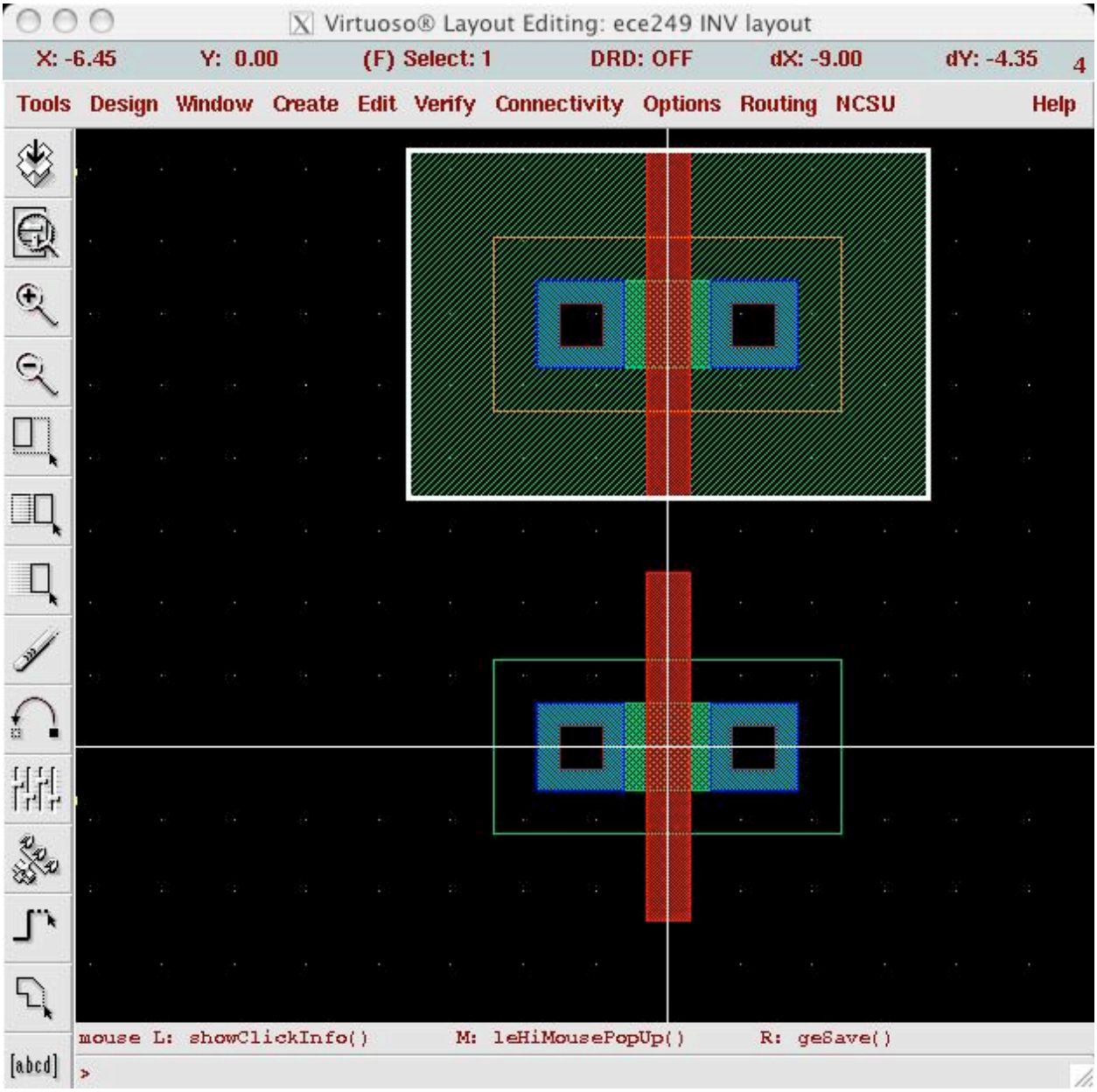

Fig. 8. Layout of NMOS and PMOS transistors.

So far, you have finished the layout of a NMOS and PMOS separately.

Step 11: Connecting the Output and Inputs of the inverter.
Use a "*metal1*" layer to connect the drains of the NMOS and PMOS transistors and use a "*poly1*" layer to connect the gates as shown in Fig. 9. Note that the transistors are completely symmetric and the source and drain regions are interchangeable.

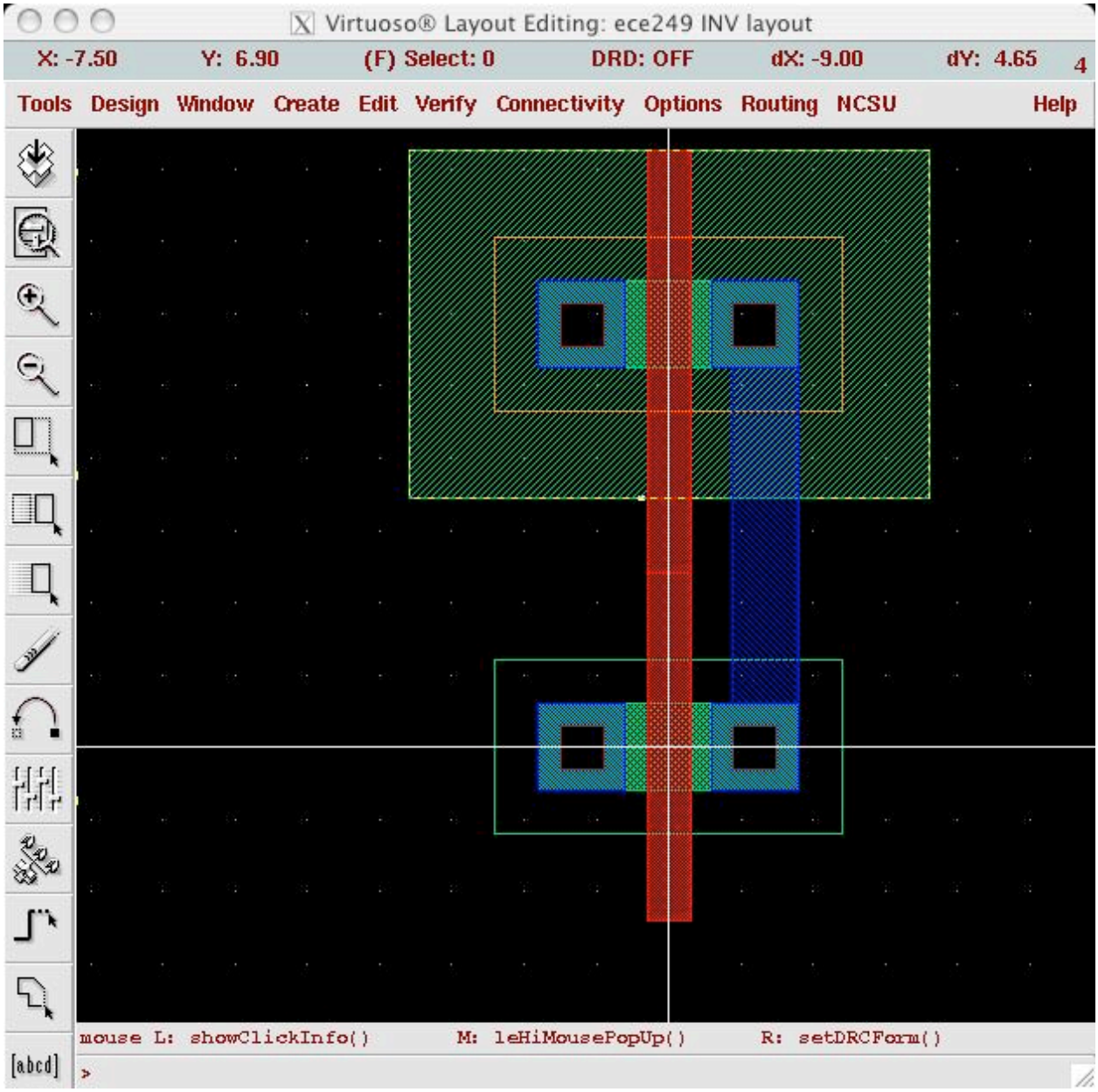

Fig. 9. Connecting the drains of NMOS and PMOS.

Step 12: Make a Metal-1 connection for the Input as shown in Fig. 10. Note that you must have a poly square completely surrounding the contact by 0.3um.

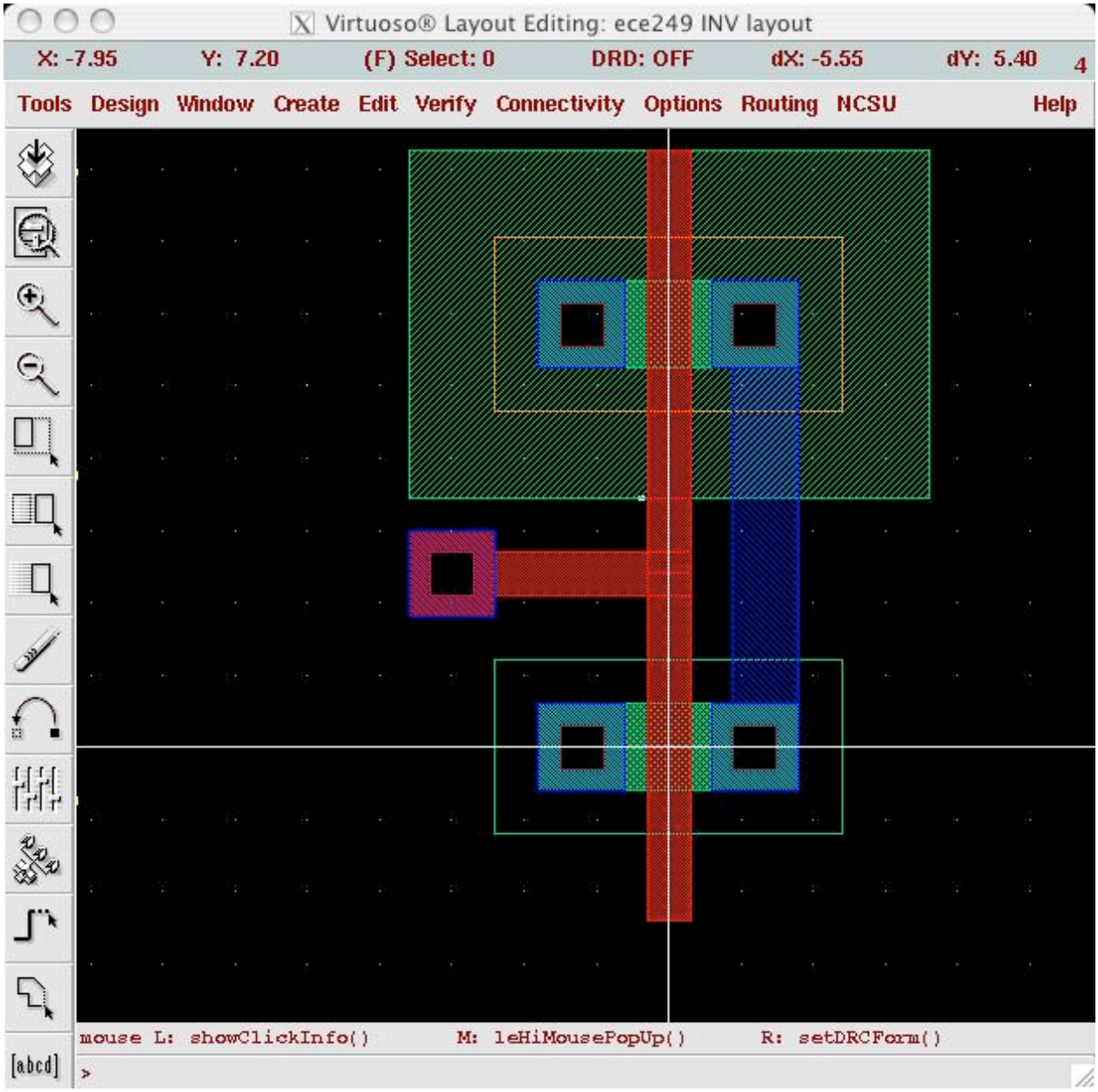

Fig. 10. Making a Metal-1 connection for the Input.

Step 13: Drawing the Power and Ground rails in Metal-1.

Select "*metal1*" layer from *LSW* window, and go to *Create* → *Rectangle* in the *Virtuoso Editing* window, drawing metal-1 box for the power and ground rails as shown in Fig. 11.

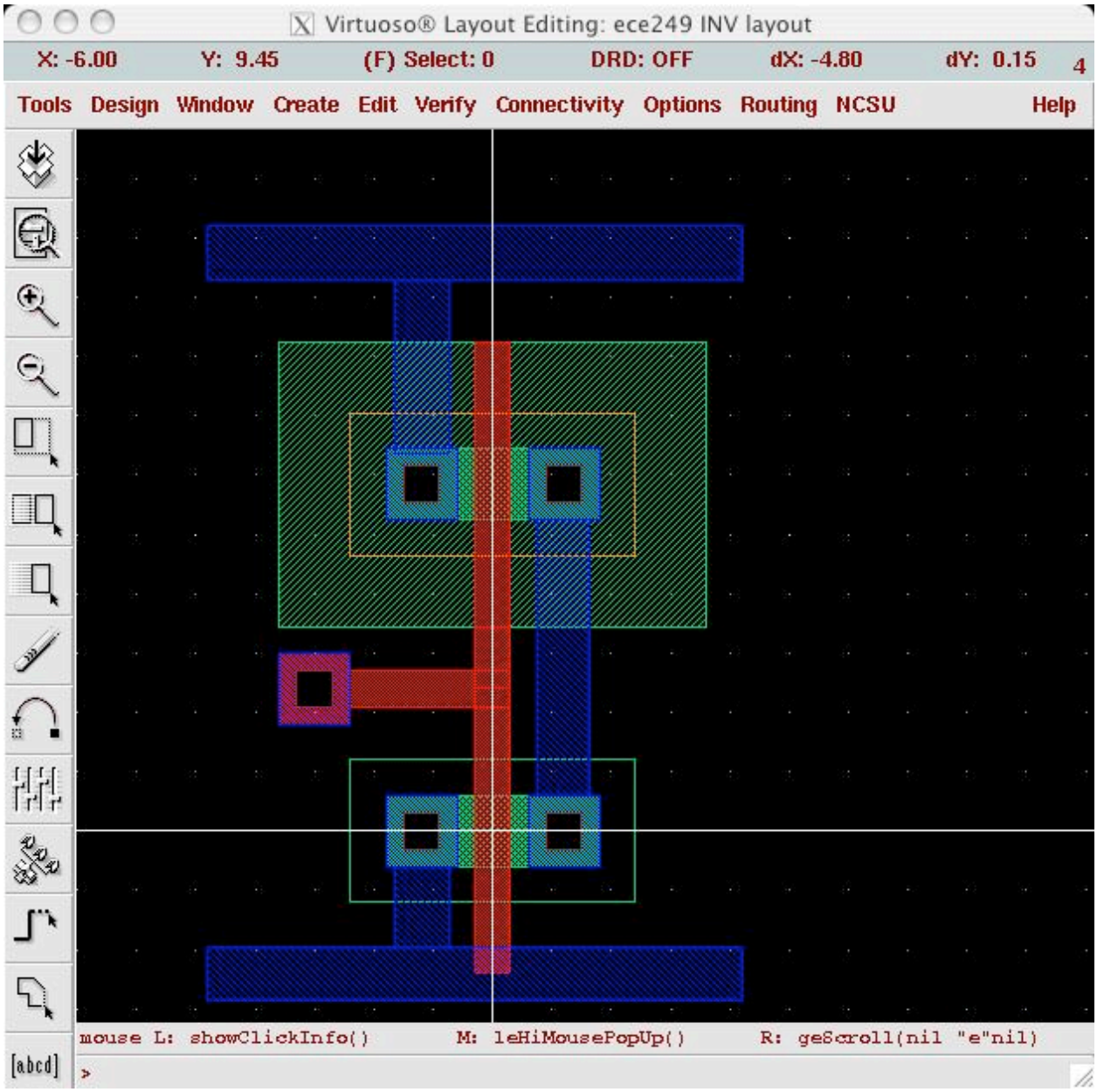

Fig. 11. The Power and Ground Rails in Metal-1

Step 14: Substrate contacts

As in Fig. 12, draw a p-select square next to the NMOS transistor, then draw an active inside the p-select region. Draw the active contact square inside the p-type active region, and finally make a metal connection to ground. For the N-substrate contact, draw a n-select square next to the PMOS transistor, then draw an active inside the n-select region. Draw the active contact square inside the n-type active region, and finally make a metal connection to vdd.

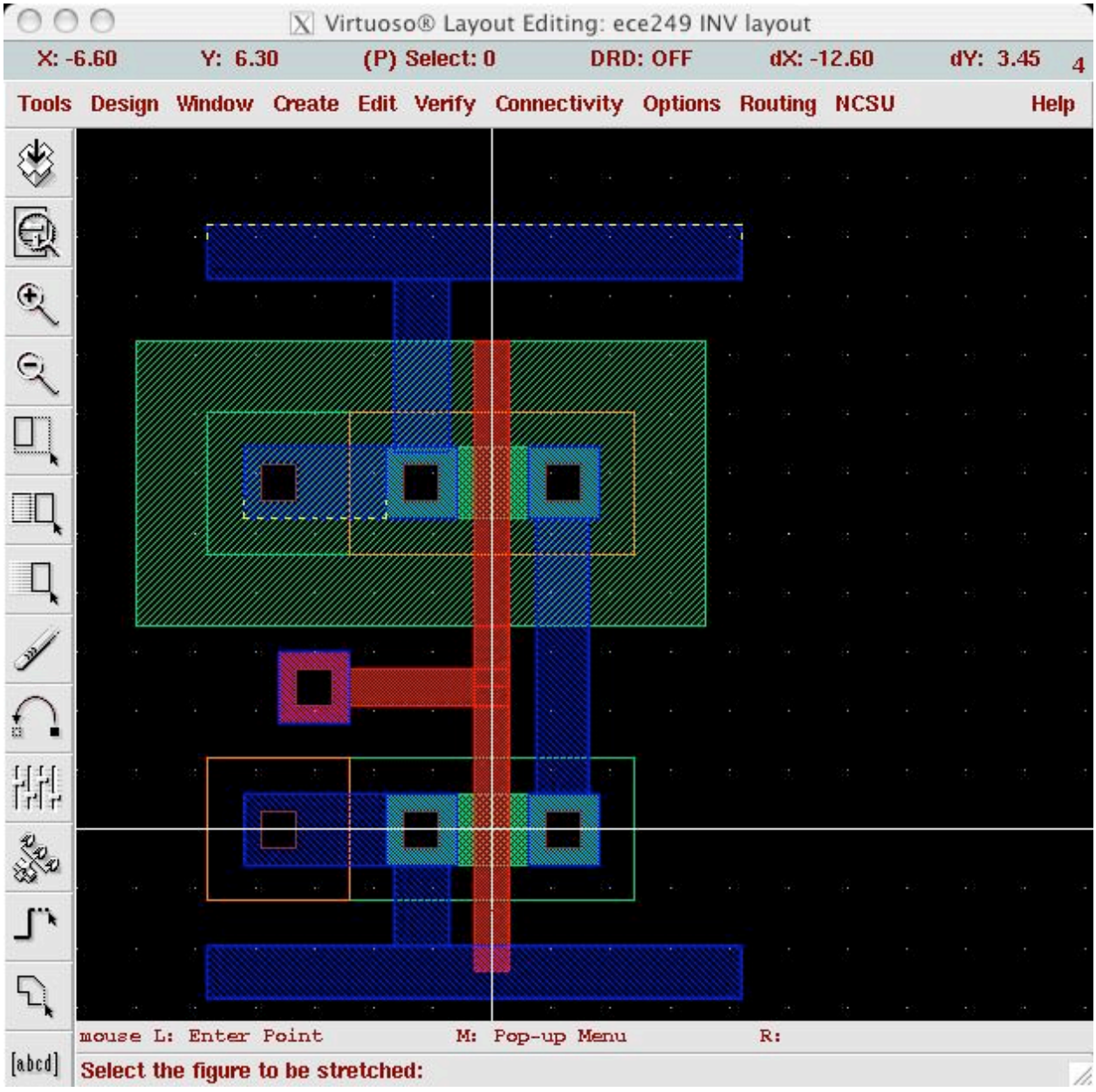

Fig. 12. Substrate contact.

Step 15: Run a DRC check and an LVS check to confirm that the layout conforms to the design rules and also matches the inverter schematic.
See http://www.engr.uconn.edu/~chandy/ece249/lvs.pdf for instructions on how to do LVS verificationø

Step 16: After you make sure your design passes DRC and LVS, merge all the blocks for the same layer by selecting the entire design and then going to *Edit* → *Merge*

HANDIN

Using the same techniques you used to create the inverter, draw the layout for a NOR gate, and hand it in. Make sure that the layout passes DRC and LVS. You will need to create a NOR schematic in order to run LVS.