# ECE 249 Lab 5

## Spring 2005

This lab is due on March 16th. The task is to design and layout a full adder. Follow the design and sizing suggestions in Figure 11-6 from the book. You will need to draw the schematics and then provide an optimal layout, and then simulate using the Cadence tools. The mirror design in Figure 11-6 should give you an idea on how to layout the adder. Hand in the schematics, the layout, LVS output, and simulation results. The truth table for a full adder is as follows.

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| **A** | **B** | **Cin** | **S** | **Cout** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |