ECE 249 Lab 7 Spring 2005

a. Design a two-stage dynamic domino logic implementation of the functions F=A+B+C and G=F+D as in HW4 problem 5a. Use n transistors with a width of 1.2 microns and p transistors with a width of 2 microns. Measure the rise time and fall time delays. Use the 1111 to 0000 transition and clk transition to measure the delays.

b. Design a two-stage dynamic zipper logic implementation of the functions F=A+B+C and G=F+D as in HW4 problem 5b. Measure the rise time and fall time delays as above.

Hand in schematics and waveforms for both parts. Compare the overall size of both designs by comparing the sum of the transistor widths. Explain any differences in the rise and fall times.