ECE 249
VLSI Design and Simulation
Spring 2005

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Department of Electrical and
Computer Engineering

Contact Info

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TA

- Janardhan Singaraju
- Office: HBL A-65
- Available for software and lab questions

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Books

- "Digital Integrated Circuits", Rabaey, Chandrakasan, and Nikolic
- Suggested reference materials
  - "Principles of CMOS VLSI Design", Weste and Eshragian
  - "CMOS Digital Integrated Circuits", Kang and Leblebici
  - "Digital Integrated Circuits", (ECE 215 notes), Ayers

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Class Schedule

- Lectures are in ITE 125
- No lectures during the weeks of April 13th and April 20th.
- Labs on Wednesdays will be in ITEB C25
  - No lab for the first week
- Lab will be open M-F 9-5
  - Evening hours may be available later in the semester

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Homework Policy

- 5 to 6 homeworks
- Due at the beginning of class on the due date
- 7 lab assignments

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Grading Policy

- 35% Exams (February 22nd and April 7th)
- 10% Homework
- 20% Labs
- 35% Final project

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Course goals

- Be able to contribute to an industry digital VLSI design project
- Become familiar with design tools (Cadence)
- Understand design flows
- Understand behavioral, structural, and physical specifications
- Can apply VLSI design practices

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Topics

- MOS Transistor Theory
- Circuit Characterization and Performance Estimation
- CMOS Logic Design
- VLSI Design Methodologies
- VLSI Subsystem Design
- Testing and Verification

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What is VLSI design?

- The process of creating an integrated circuit from specification to fabrication

What is an integrated circuit?

- A single integrated component that contains all the primary elements of an electrical circuit - transistors, wiring, resistors, etc.

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Integrated circuit

- Small Scale Integration (SSI)
  - Tens of transistors
- Medium Scale Integration (MSI)
  - Hundreds of transistors
- Large Scale Integration (LSI)
  - Thousands of transistors
- Very Large Scale Integration (VLSI)
  - Hundred thousands of transistors

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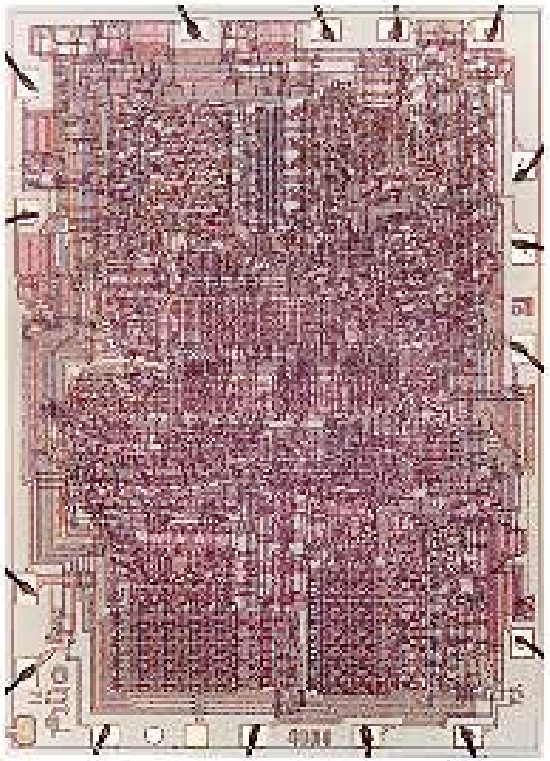
Intel 4004



- First microprocessor
- Designed in 1971
- 2300 transistors
- ~100 KHz

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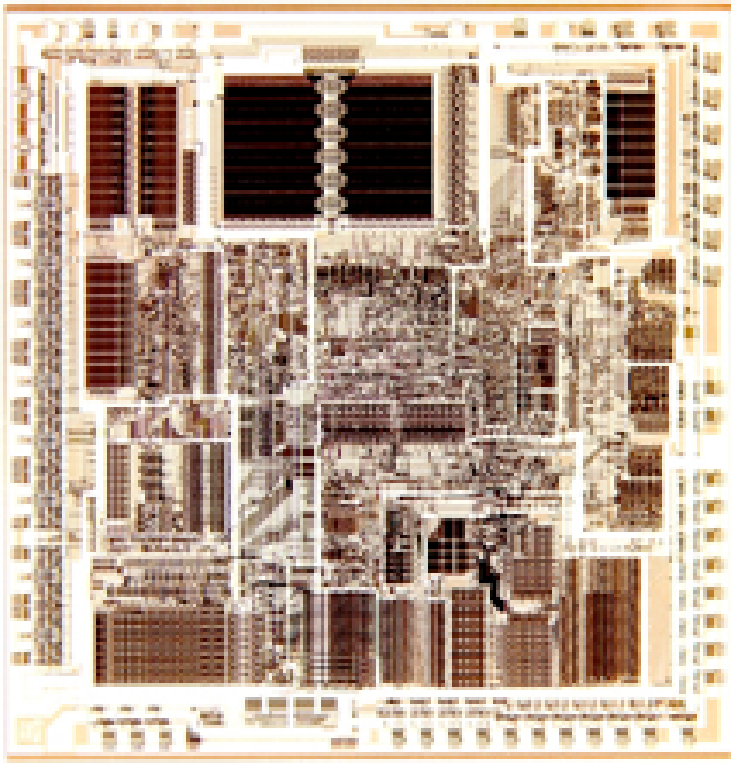
Intel 80286



- Released in 1982
- 134,000 transistors
- 6-12.5 MHz

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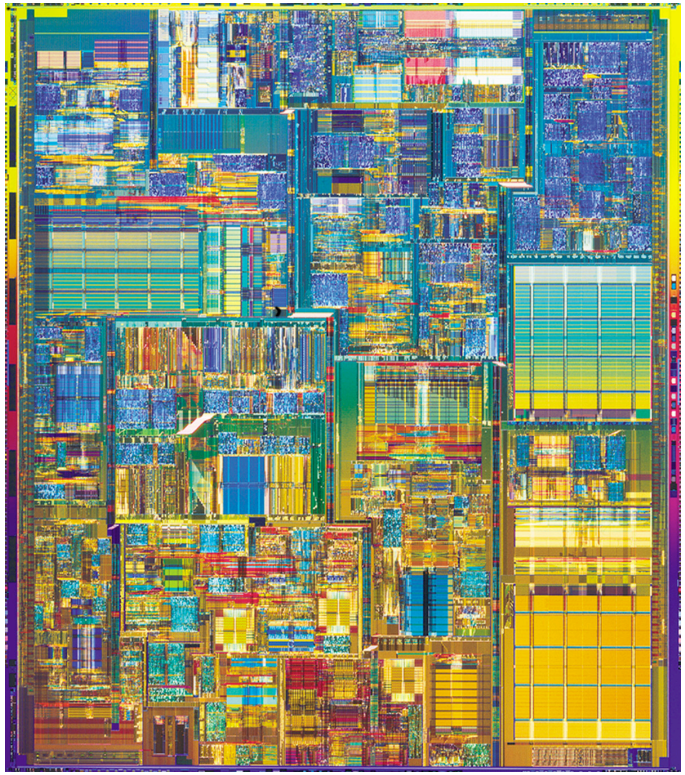
Intel Pentium IV



- Released in 2000
- 42 million transistors
- .18 micron
- > 1 GHz

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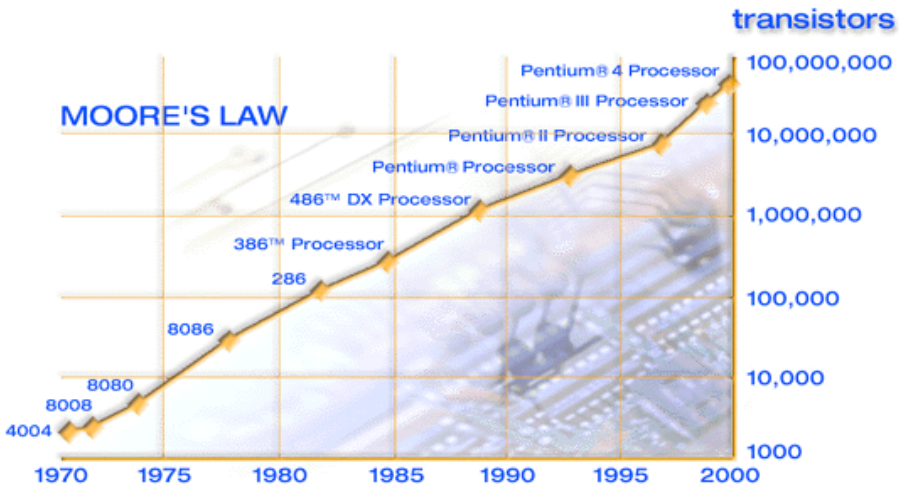
Moore's Law



The number of available transistors in a circuit doubles every 18 months

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100 million transistors???

- Partitioning
- Computer-Aided Design Tools (EDA)
- Design Methodology
- Testing and Verification

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Partitioning

- Break the problem into smaller more manageable parts
- Reuse logic modules
- Simplifies layout
- But its not always easy deciding how to partition the problem

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Computer-Aided Design Tools

- Schematic Capture
- Synthesis
- Simulation
- Verification
- Automated placement and routing

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Computer-Aided Design Tools

- Cadence
- Synopsys
- Mentor Graphics

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Design Methodology

- Functional Specification
  - What does the chip do?
- Behavioral Specification
  - How does it do it? (abstractly)
- Logic Design
  - How does it do it? (logically)
- Layout
  - How does it do it? (physically)

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Design constraints

- Budget ($$$)
- Area
- Power requirements
- Speed
- Schedule
- Risk

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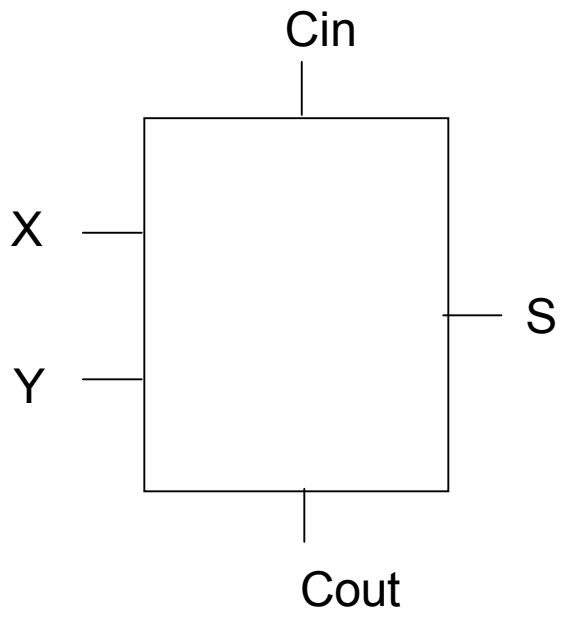
Functional Specification

Full Adder



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Behavioral specification

- VHDL
- Verilog

```
entity Full_Adder is
        generic (TS : TIME := 0.11 ns; TC : TIME := .1 ns);
        port (X, Y, Cin: in BIT; Cout, Sum: out BIT);
end Full_Adder

architecture Behave of Full_Adder is
begin
Sum <= X xor Y xor Cin after TS;
Cout <= (X and Y) or (X and Cin) or (Y and Cin) after TC;
end;
```


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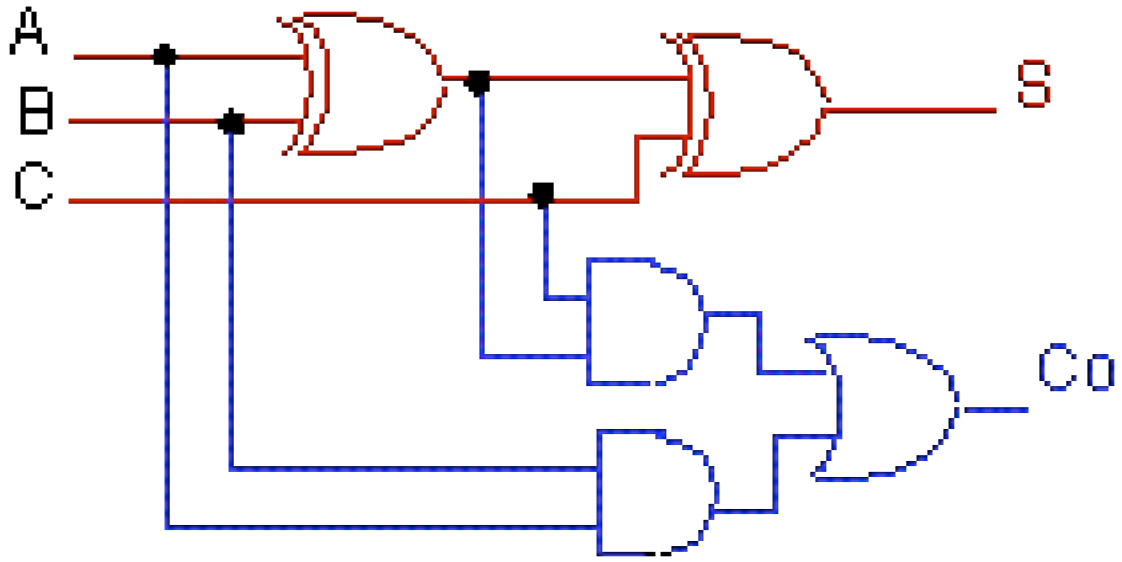
Logic Design



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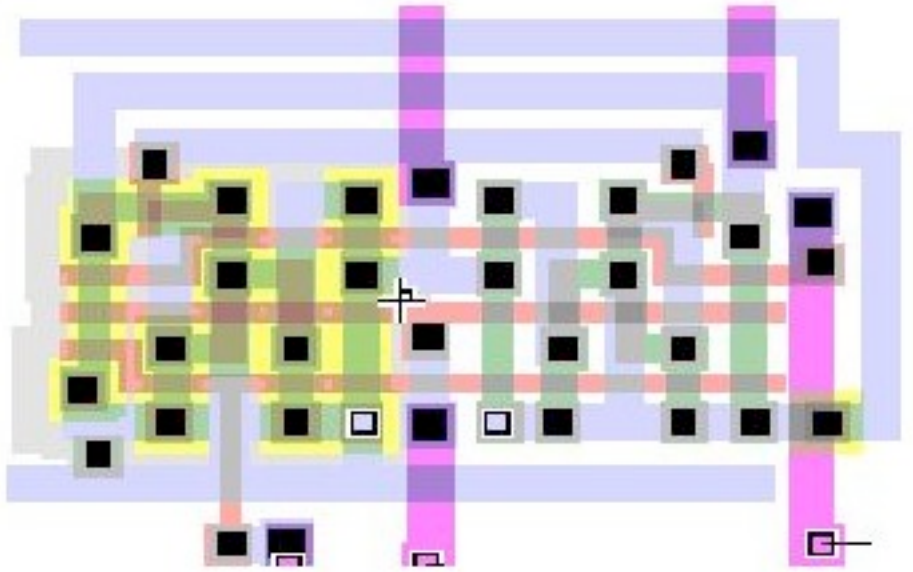
Layout



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Testing and Verification

- Do it at every phase of the design
- Critical to keeping to budget

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Trust, but verify …

Phase	Testing time	Time to redo	Cost to redo
Behavioral Spec	1-2 days	1-2 weeks	~$20K
Logic Design	2-3 days	2-3 weeks	~$40K
Layout	2-3 days	1-2 weeks	~$20K
Fabrication	1 week	3-4 months	$1MM

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VLSI Design Methodologies

- Full Custom
- Standard Cell
- Gate Array

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Full Custom VLSI Design

- Advantages
  - Fastest implementation possible
  - Can be very cheap in high volumes
- Disadvantages
  - Very expensive to design
  - Not customizable
  - Error-prone design flows

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Full Custom VLSI Alternatives

- Gate Arrays
  - Advantages
    - Faster than microprocessor
    - Field programmable versions are easily customizable
    - Design is easier than full custom VLSI
  - Disadvantages
    - Slower than full custom VLSI
    - Limited in number of transistors/gates
    - Takes more area

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Full Custom VLSI Alternatives

- Standard Cell Design
  - Advantages
    - Faster design time than full custom
    - Higher performance than Gate Arrays
  - Disadvantages
    - Lower performance than full custom
    - More area than full custom

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Full Custom VLSI Alternatives

- Microprocessor
  - Advantages
    - General purpose
    - Widely available
    - Cheap on a single use basis
    - Design is easy
  - Disadvantages
    - Slower than VLSI
    - Takes more area
    - More expensive than VLSI over millions of units

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MOS Transistor Theory

- We will focus only CMOS VLSI design since that is the dominant design style in current industry practice
- Other VLSI technologies include:
  - nMOS
  - TTL
  - BiCMOS
  - GaAs
  - ECL

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MOS Transistor Theory

- Two types of transistors
  - nMOS
  - pMOS
- Digital integrated circuits use these transistors essentially as a voltage controlled switch

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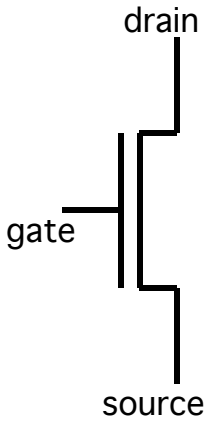
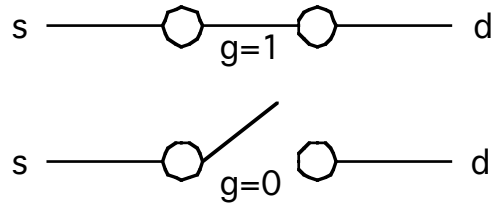
nMOS Transistor

- If the gate is “high”, the switch is on
- If the gate is “low”, the switch is off





- Conducts “lows” well

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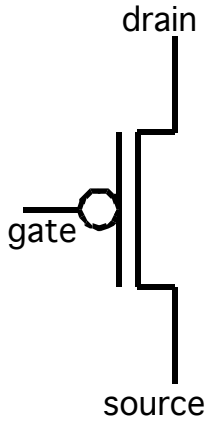
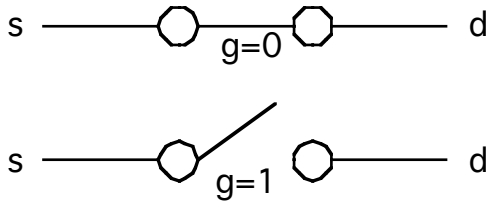
pMOS Transistor

- If the gate is “low”, the switch is on
- If the gate is “high”, the switch is off





- Conducts “highs” well

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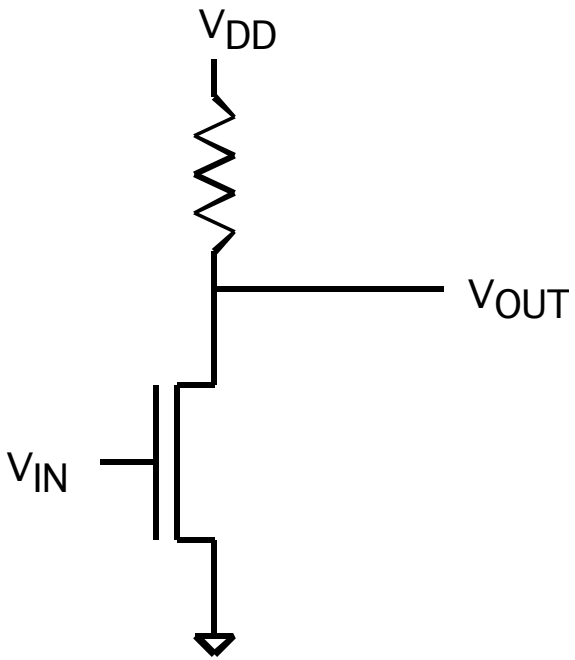
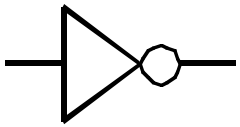
Logic gates in nMOS





Inverter

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Problems with nMOS

- Static current draw
  - When the transistor is on, there is a path from V_{DD} to ground
  - More power drain
- Logic high output does not go all the way to VDD

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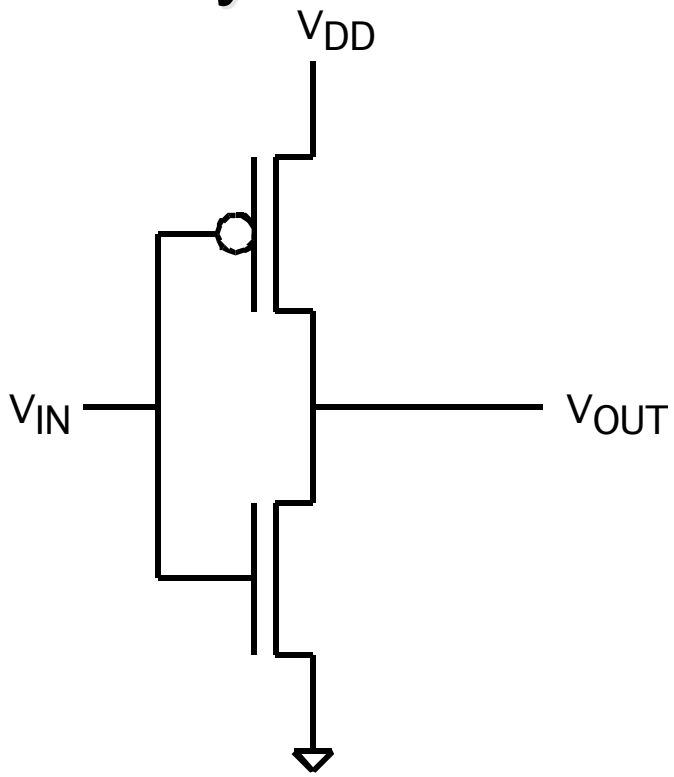
Solution: CMOS

- Complementary MOS



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CMOS

- No static current flow
- Less current means less power

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Next class

- Read Chapters 1, 2 and 3 of book

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