VLSI Design and Simulation

Lecture 2

MOS Transistor Theory

Lab

- Make sure that you have an engineering UNIX account
- Contact ECS if you don't

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MOS Transistor Theory

- Two types of transistors
  - nMOS
  - pMOS
- Digital integrated circuits use these transistors essentially as a voltage controlled switch

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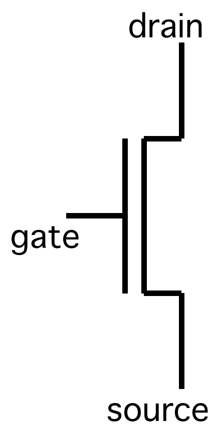
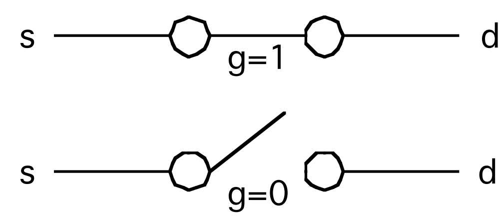
nMOS Transistor

- If the gate is “high”, the switch is on
- If the gate is “low”, the switch is off





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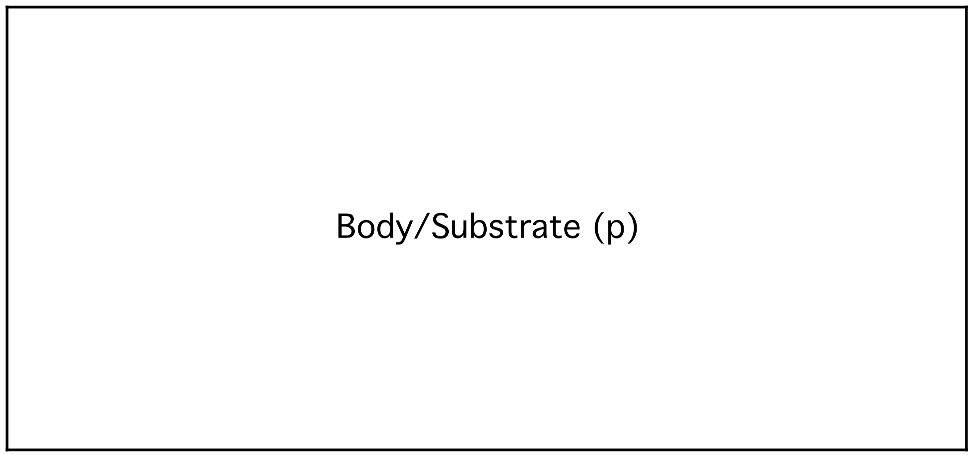
nMOS Transistor



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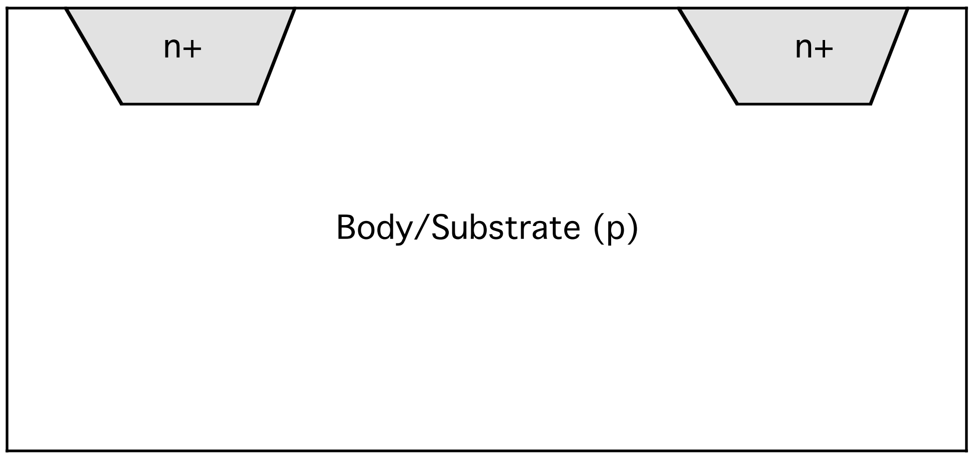
nMOS Transistor



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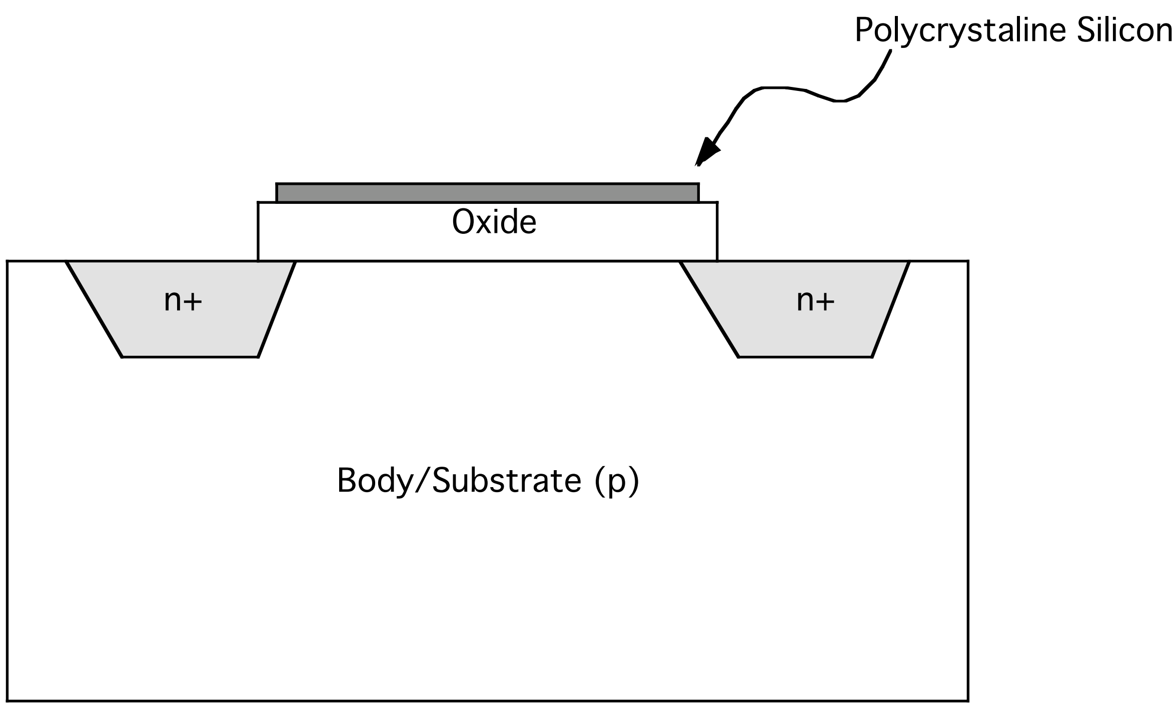
nMOS Transistor



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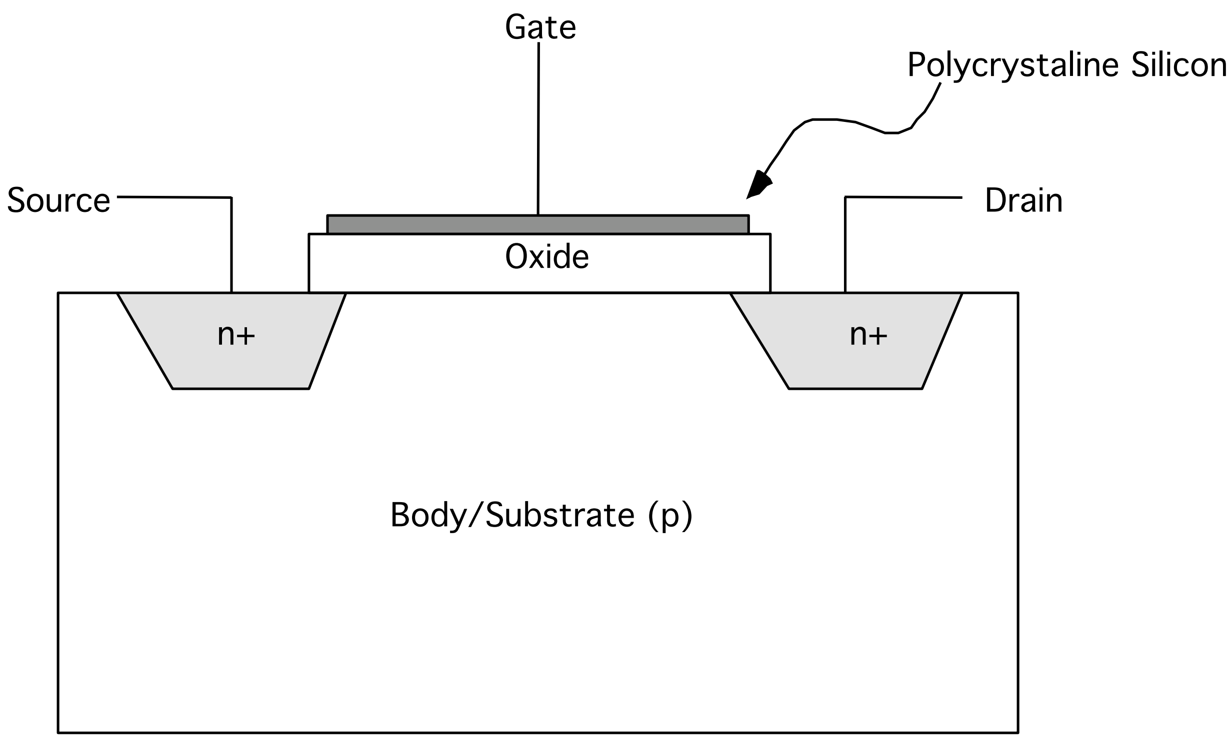
nMOS Transistor



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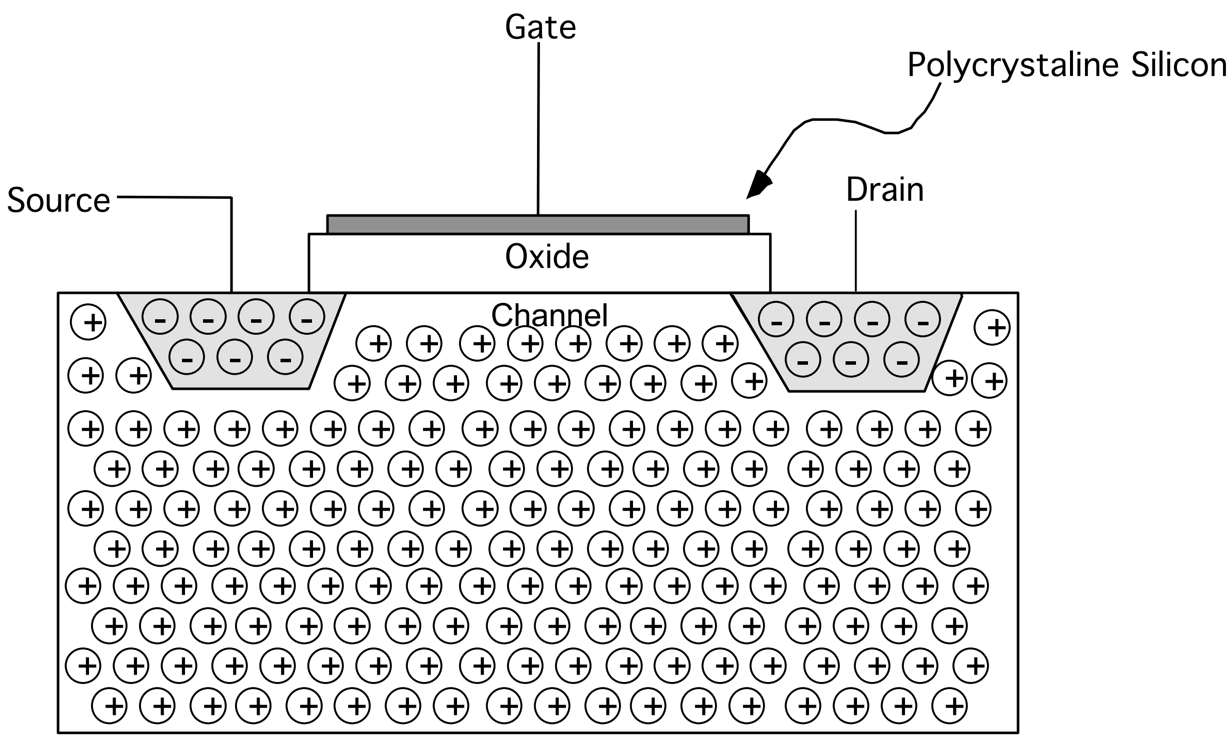
nMOS Transistor



Accumulation Mode

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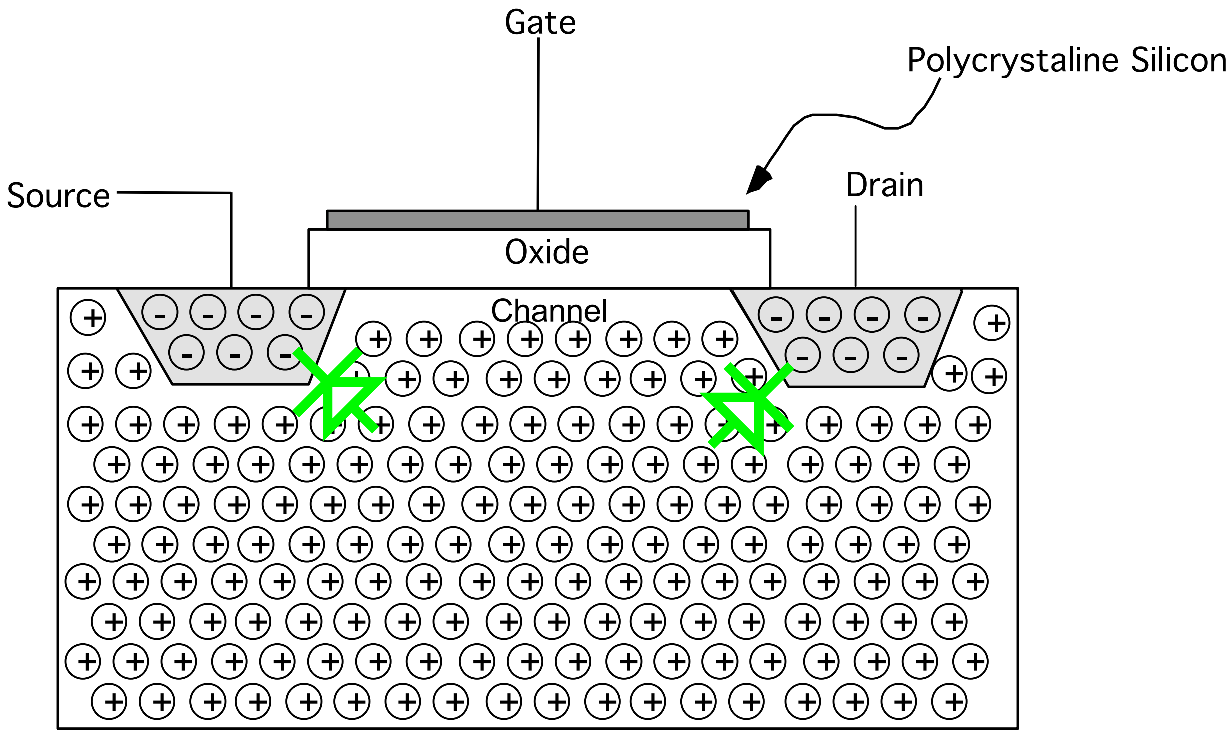
nMOS Transistor



Accumulation Mode

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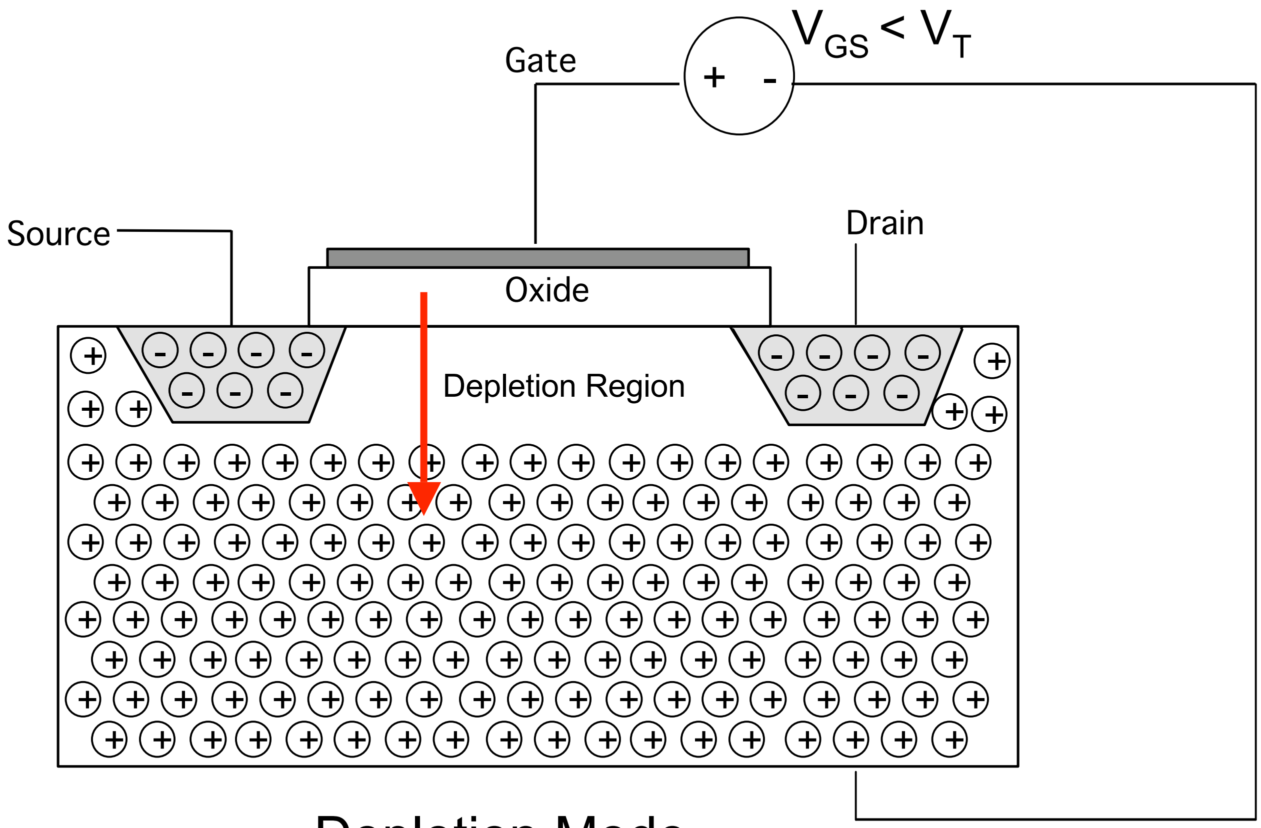
nMOS Transistor



Depletion Mode

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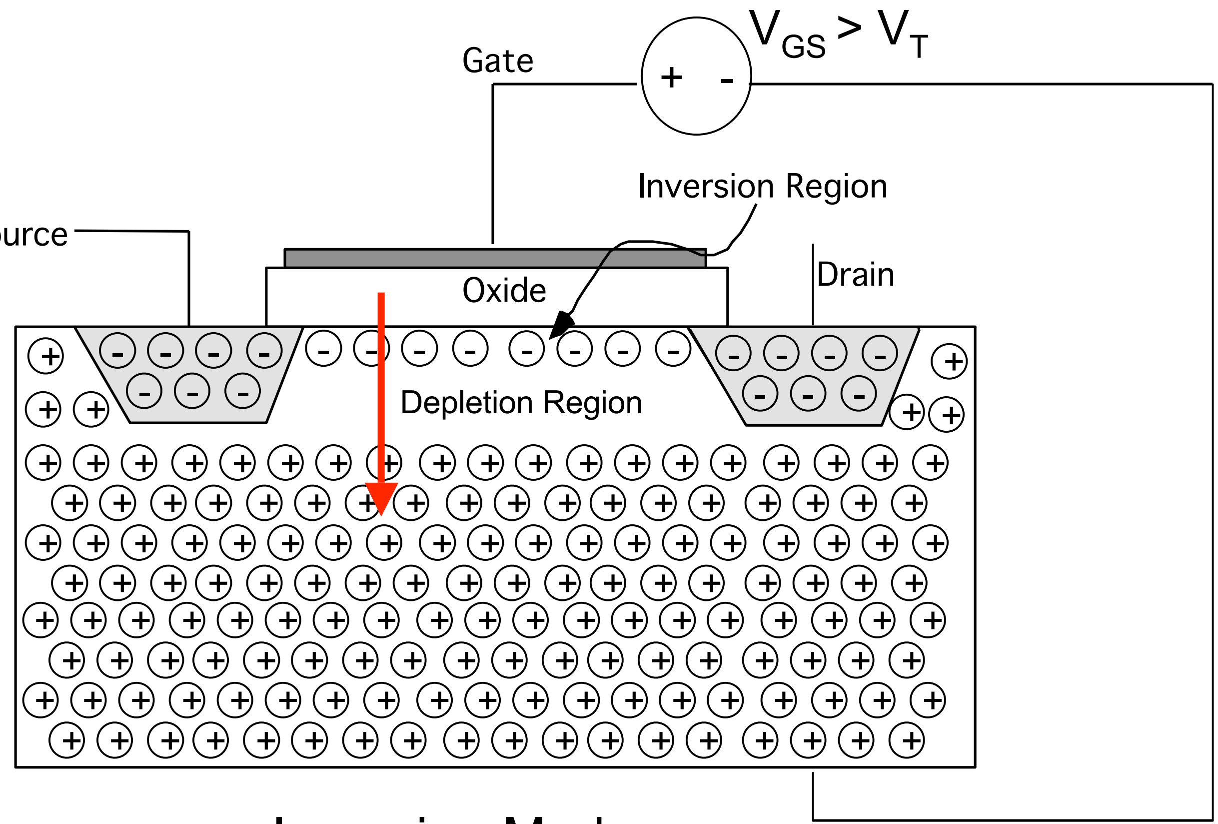
nMOS Transistor



Inversion Mode

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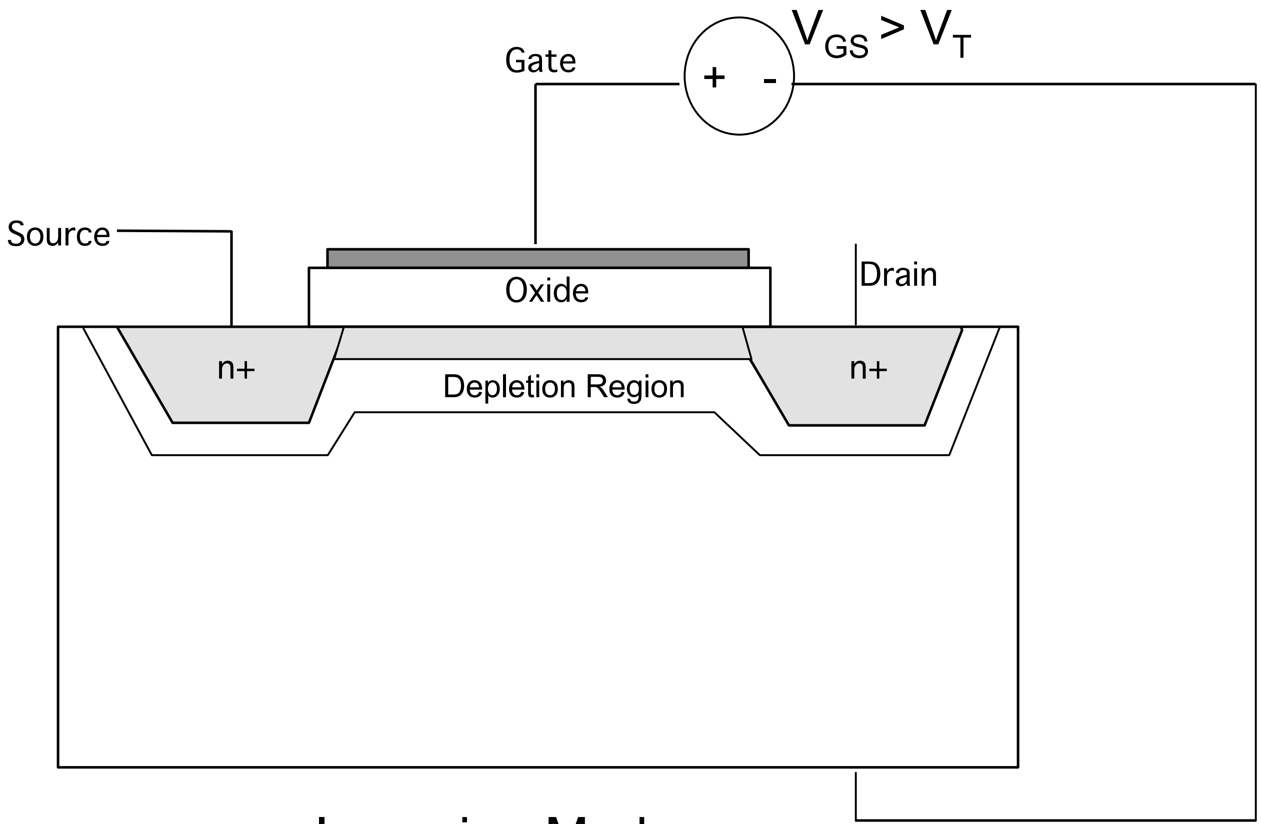
nMOS Transistor



Inversion Mode

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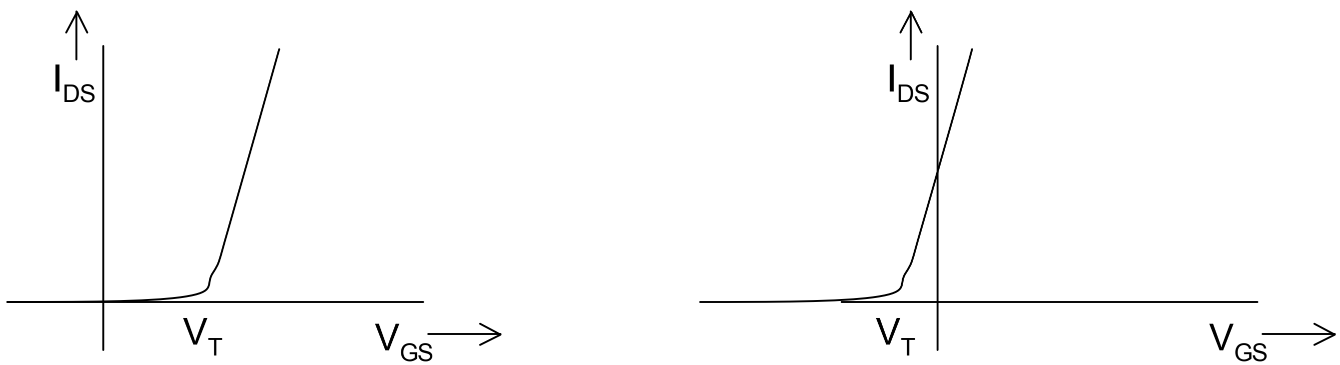
nMOS Transistor



Enhancement-mode

Depletion-mode

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Threshold Voltage

- Dependent on
  - Gate conductor material
  - Gate insulator material
  - Channel Doping
  - Voltage difference between source and body

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Threshold Voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right)$$

- Threshold voltage is usually arrived at empirically
- γ is the body-effect coefficient and controls the impact of the source to bulk voltage
- ϕ_F is the Fermi potential and is dependent on doping levels

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{N_i}\right)$$

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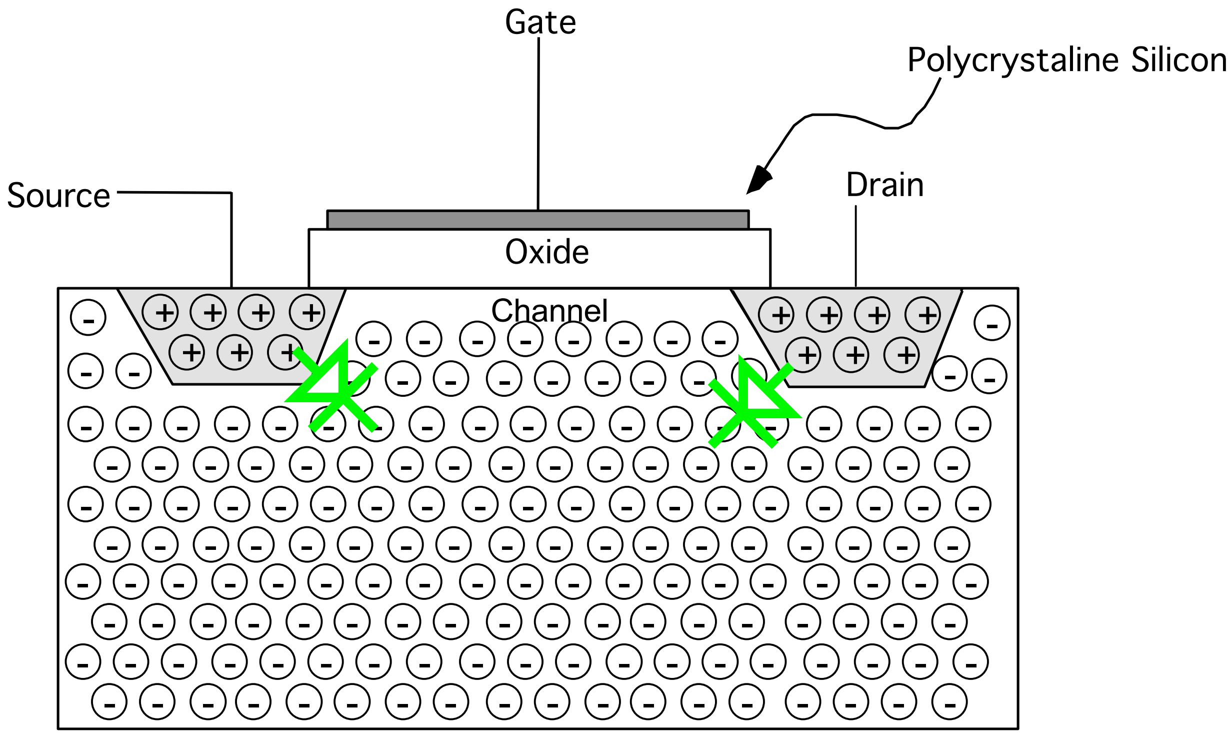
pMOS Transistor



Accumulation Mode

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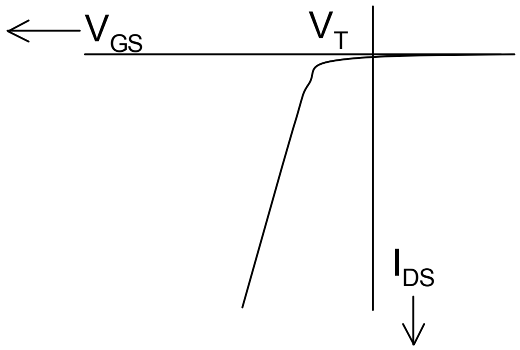
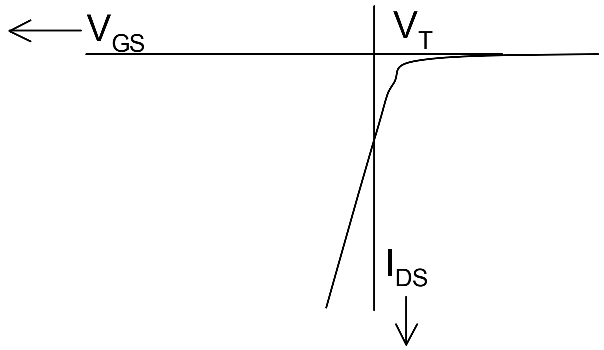
pMOS Transistor



Enhancement-mode



Depletion-mode

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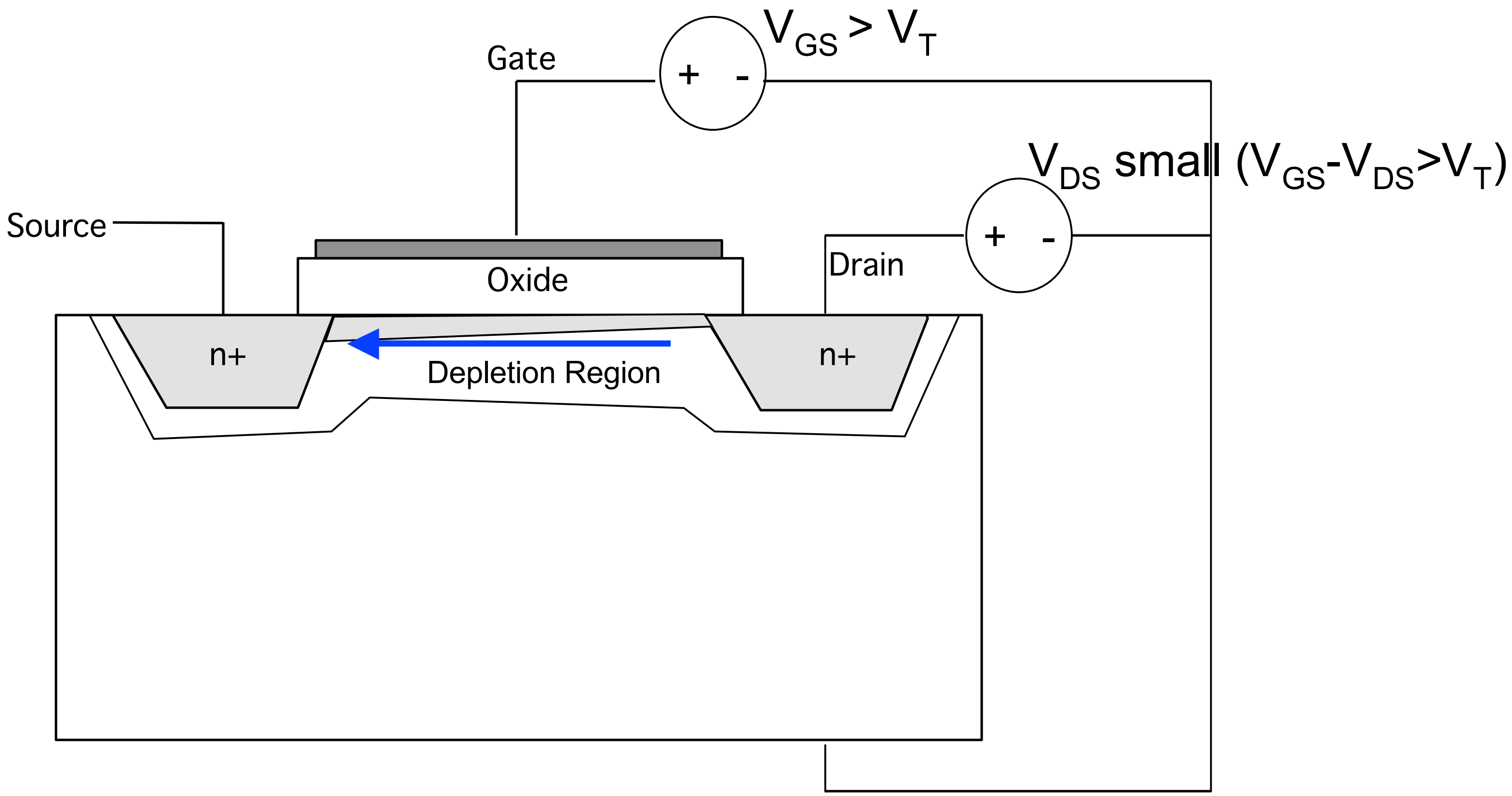
nMOS Transistor



Linear or Nonsaturated Mode

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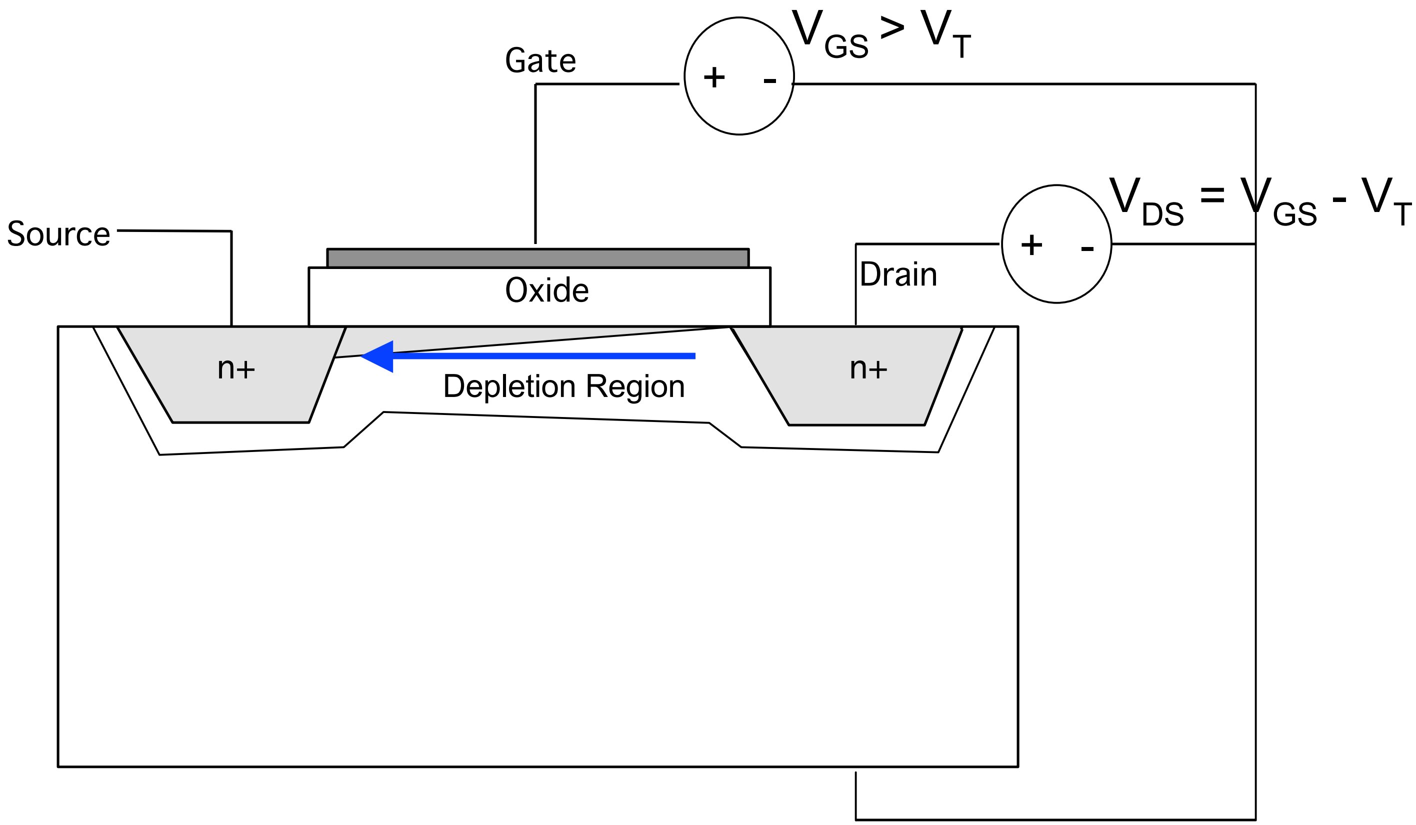
nMOS Transistor



Linear or Nonsaturated Mode

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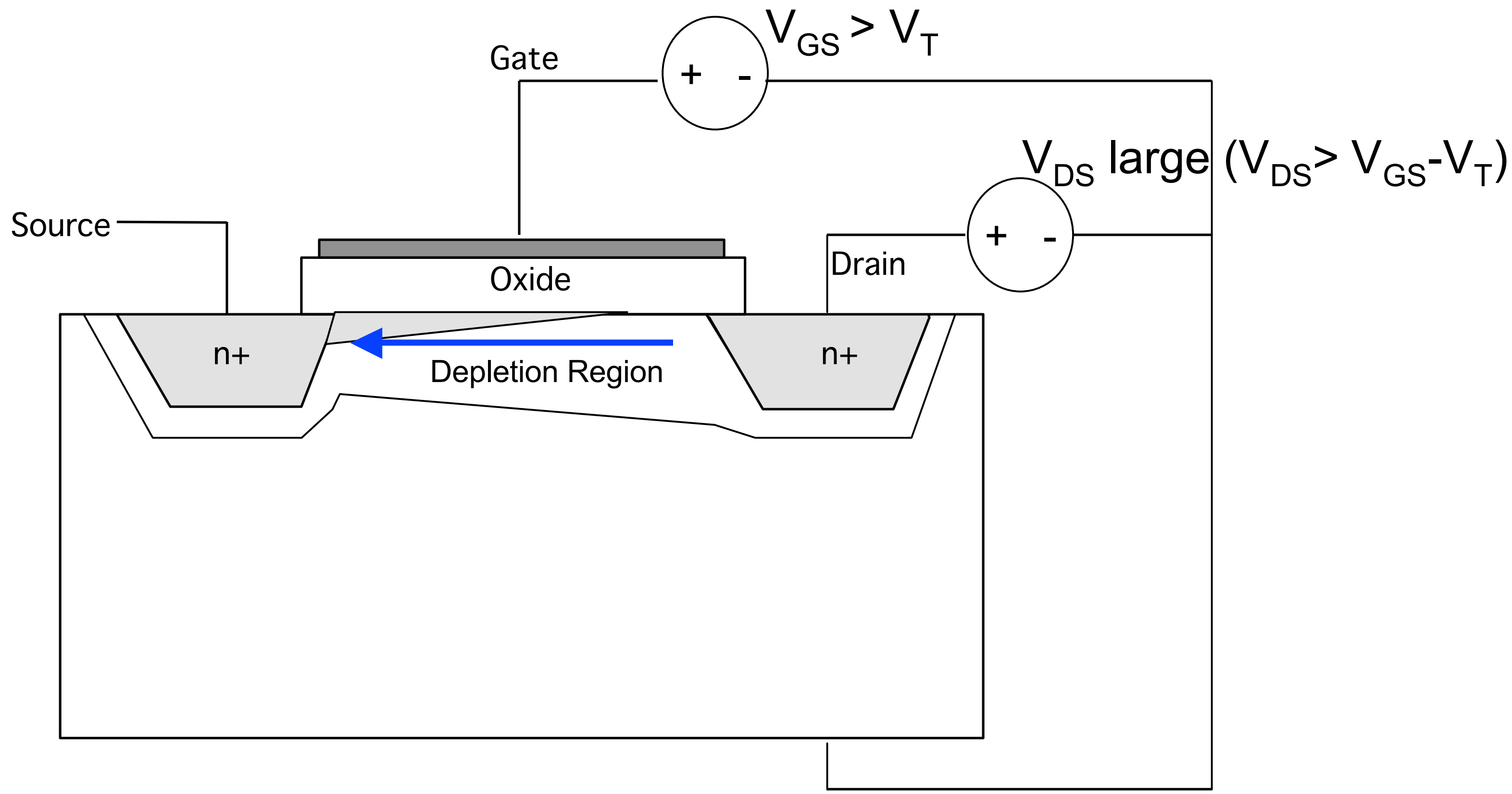
nMOS Transistor



Saturated Mode

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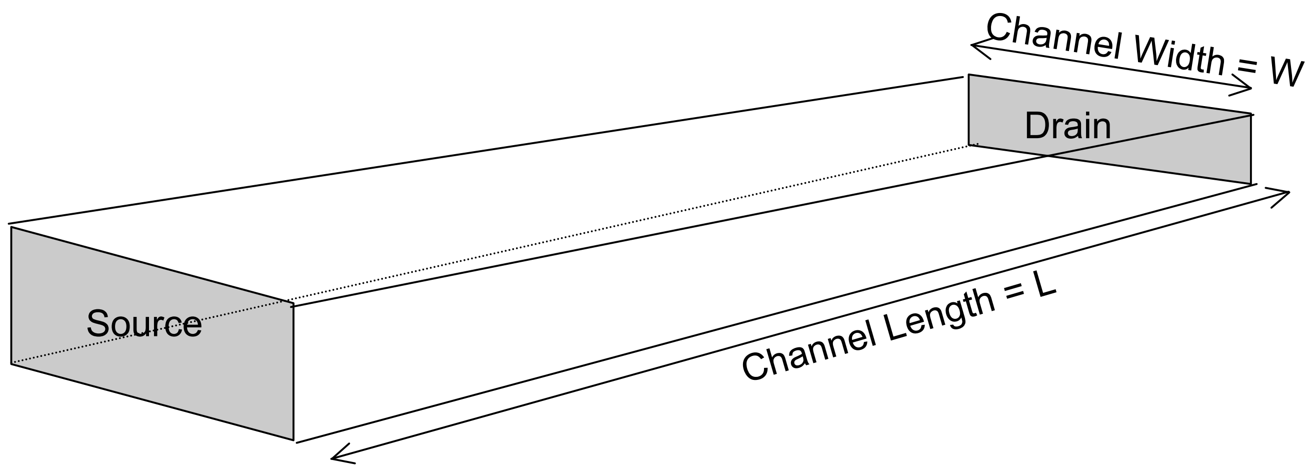
MOS Transistor Parameters



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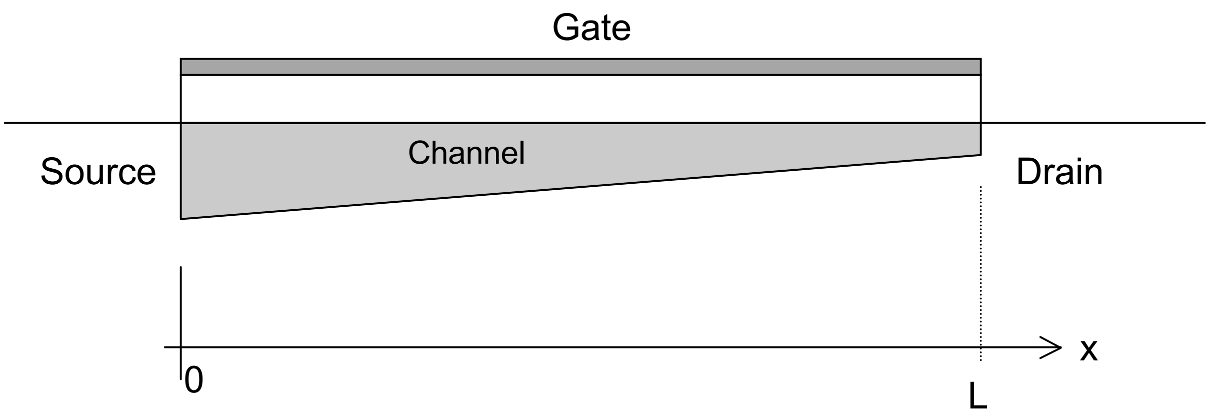
MOS Transistor Characteristics



- Linear Mode
- Assume both $V_{GS} > V_T$ and $V_{GD} > V_T$
- Assume that V_T is constant for x in [0:L]
- $V(0) = 0$ and $V(L) = V_{DS}$

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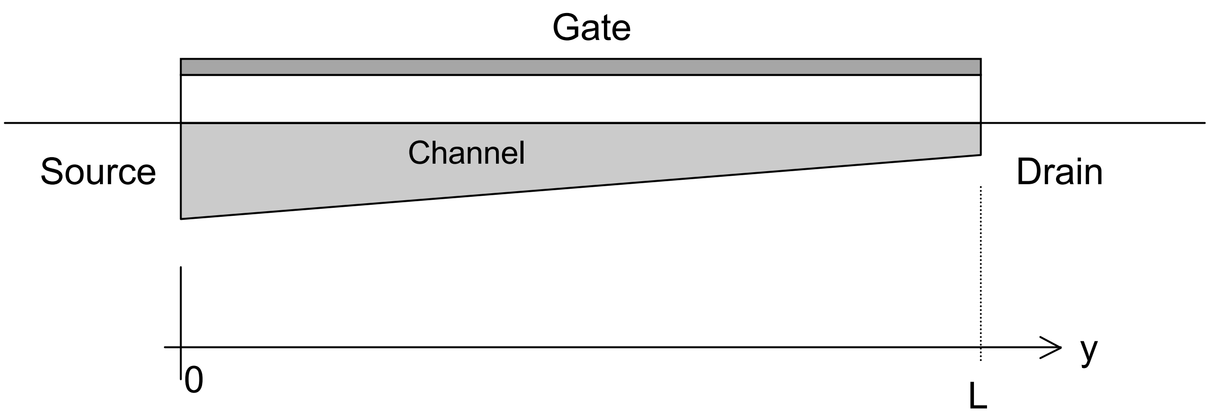
MOS Transistor Characteristics



- Mobile electron charge

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T]$$

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MOS Transistor Characteristics

- Current is product of carrier drift velocity and availabe charge

$$I_{DS} = -\upsilon(x) Q_i(x) W$$

$$I_{DS} = -\mu_n \frac{dV}{dx} Q_i(x) W$$

$$I_{DS} dx = -W \mu_n Q_i(x) dV$$

- Integrating along channel

$$\int_0^L I_{DS} dx = -W \mu_n \int_0^{V_{DS}} Q_i(x) dV$$

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MOS Transistor Characteristics

$$\int_0^L I_{DS} dx = -W\mu_n \int_0^{V_{DS}} Q_i(x) dV$$

$$I_{DS} L = W\mu_n \int_0^{V_{DS}} C_{ox}\left[V_{GS} - V(x) - V_T\right] dV$$

$$I_{DS} L = W\mu_n C_{ox}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_{DS} = k_n\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- k_n is the gain factor and is dependent on the transconductance ($\mu_n C_{ox}$) and the ratio between *W* and *L*.

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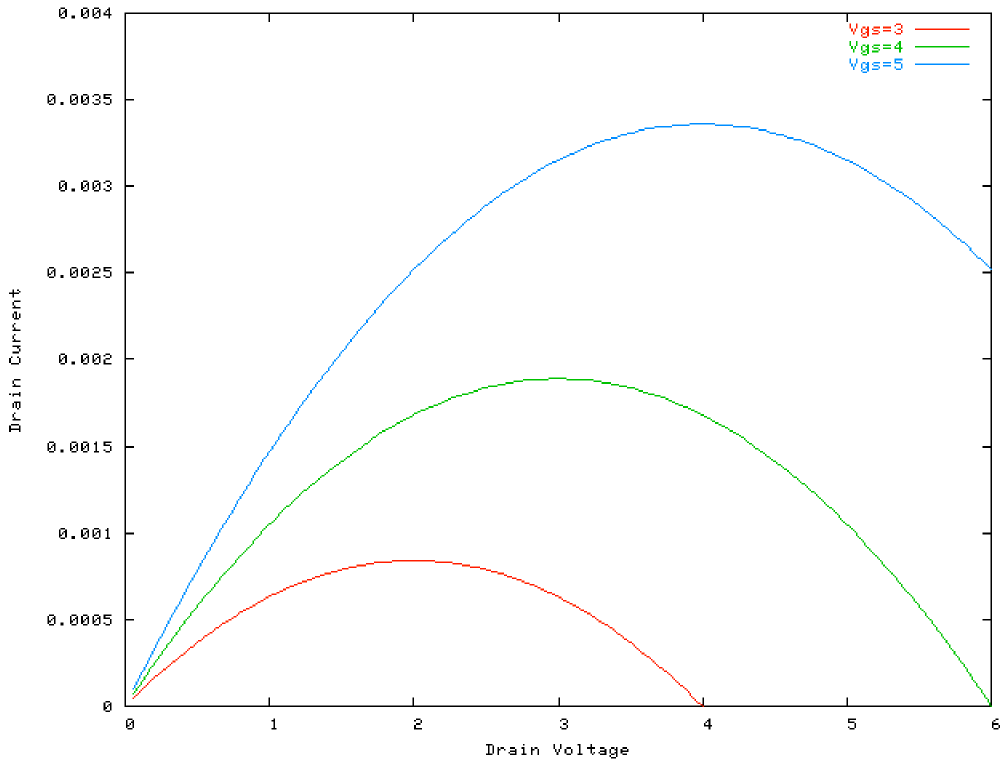
Example

- $\mu_n = 600\ cm^2/V\ s$
- $C_{ox} = 7 \times 10^{-8}\ F/cm^2$
- $W = 20\ \mu m$
- $L = 2\ \mu m$
- $k_n = \mu_n C_{ox} W/L = 0.42\ mA/V^2$

MOS Transistor



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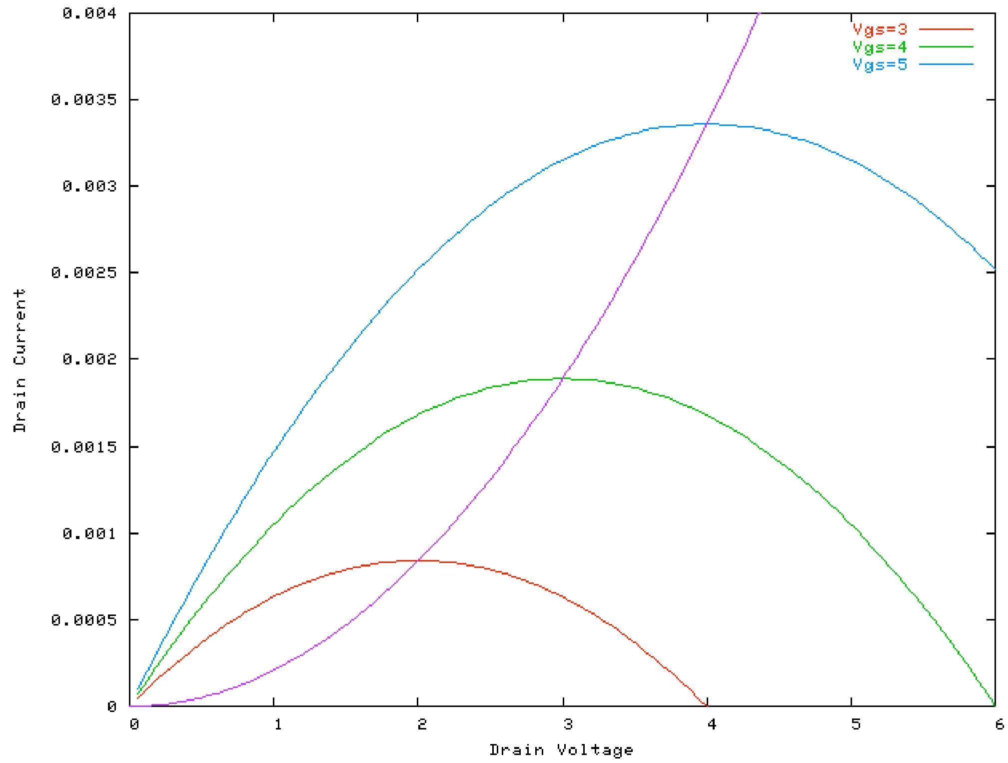
MOS Transistor



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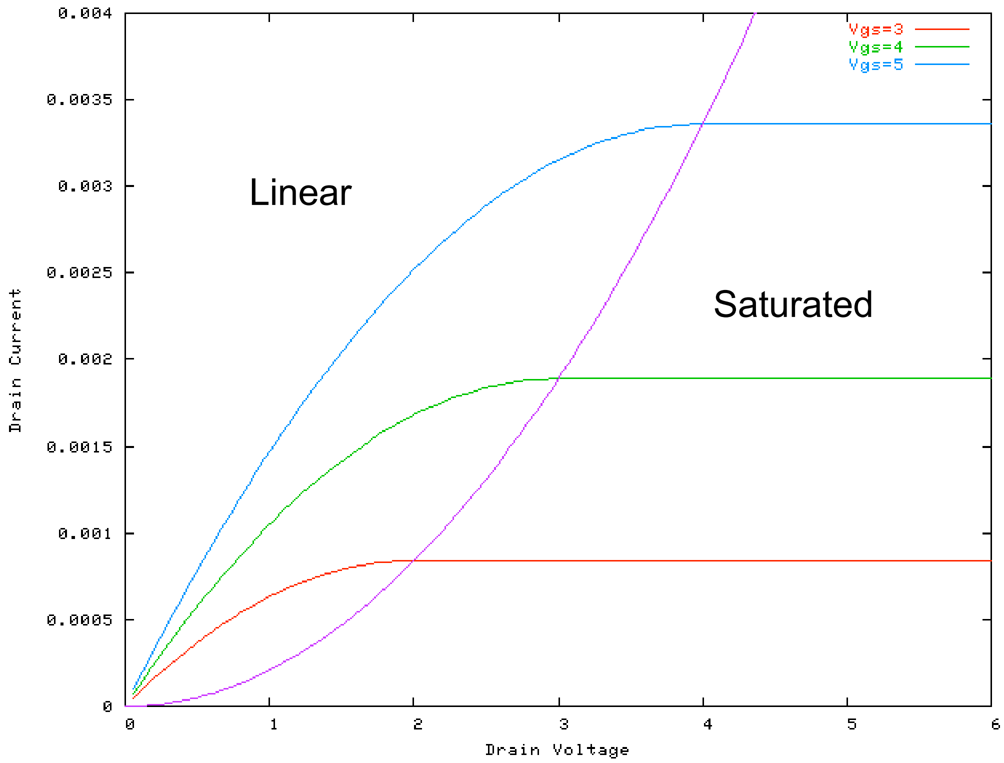
MOS Transistor



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MOS Transistor

- Cutoff region ($V_{GS}<V_T$)

$$I_{DS} = 0$$

- Linear region ($V_{GS}>V_T$, $V_{DS}<V_{GS}-V_T$)

$$I_{DS} = k_n\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Saturated region ($V_{GS}>V_T$, $V_{DS}>V_{GS}-V_T$)

$$I_{DS} = k_n\frac{(V_{GS} - V_T)^2}{2}$$

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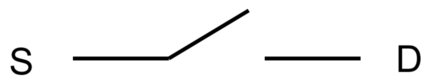
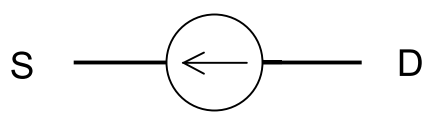
MOS Transistor

- Cutoff region ($V_{GS}<V_T$)



- Linear region ($V_{GS}>V_T$, $V_{DS}<V_{GS}-V_T$)

- Saturated region ($V_{GS}>V_T$, $V_{DS}>V_{GS}-V_T$)



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MOS Transistor Secondary Effects

- Body effect
- Channel-length modulation
- Drain punchthrough
- Impact ionization
- Velocity Saturation

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Body effect

- We assumed that $V_{SB}=0$ - I.e. the source potential equals the substrate potential
- In certain situations, this assumption is not true
- Has the effect of raising the threshold voltage

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Channel-Length Modulation

- We previously assumed a constant L
- In reality, when $V_{DS} > (V_{GS}-V_T)$, the channel is pinched off and the effective channel length is reduced.
- Pinch off length is proportional to the square root of $V_{GS}-V_T$
- Net effect is that I_{DS} is not constant in the saturated region.

MOS Transistor

- Cutoff region ($V_{GS}<V_T$)

$$I_{DS} = 0$$

- Linear region ($V_{GS}>V_T$, $V_{DS}<V_{GS}-V_T$)

$$I_{DS} = k_n\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Saturated region ($V_{GS}>V_T$, $V_{DS}>V_{GS}-V_T$)

$$I_{DS} = k_n\frac{(V_{GS} - V_T)^2}{2}(1 + \lambda V_{DS})$$

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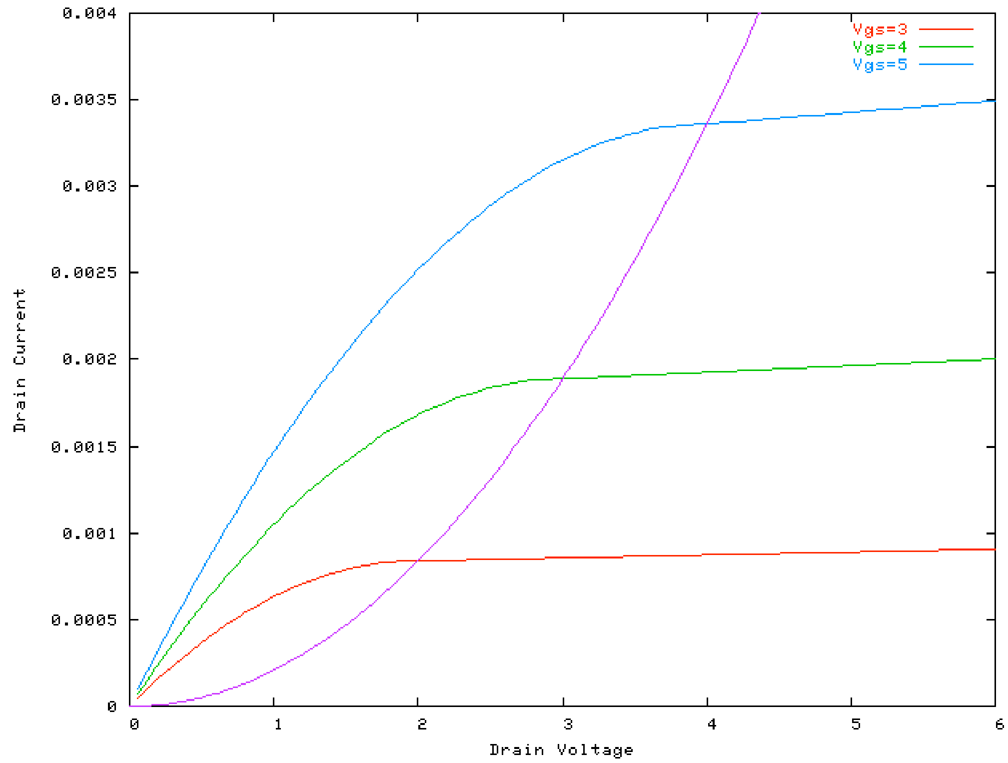
Channel-Length Modulation



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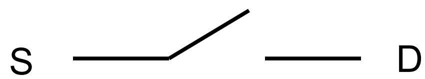
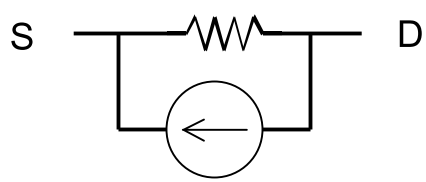
MOS Transistor

- Cutoff region ($V_{GS}<V_T$)



- Linear region ($V_{GS}>V_T$, $V_{DS}<V_{GS}-V_T$)

- Saturated region ($V_{GS}>V_T$, $V_{DS}>V_{GS}-V_T$)



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Drain punch-through

- For very large V_{DS}, the depletion region grows from the drain to the source
- Current flow increases rapidly
- V_{GS} has no control on the current
- Potentially damaging to transistor
- Short channel effect

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Impact ionization

- At small gate lengths, electric field becomes more pronounced
- Electrons get excited with enough energy to cause a substrate current
- This causes change of transistor parameters - threshold voltage, current flow, etc.

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Velocity Saturation

- Assumption was that carrier velocity is proportional to electric field
- When channel is small, and the voltage is large, the velocity can saturate

$$\upsilon = \begin{cases} \mu_n \xi & \xi < \xi_c \\ \mu_n \xi_c & \xi > \xi_c \end{cases}$$

ξ_c is value of electric field at which velocity saturates

MOS Transistor

- Cutoff region ($V_{GS}<V_T$)

$$I_{DS} = 0$$

- Linear region ($V_{GS}>V_T$, $V_{DS}<V_{GS}-V_T$)

$$I_{DS} = k_n\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- Saturated region ($V_{GS}>V_T$, $V_{DS}>V_{GS}-V_T$)

$$I_{DS} = k_n\left[\left(V_{GS} - V_T\right)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

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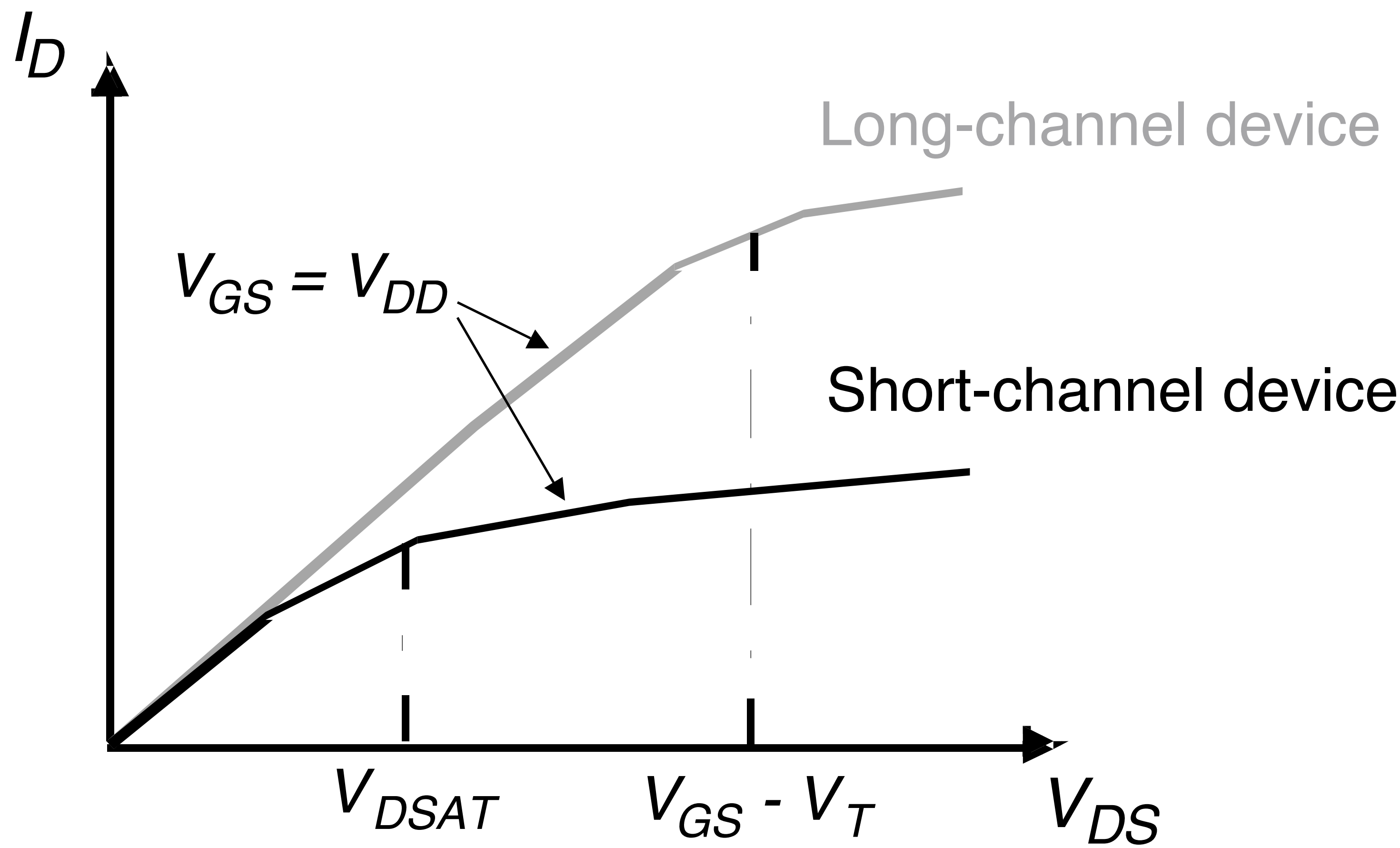
Velocity Saturation



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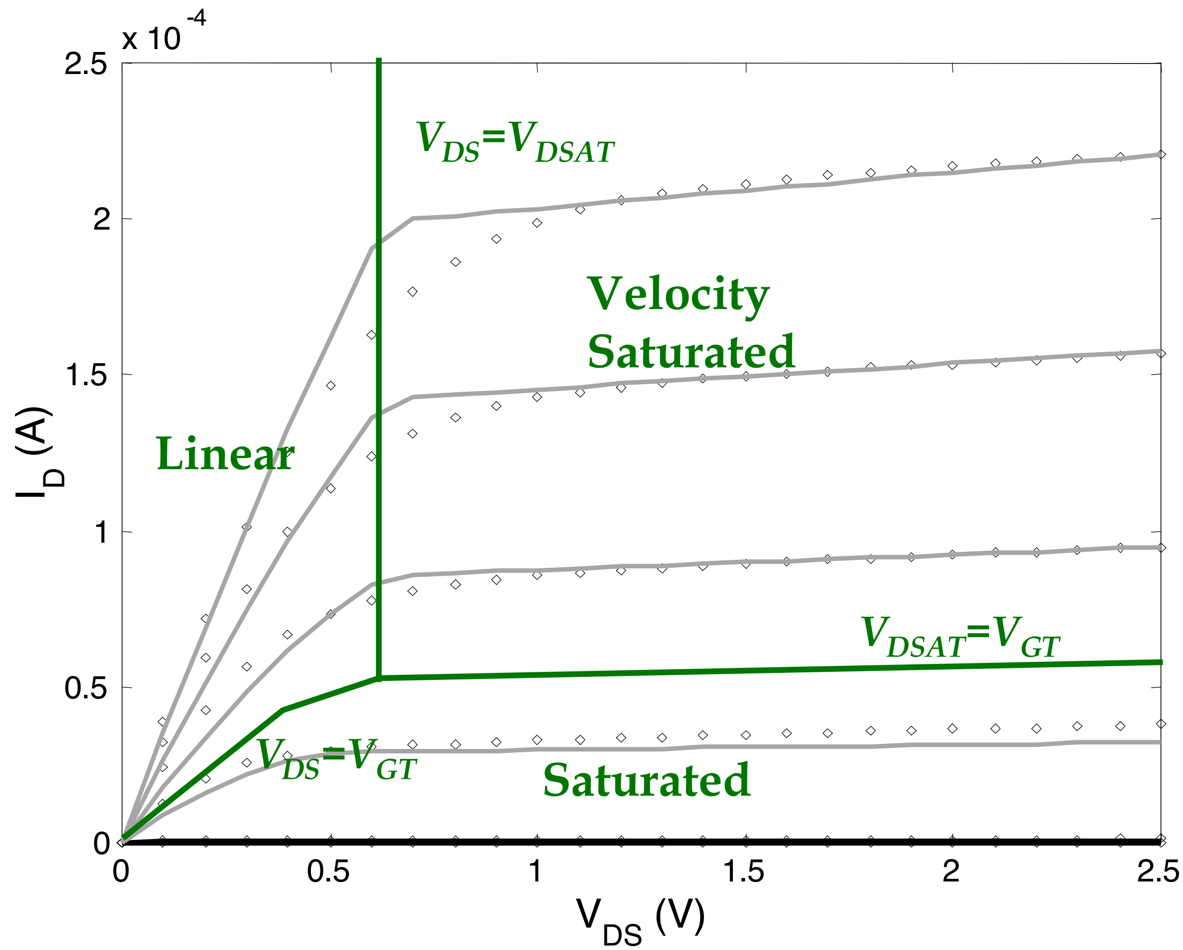
Velocity Saturation



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MOS Gain Characteristics

- Transconductance $g_m = \frac{dI_{DS}}{dV_{GS}}$
  - Cutoff region

$$g_m = 0$$

  - Linear region

$$g_m = k_n V_{DS}$$

  - Saturated region

$$g_m = k_n \left(V_{GS} - V_T\right)$$

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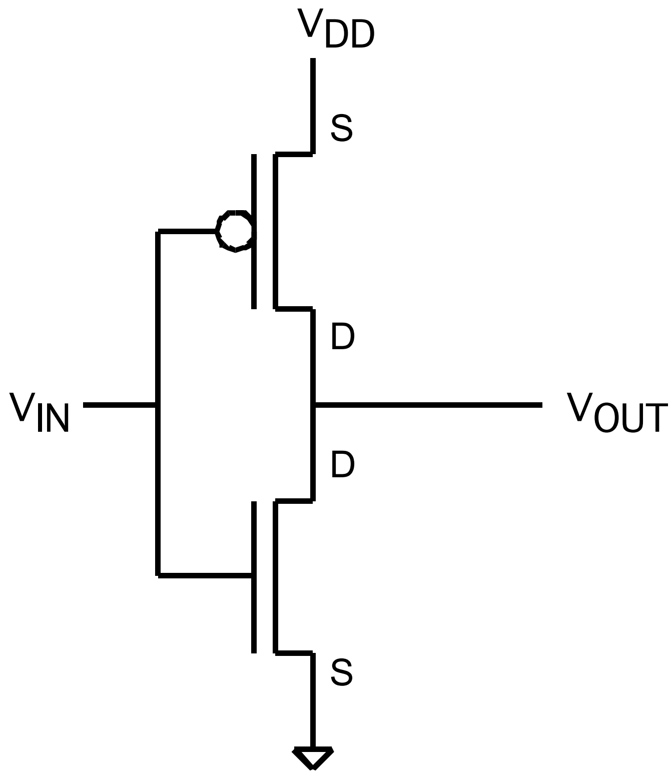
CMOS Characteristics



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nMOS Transistor

- Cutoff region ($V_{GSn}>V_{Tn}$)

$$I_{DSn} = 0$$

- Linear region ($V_{GSn}<V_{Tn}$, $V_{DSn}>V_{GSn}-V_{Tn}$)

$$I_{DSn} = -k_n\left[\left(V_{GSn} - V_{Tn}\right)V_{DSn} - \frac{V_{DSn}^2}{2}\right]$$

- Saturated region ($V_{GSn}<V_{Tn}$, $V_{DSn}<V_{GSn}-V_{Tn}$)

$$I_{DSn} = -k_n\frac{\left(V_{GSn} - V_{Tn}\right)^2}{2}\left(1+\lambda V_{DSn}\right)$$

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pMOS Transistor

- Cutoff region ($V_{GSp}>V_{Tp}$)

$$I_{DSp} = 0$$

- Linear region ($V_{GSp}<V_{Tp}$, $V_{DSp}>V_{GSp}-V_{Tp}$)

$$I_{DSp} = k_p\left[\left(V_{GSp} - V_{Tp}\right)V_{DSp} - \frac{V_{DSp}^2}{2}\right]$$

- Saturated region ($V_{GSp}<V_{Tp}$, $V_{DSp}<V_{GSp}-V_{Tp}$)

$$I_{DSp} = k_p\frac{\left(V_{GSp} - V_{Tp}\right)^2}{2}\left(1 + \lambda V_{DSp}\right)$$

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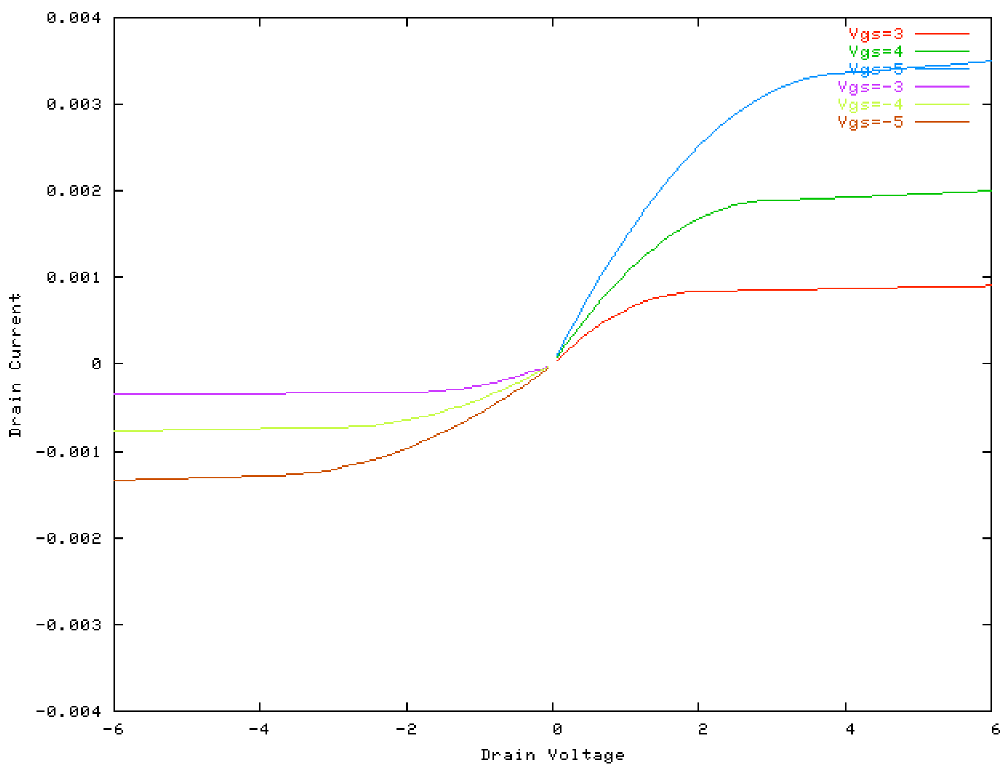
CMOS Inverter



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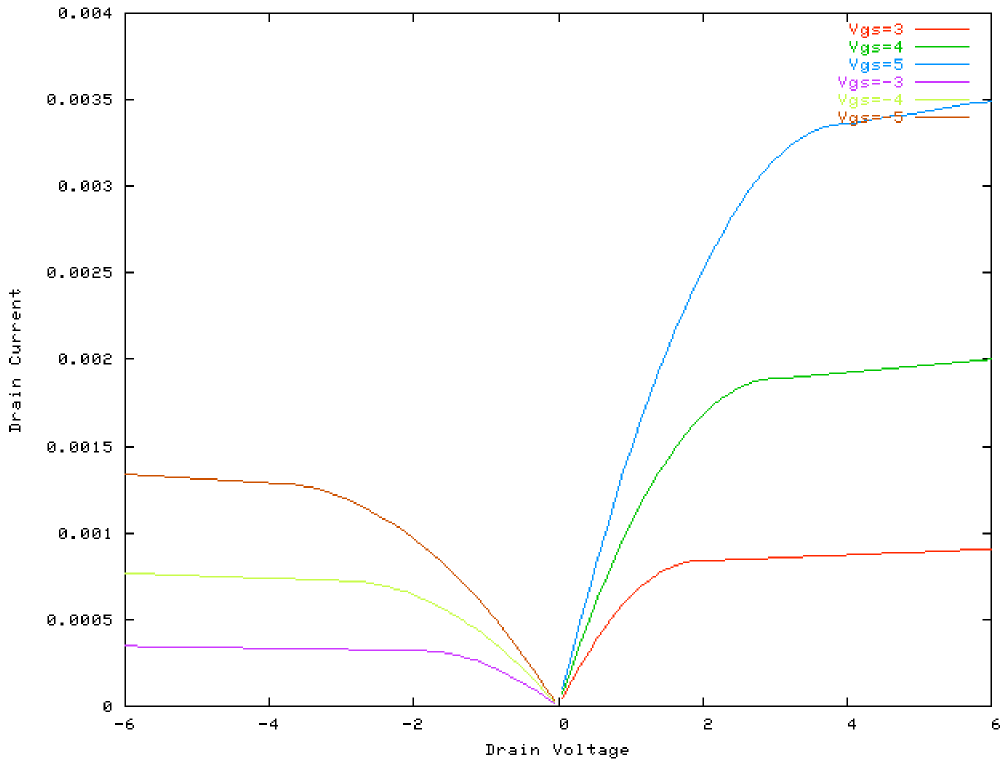
CMOS Inverter



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CMOS Inverter

$$V_{GSn} = V_{in}$$

$$V_{DSn} = V_{out}$$

$$V_{GSp} = V_{in} - V_{DD}$$

$$V_{DSp} = V_{out} - V_{DD}$$

$$V_{tn} \approx V_{tp}$$

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pMOS Transistor

- Cutoff region ($V_{in}>V_{DD}-V_T$)

$$I_{DSp}=0$$

- Linear region ($V_{in}<V_{DD}-V_T$, $V_{out}>V_{in}+V_T$)

$$I_{DS}=k_p\left[\left(V_{in}-V_{DD}+V_T\right)\left(V_{out}-V_{DD}\right)-\frac{\left(V_{out}-V_{DD}\right)^2}{2}\right]$$

- Saturated region ($V_{in}<V_{DD}-V_T$, $V_{out}<V_{in}+V_T$)

$$I_{DS}=k_p\frac{\left(V_{in}-V_{DD}+V_T\right)^2}{2}\left(1+\lambda\left(V_{out}-V_{DD}\right)\right)$$

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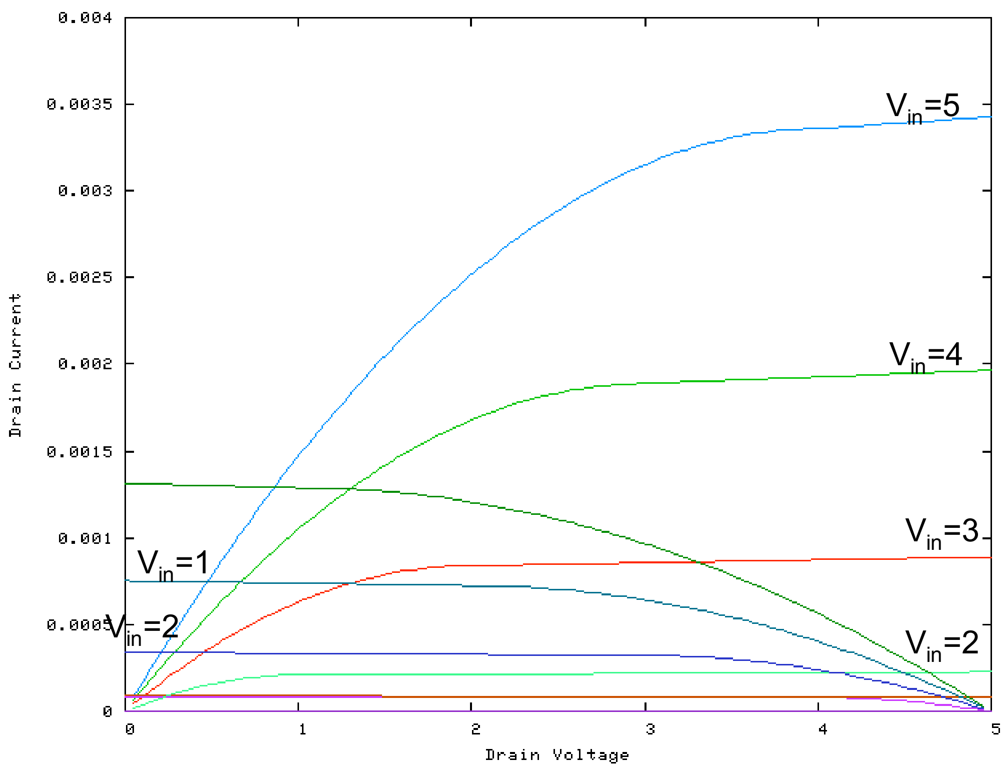
CMOS Inverter



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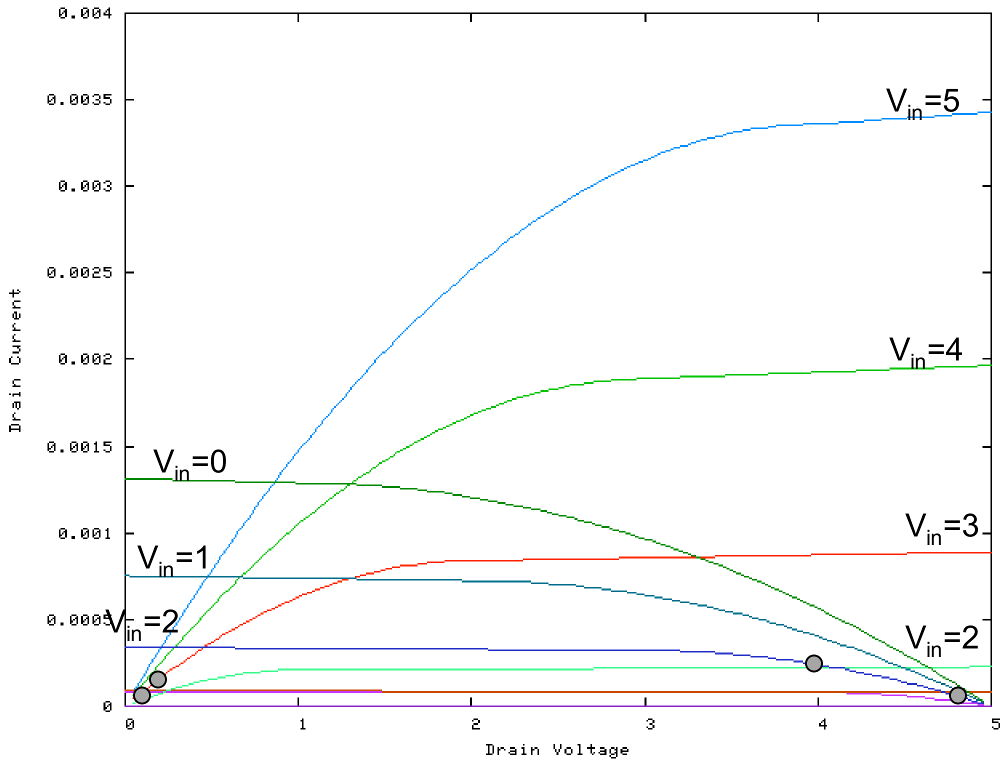
CMOS Inverter



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Next Class

- Noise Margin
- Static Load Inverters
- Read Chapter 5

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