VLSI Design and Simulation

Lecture 3

CMOS Inverters

Topics

- Inverter VTC
- Noise Margin
- Static Load Inverters

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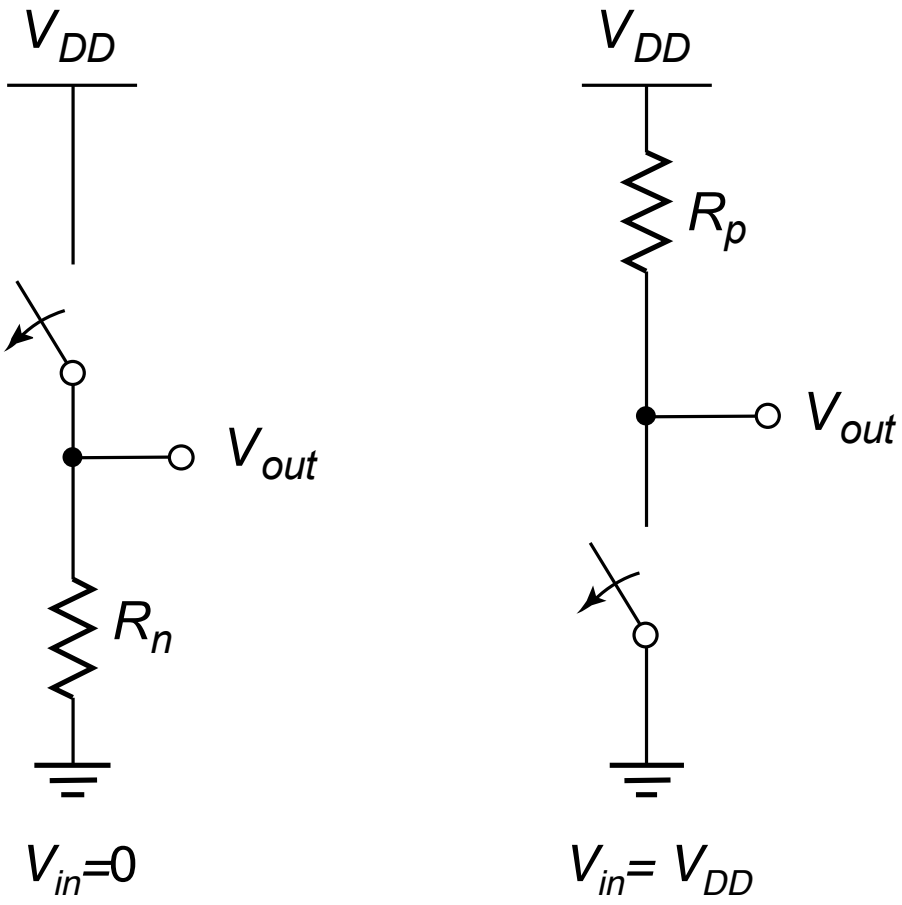
CMOS Inverter
First-Order DC Analysis



$V_{OL} = 0$
$V_{OH} = V_{DD}$

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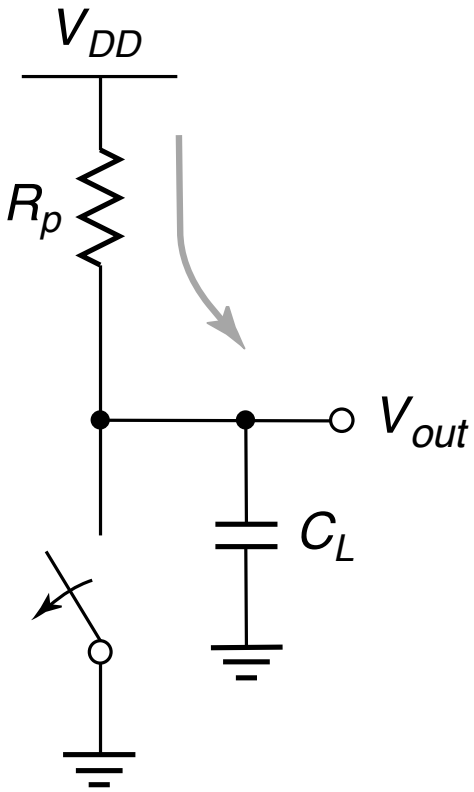
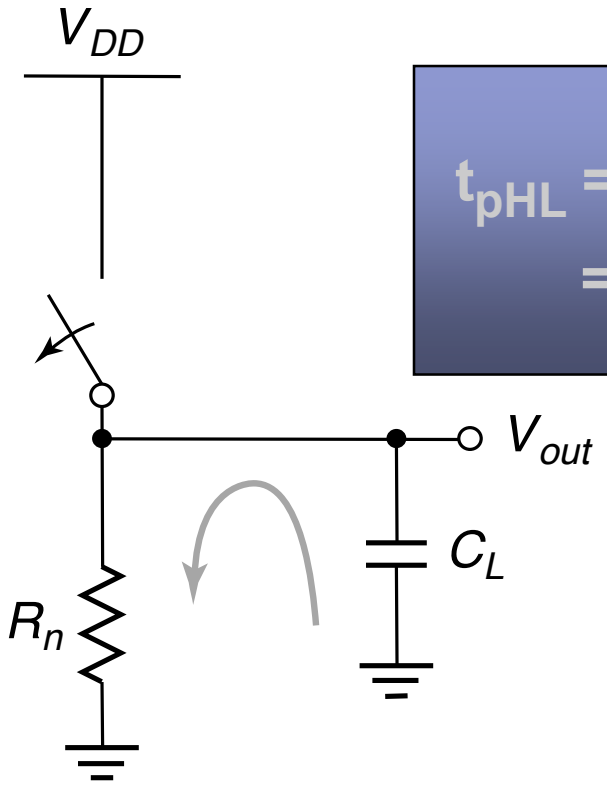
CMOS Inverter: Transient Response



(a) Low-to-high



(b) High-to-low

$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

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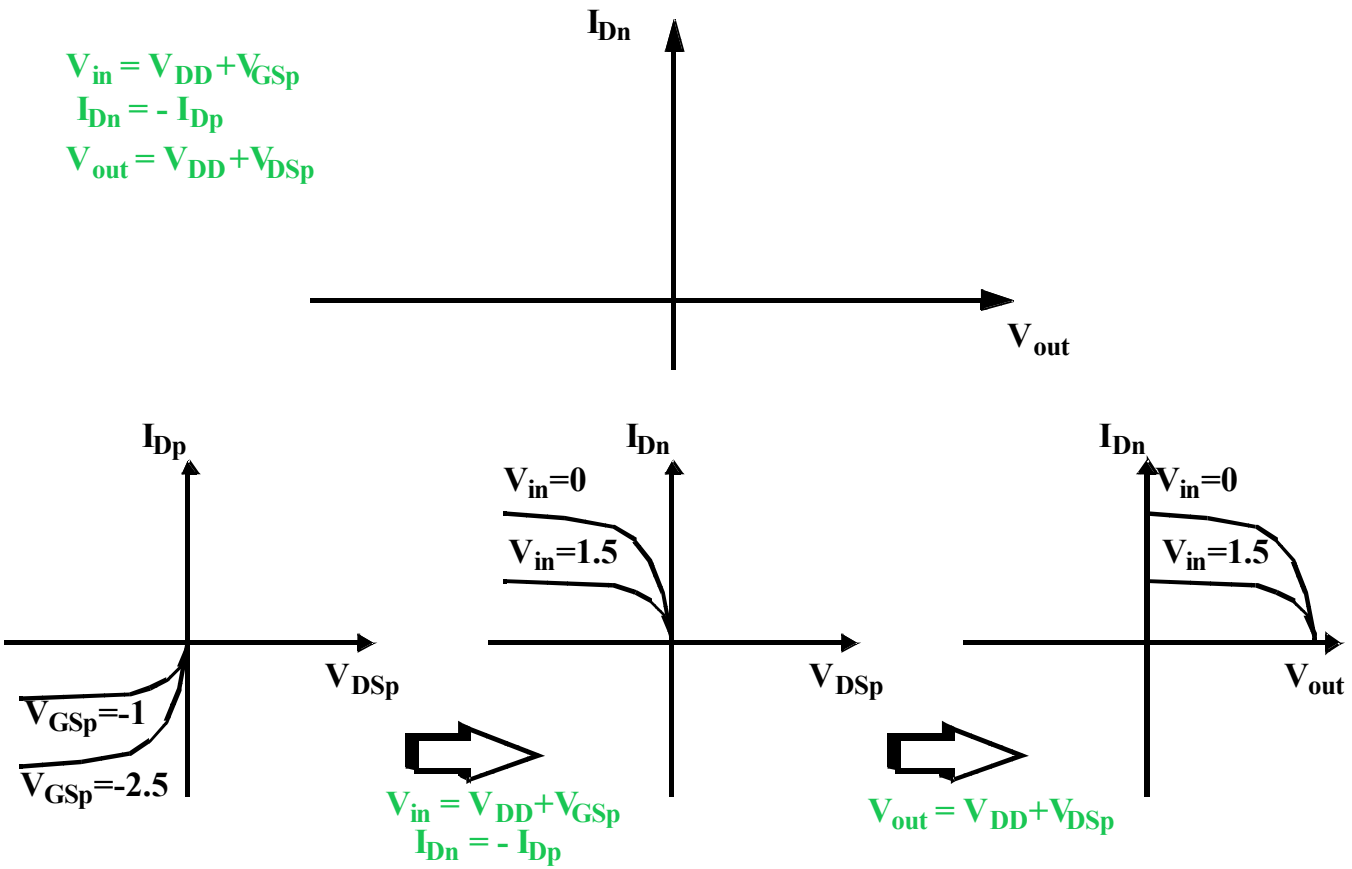
PMOS Load Lines



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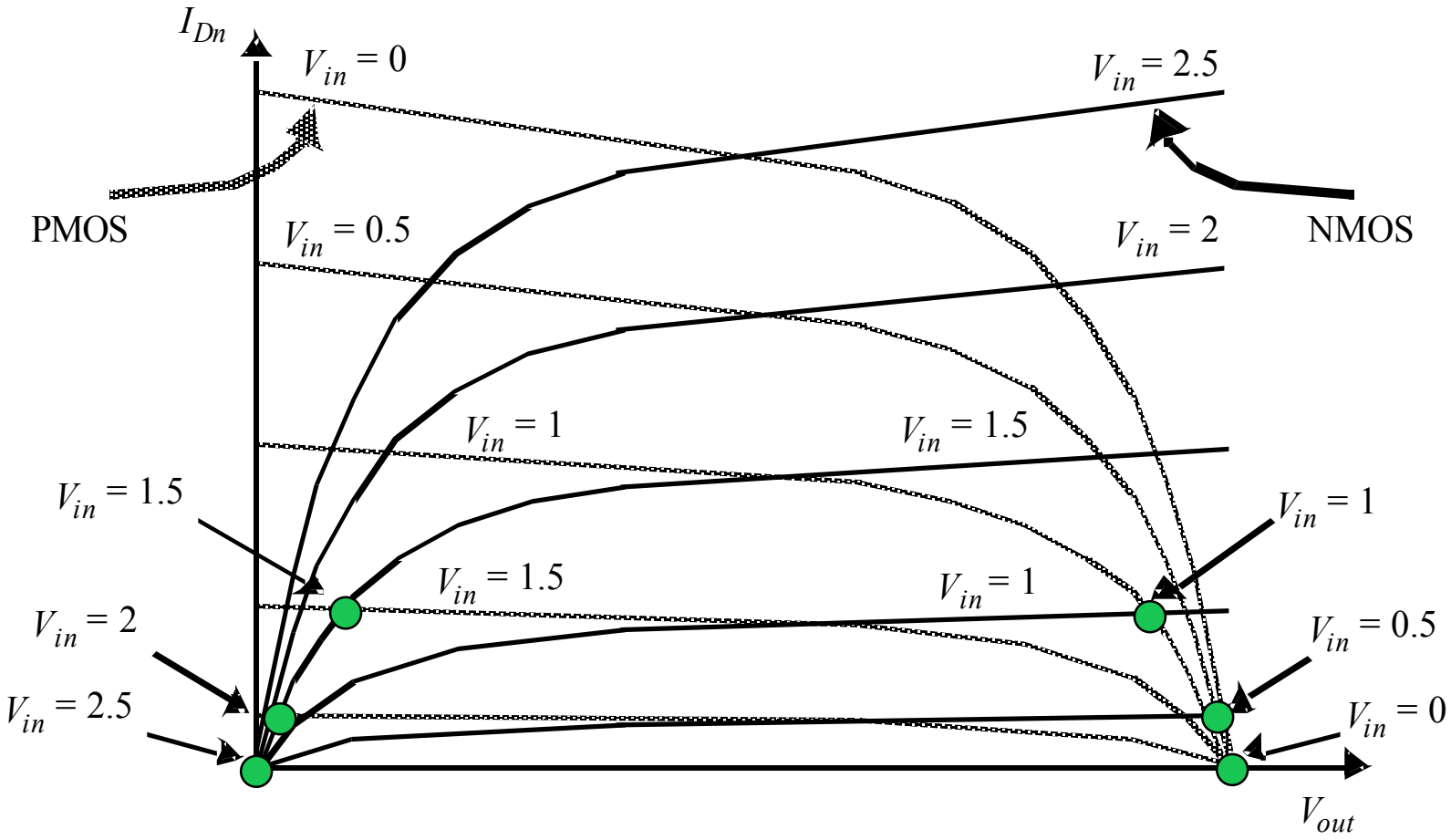
CMOS Inverter Load Characteristics



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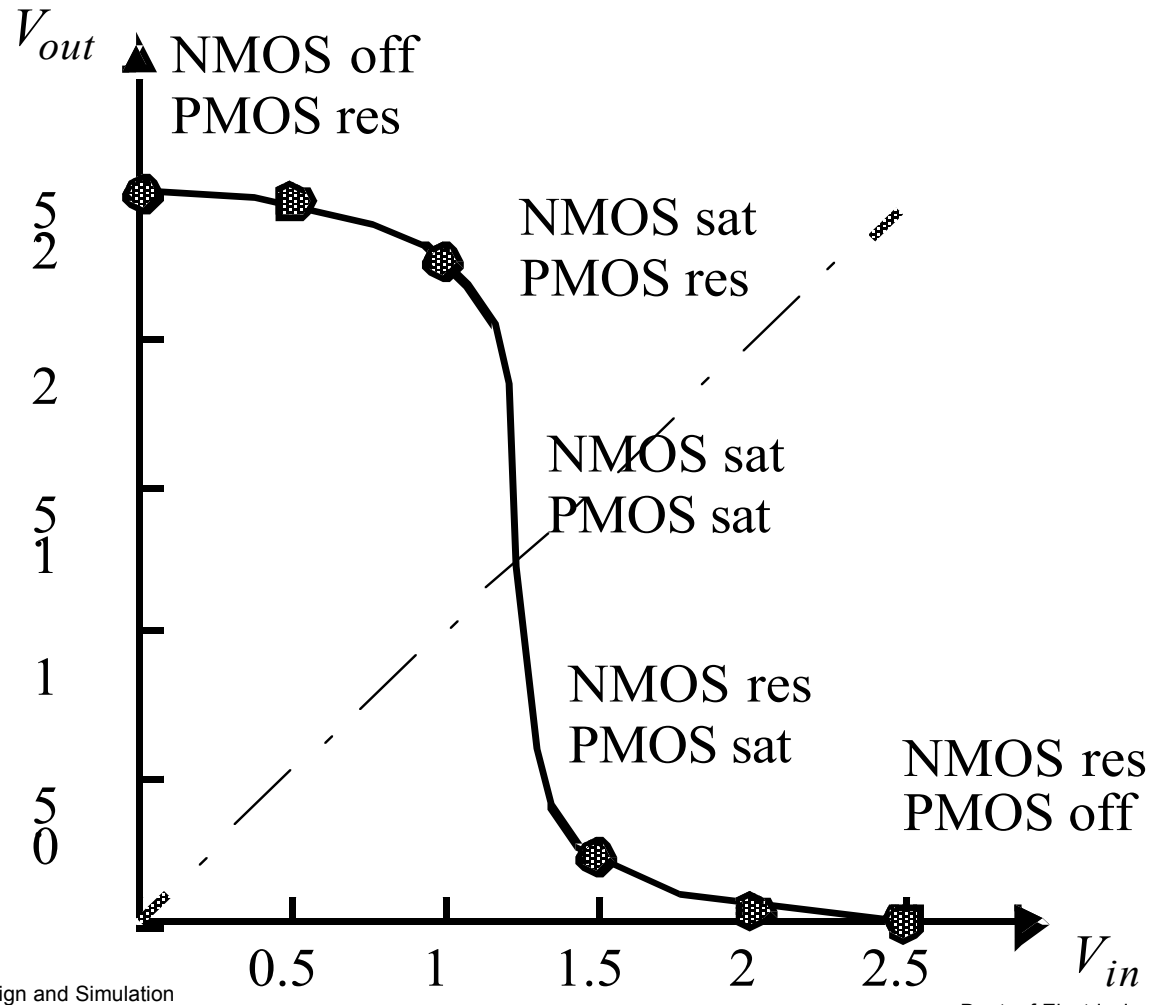
CMOS Inverter VTC



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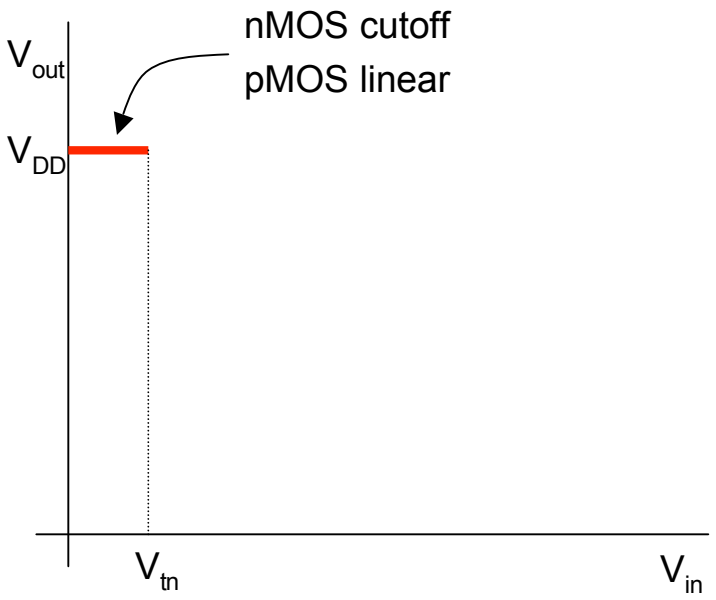
CMOS Inverter VTC



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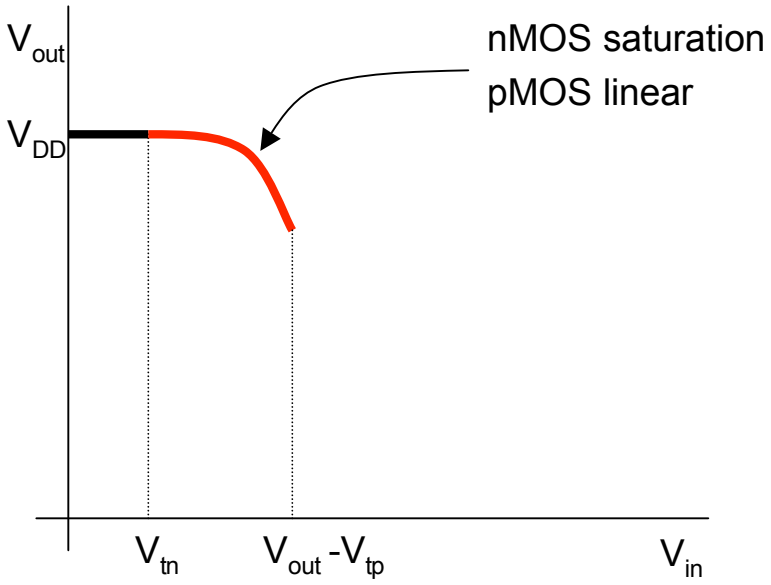
CMOS Inverter VTC



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CMOS Inverter VTC

- Set pMOS Linear I_{DS} equal to nMOS Saturation I_{DS}

$$k_n\left(\frac{(V_{in}-V_{tn})^2}{2}\right)=k_p\left((V_{in}-V_{DD}-V_{tp})(V_{out}-V_{DD})-\frac{(V_{out}-V_{DD})^2}{2}\right)$$

$$\frac{(V_{out}-V_{DD})^2}{2}-(V_{in}-V_{DD}-V_{tp})(V_{out}-V_{DD})+\frac{k_n}{k_p}\frac{(V_{in}-V_{tn})^2}{2}=0$$

$$(V_{out}-V_{DD})=(V_{in}-V_{DD}-V_{tp})+\sqrt{(V_{in}-V_{DD}-V_{tp})^2-\frac{k_n}{k_p}(V_{in}-V_{tn})^2}$$

$$V_{out}=(V_{in}-V_{tp})+\sqrt{(V_{in}-V_{DD}-V_{tp})^2-\frac{k_n}{k_p}(V_{in}-V_{tn})^2}$$

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CMOS Inverter VTC

- Short channel model

$$k_n V_{DSATn}\left(V_{in} - V_{tn} - \frac{V_{DSATn}}{2}\right) = k_p\left(\left(V_{in} - V_{DD} - V_{tp}\right)\left(V_{out} - V_{DD}\right) - \frac{\left(V_{out} - V_{DD}\right)^2}{2}\right)$$

$$\frac{\left(V_{out} - V_{DD}\right)^2}{2} - \left(V_{in} - V_{DD} - V_{tp}\right)\left(V_{out} - V_{DD}\right) + \frac{k_n}{k_p} V_{DSATn}\left(V_{in} - V_{tn} - \frac{V_{DSATn}}{2}\right) = 0$$

$$\left(V_{out} - V_{DD}\right) = \left(V_{in} - V_{DD} - V_{tp}\right) + \sqrt{\left(V_{in} - V_{DD} - V_{tp}\right)^2 - 2\frac{k_n}{k_p} V_{DSATn}\left(V_{in} - V_{tn} - \frac{V_{DSATn}}{2}\right)}$$

$$V_{out} = \left(V_{in} - V_{tp}\right) + \sqrt{\left(V_{in} - V_{DD} - V_{tp}\right)^2 - 2\frac{k_n}{k_p} V_{DSATn}\left(V_{in} - V_{tn} - \frac{V_{DSATn}}{2}\right)}$$

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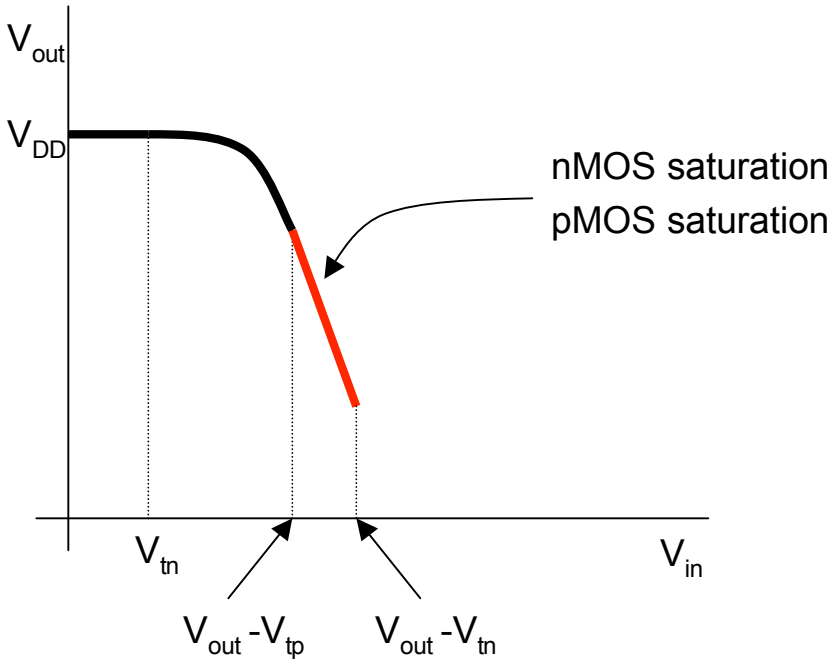
CMOS Inverter VTC



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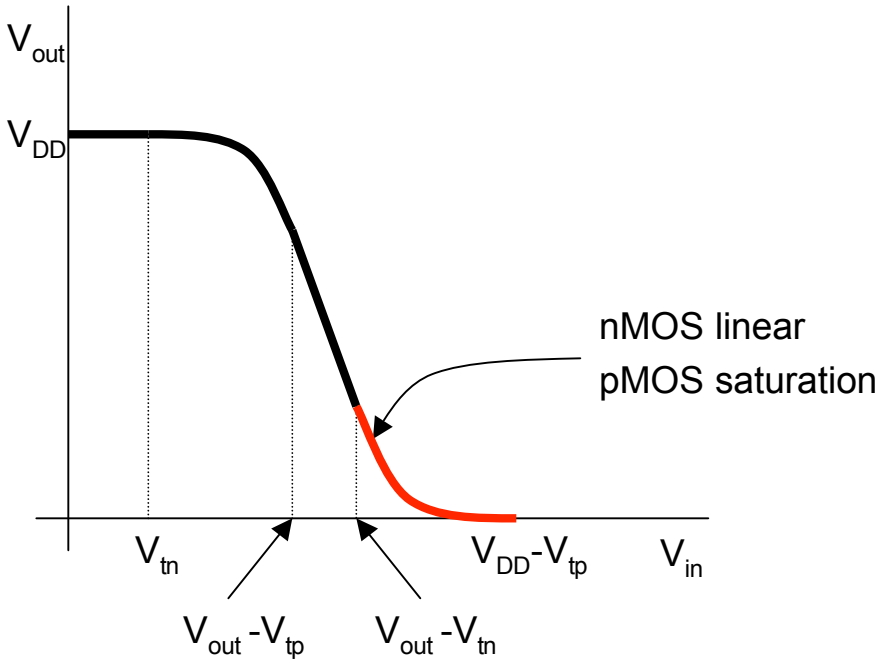
CMOS Inverter VTC



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CMOS Inverter VTC

- Set nMOS Linear I_{DS} equal to pMOS Saturation I_{DS}

$$k_p\left(\frac{\left(V_{in}-V_{DD}-V_{tp}\right)^2}{2}\right)=k_n\left(\left(V_{in}-V_{tn}\right)V_{out}-\frac{{V_{out}}^2}{2}\right)$$

$$\frac{{V_{out}}^2}{2}-\left(V_{in}-V_{tn}\right)V_{out}+\frac{k_p}{k_n}\frac{\left(V_{in}-V_{DD}-V_{tp}\right)^2}{2}=0$$

$$V_{out}=\left(V_{in}-V_{tn}\right)-\sqrt{\left(V_{in}-V_{tn}\right)^2-\frac{k_p}{k_n}\left(V_{in}-V_{DD}-V_{tp}\right)^2}$$

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CMOS Inverter VTC

- Short channel model

$$k_p V_{DSATp}\left(V_{in} - V_{DD} - V_{tp} - \frac{V_{DSATp}}{2}\right) = k_n\left((V_{in} - V_{tn})V_{out} - \frac{{V_{out}}^2}{2}\right)$$

$$\frac{{V_{out}}^2}{2} - (V_{in} - V_{tp})V_{out} + \frac{k_p}{k_n} V_{DSATp}\left(V_{in} - V_{DD} - V_{tp} - \frac{V_{DSATp}}{2}\right) = 0$$

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - 2\frac{k_p}{k_n} V_{DSATp}\left(V_{in} - V_{DD} - V_{tp} - \frac{V_{DSATp}}{2}\right)}$$

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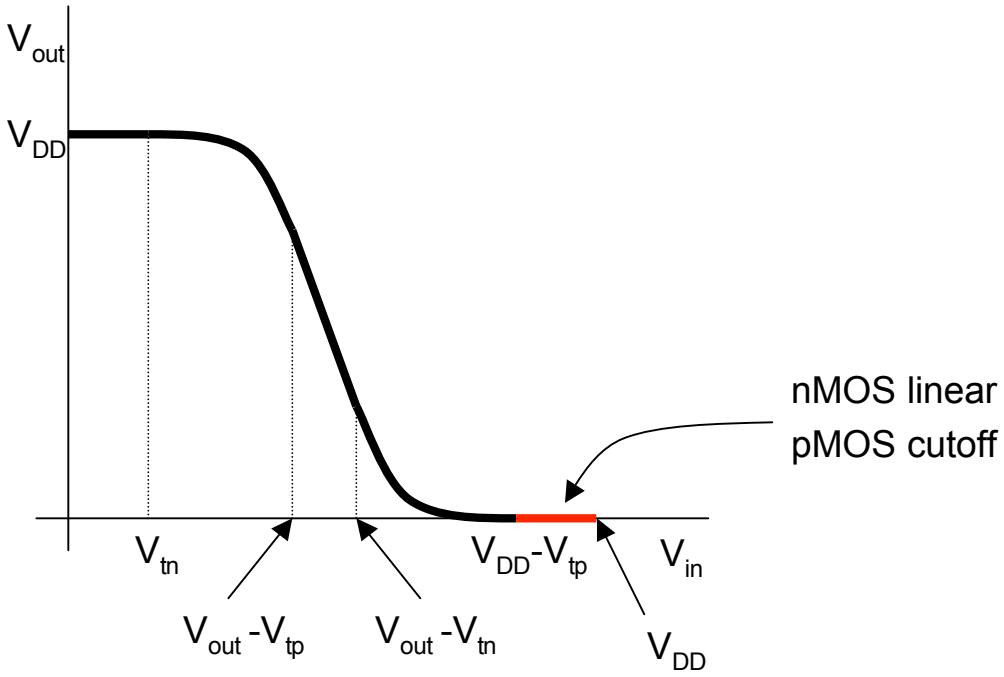
CMOS Inverter VTC



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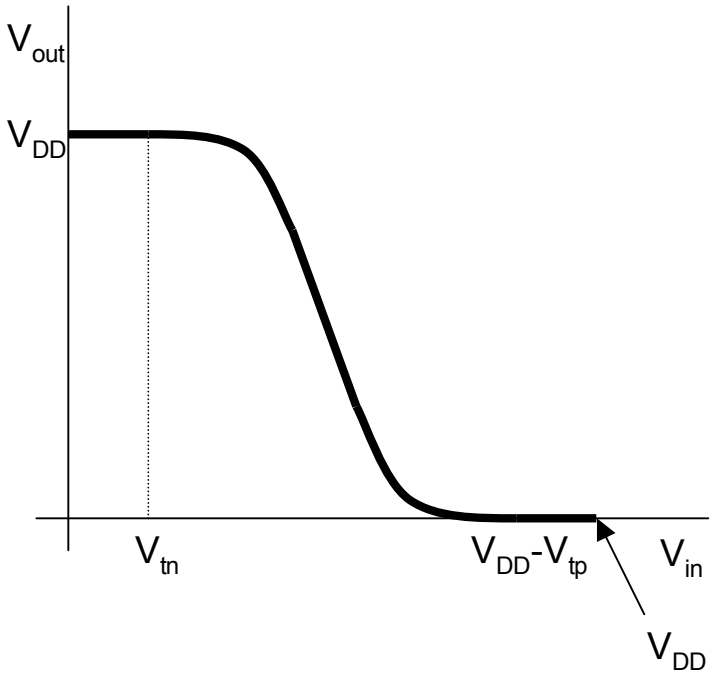
CMOS Inverter VTC



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CMOS Inverter

V_{in}	pMOS mode	nMOS mode	V_{out}
$V_{in} < V_t$	Linear	Cutoff	V_{DD}
$V_t < V_{in} < V_{out} - V_t$	Linear	Saturation	$(V_{in} + V_t) + \sqrt{(V_{in} - V_{DD} + V_t)^2 - (V_{in} - V_t)^2}$
$V_{out} - V_t < V_{in} < V_{out} + V_t$	Saturation	Saturation	Interpolate
$V_{out} + V_t < V_{in} < V_{DD} - V_t$	Saturation	Linear	$(V_{in} - V_t) - \sqrt{(V_{in} - V_t)^2 - (V_{in} - V_{DD} + V_t)^2}$
$V_{in} > V_{DD} - V_t$	Cutoff	Linear	0

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Switching Threshold

- The point at which the inverter has both transistors in saturation

$$\frac{k_n}{2}\left(V_M - V_{tn}\right)^2 = -\frac{k_p}{2}\left(V_M - V_{DD} - V_{tp}\right)^2$$

$$\left(V_M - V_{tn}\right) = -\sqrt{\frac{-k_p}{k_n}}\left(V_M - V_{DD} - V_{tp}\right)$$

$$V_M\left(1 + r\right) = V_{tn} + r\left(V_{DD} + V_{tp}\right)$$

$$V_M = \frac{V_{tn} + r\left(V_{DD} + V_{tp}\right)}{1 + r}$$

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Switching Threshold

$$V_M = \frac{r\left(V_{DD} + V_{tp}\right) + V_{tn}}{1 + r}$$

- When V_{tn}=-V_{tp} and r=1,

$$V_M = \frac{V_{DD}}{2}$$

  - In switching region, the curve is actually vertical; V_{out} can have multiple values

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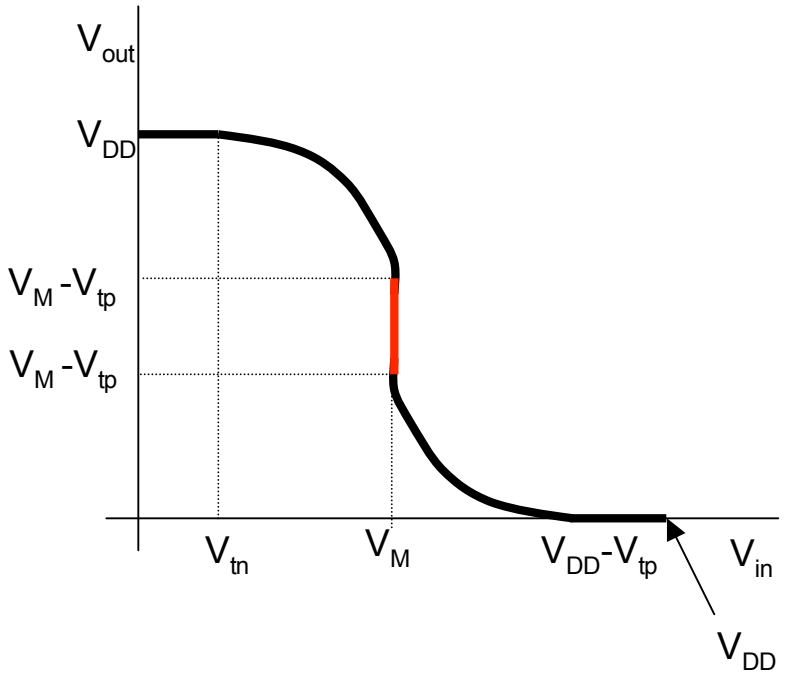
CMOS Inverter VTC



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Switching Threshold

- With short-channel devices

$$k_n V_{DSATn}\left(V_M - V_{tn} - \frac{V_{DSATn}}{2}\right) = -k_p V_{DSATp}\left(V_M - V_{DD} - V_{tp} - \frac{V_{DSATp}}{2}\right)$$

$$\left(V_M - V_{tn} - \frac{V_{DSATn}}{2}\right) = -\frac{k_p V_{DSATp}}{k_n V_{DSATn}}\left(V_M - V_{DD} - V_{tp} - \frac{V_{DSATp}}{2}\right)$$

$$V_M\left(1 + \frac{k_p V_{DSATp}}{k_n V_{DSATn}}\right) = V_{tn} + \frac{V_{DSATn}}{2} - \frac{k_p V_{DSATp}}{k_n V_{DSATn}}\left(-V_{DD} - V_{tp} - \frac{V_{DSATp}}{2}\right)$$

$$V_M = \frac{V_{tn} + \frac{V_{DSATn}}{2} + r\left(V_{DD} + V_{tp} + \frac{V_{DSATp}}{2}\right)}{1 + r}$$

$$V_M = V_{DD}\frac{r}{1 + r}$$

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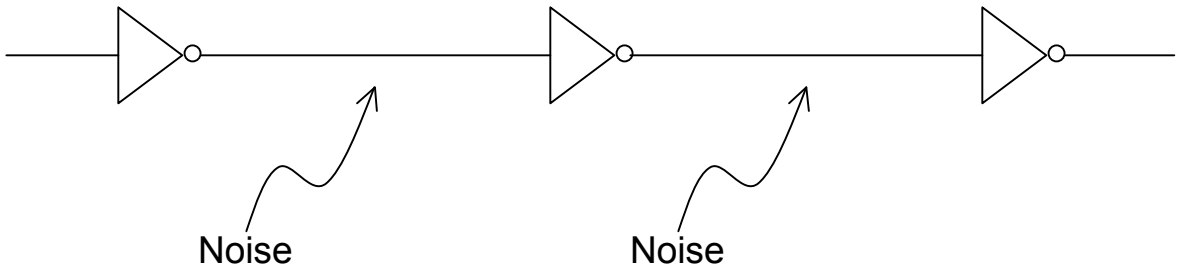
Noise Margin

- A measure of the acceptable noise at a gate input so that the output is not affected.



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Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources

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Key Reliability Properties

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

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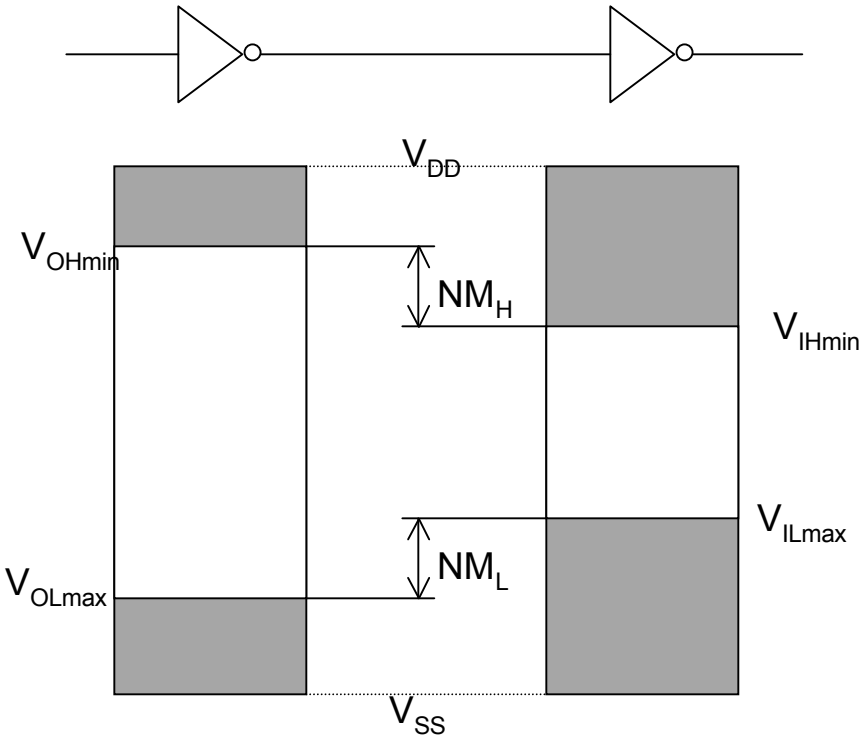
Noise Margins



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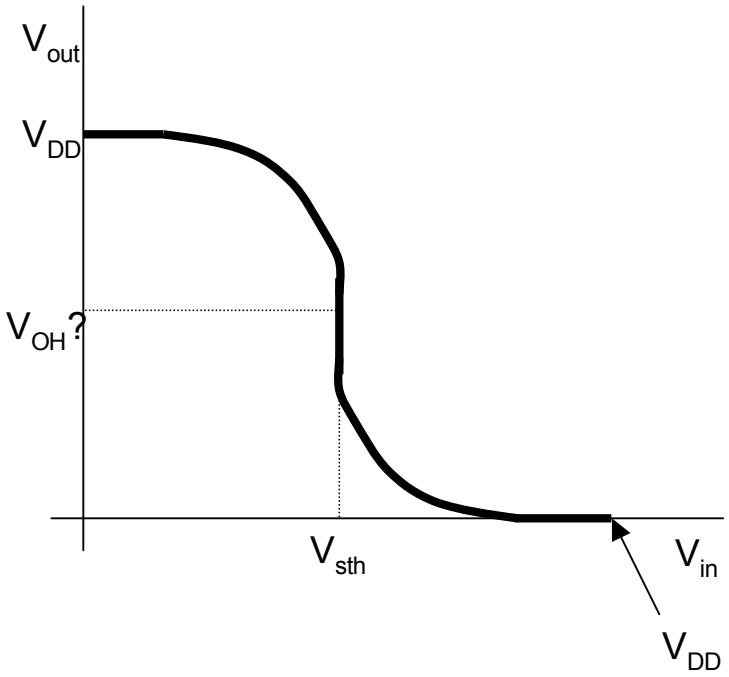
Noise Margins



- Obvious choice
- Set $V_{IH}=V_{IL}=V_M$
- No noise margin
- High gain at V_{IH} and V_{IL}
- Any perturbations could cause incorrect values

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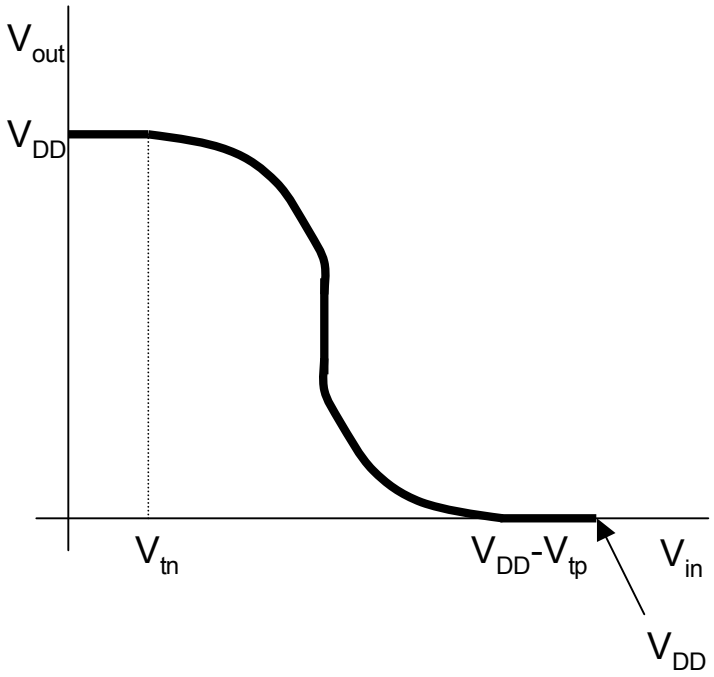
Noise Margins



- Set $V_{IL} = V_{tn}$ and $V_{IH} = V_{DD} - V_{tp}$
- $V_{OL} = 0$ and $V_{OH} = V_{DD}$
- Too restrictive

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Noise Margins

- Voltage Transfer Function

$$V_{out} = f\left(V_{in}\right)$$

- Voltage Transfer Function with Noise

$$V_{out} = f\left(V_{in} + \Delta V_{noise}\right)$$

$$V_{out} \approx f\left(V_{in}\right) + \frac{dV_{out}}{dV_{in}} \Delta V_{noise}$$

- Perturbed voltage is the sum of the nominal output plus the gain times the noise
- Keep the gain less than 1

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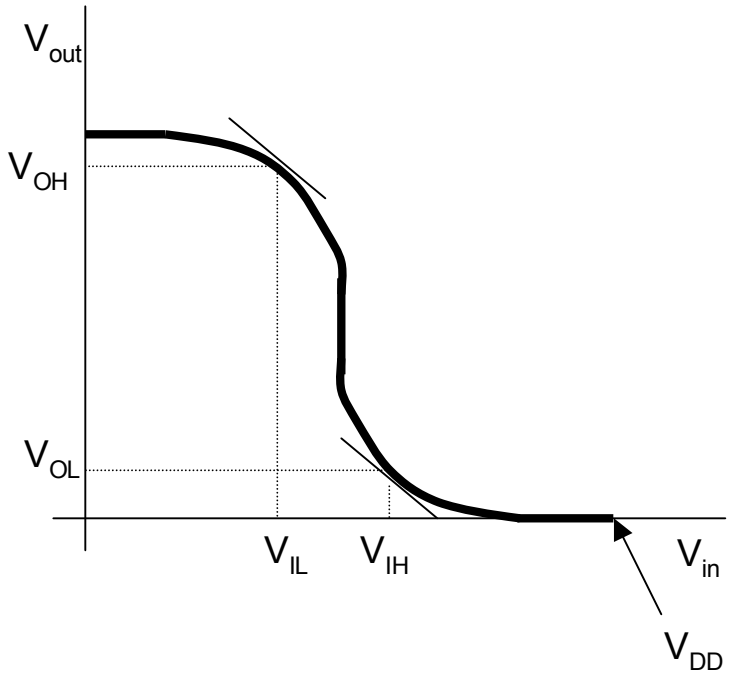
Noise Margins



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Noise Margins

- Setting the derivative to -1 and solving

$$V_{IH} = V_M + V_M \frac{\left(V_M - V_{Tn} - V_{DSATn}/2\right)\left(\lambda_n - \lambda_p\right)}{1+r}$$

$$V_{IL} = V_M - \left(V_{DD} - V_M\right)\frac{\left(V_M - V_{Tn} - V_{DSATn}/2\right)\left(\lambda_n - \lambda_p\right)}{1+r}$$

- Assuming $r = 1, V_{Tn} = -V_{Tp}, V_{DSATn} = -V_{DSATp}$

$$V_{IH} = \frac{V_{DD}}{2}\left[1 + \left(\frac{V_{DD}}{2} - V_T - \frac{V_{DSAT}}{2}\right)\frac{\left(\lambda_n - \lambda_p\right)}{2}\right]$$

$$V_{IL} = \frac{V_{DD}}{2}\left[1 - \left(\frac{V_{DD}}{2} - V_T - \frac{V_{DSAT}}{2}\right)\frac{\left(\lambda_n - \lambda_p\right)}{2}\right]$$

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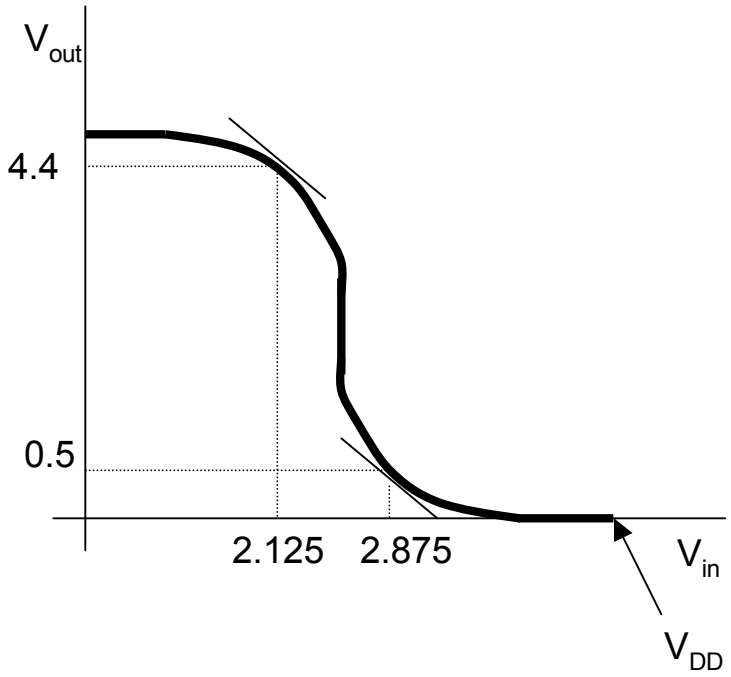
Noise Margins



- V_{DD} = 5 V
- V_t = 0.5 V
- V_{DSAT}=1.0V
- λ=0.1

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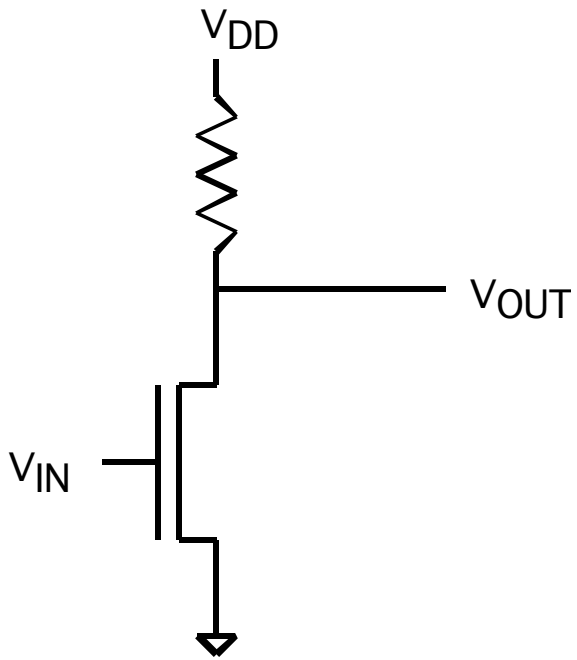
Static Load Inverter



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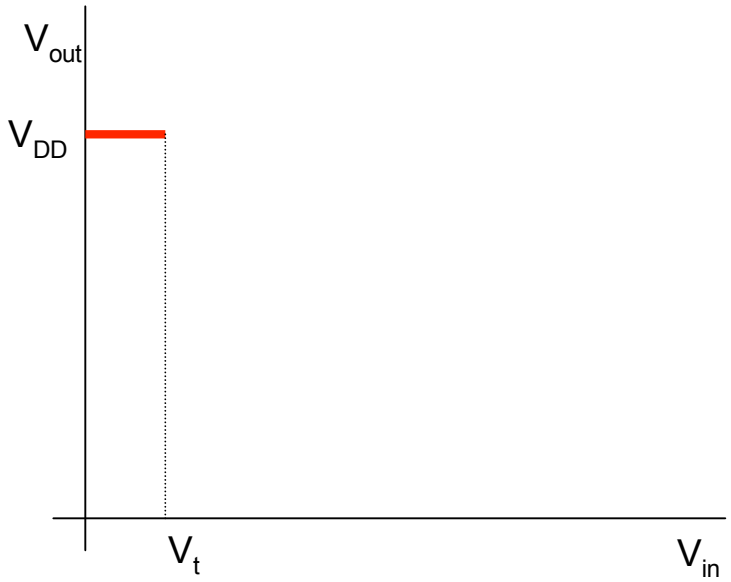
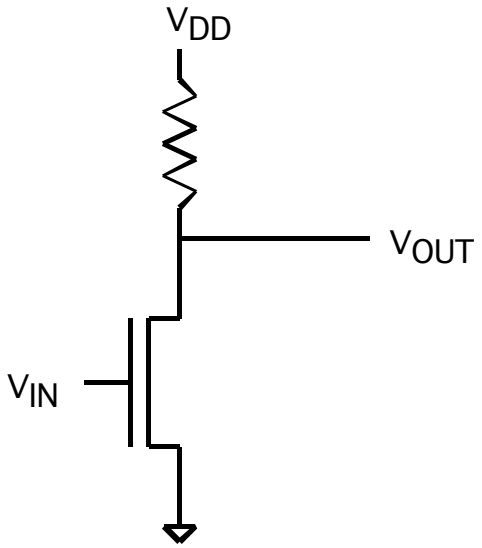
Static Load Inverter





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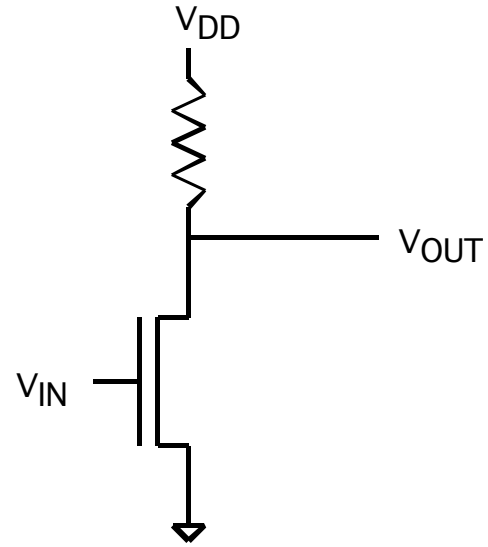
Static Load Inverter

- Transistor is in saturation

$$I_{DS} = k_n \frac{\left(V_{GS} - V_T\right)^2}{2}\left(1 + \lambda V_{DS}\right)$$

$$V_{OUT} = V_{DD} - Rk_n \frac{\left(V_{IN} - V_T\right)^2}{2}\left(1 + \lambda V_{OUT}\right)$$

$$V_{OUT} = \frac{2V_{DD} - Rk_n\left(V_{IN} - V_T\right)^2}{2 + \lambda Rk_n\left(V_{IN} - V_T\right)^2}$$



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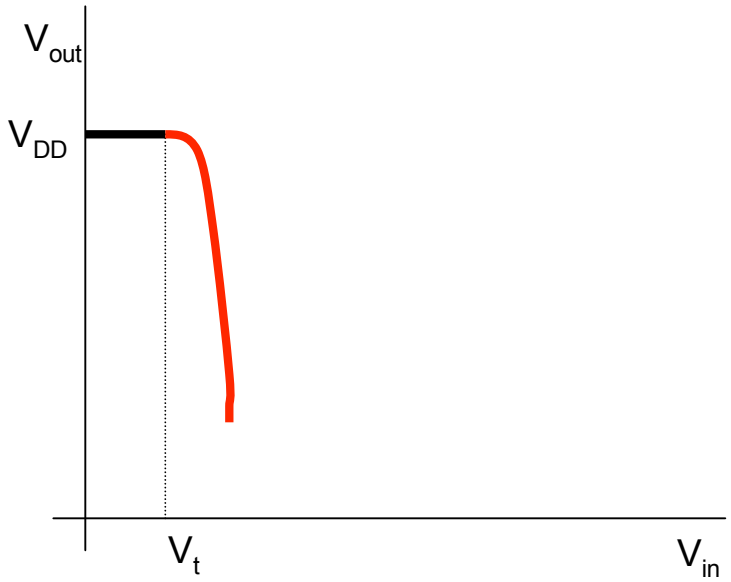
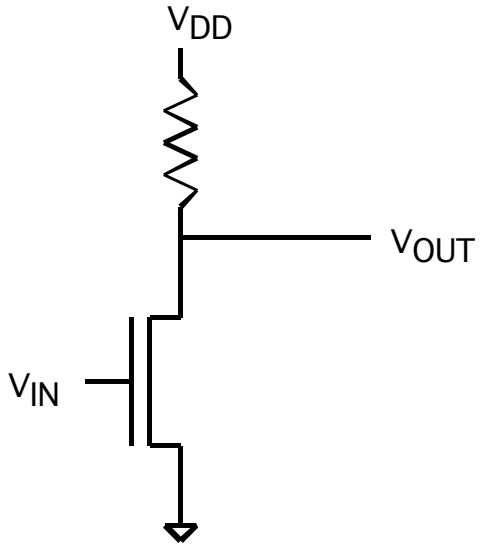
Static Load Inverter





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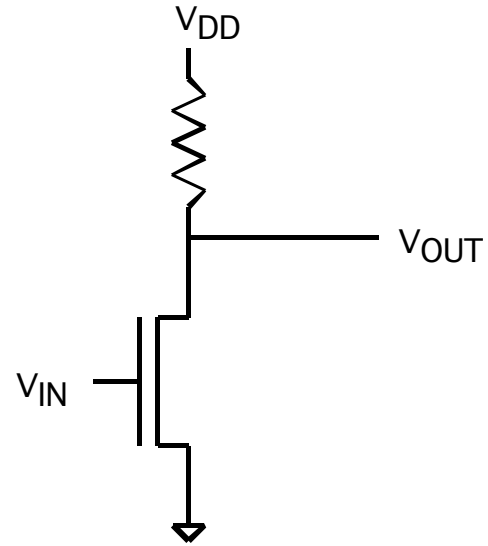
Static Load Inverter

- Transistor is in linear region



$$I_{DS} = k_n\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

$$V_{OUT} = V_{DD} - Rk_n\left[\left(V_{IN} - V_T\right)V_{OUT} - \frac{{V_{OUT}}^2}{2}\right]$$

$$\frac{Rk_n}{2}{V_{OUT}}^2 - \left(Rk_n\left(V_{IN} - V_T\right) + 1\right)V_{OUT} + V_{DD} = 0$$

$$V_{OUT} = \left(V_{IN} - V_T\right) + \frac{1}{Rk_n} - \sqrt{\left(\left(V_{IN} - V_T\right) + \frac{1}{Rk_n}\right)^2 - 2\frac{V_{DD}}{Rk_n}}$$

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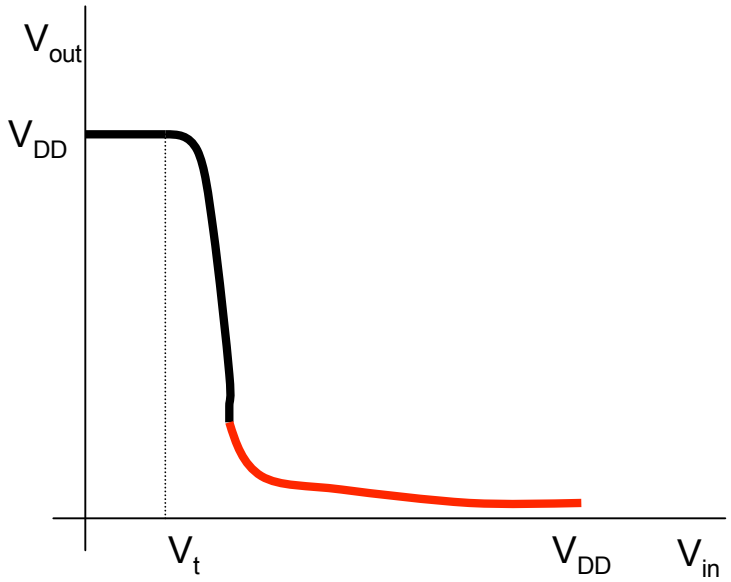
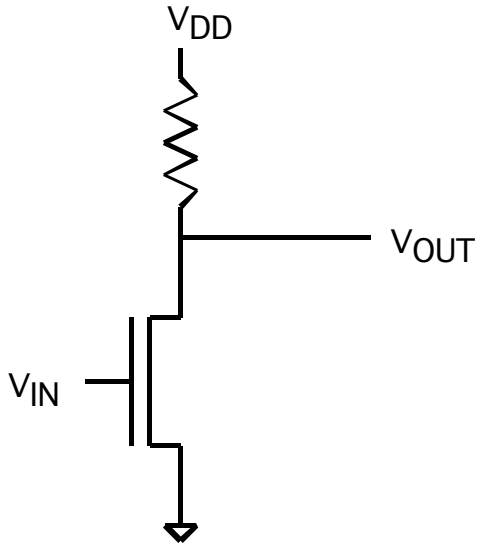
Static Load Inverter





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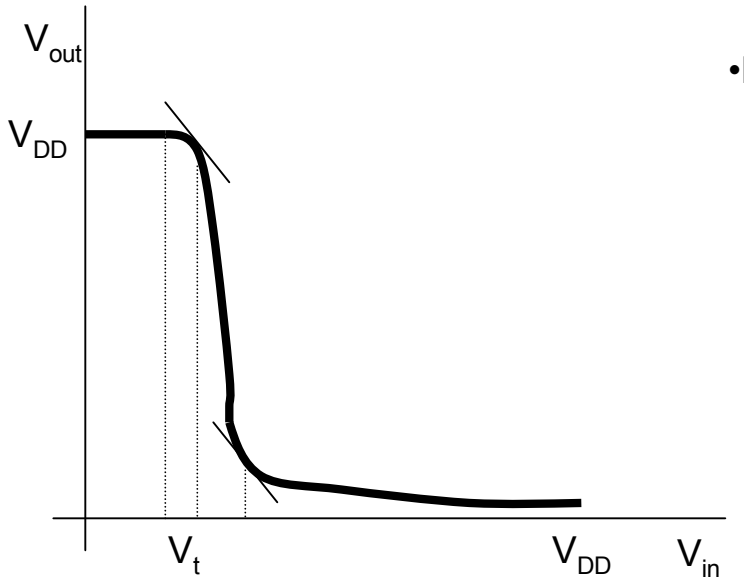
Static Load Inverter



•Noise Margin

$$V_{IL} = V_T + \frac{1}{k_n R}$$

$$V_{IH} = V_T + \sqrt{\frac{8}{3}\frac{V_{DD}}{k_n R}} - \frac{1}{k_n R}$$

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Static Load Inverter

- Does not go down all the way to 0
- Noise margins are tighter
- Switching threshold is not centered
- To get high gain in the transition region, you need bigger resistors

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Homework

- Due February 3rd
- Read Chapter 2

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