VLSI Design and Simulation

Lecture 4

CMOS Processing Technology

Topics

- CMOS Processing Technology

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Semiconductor Processing

- How do we make a transistor?
- Fabrication Process

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Wafer Processing

- Silicon single crystal growth from polysilicon
- Silicon ingot with impurities is created
- Ingot diameter can vary from 100mm to 300mm
- Wafers are sliced from the ingot
- Typically 300-600μm thick

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Wafer Processing

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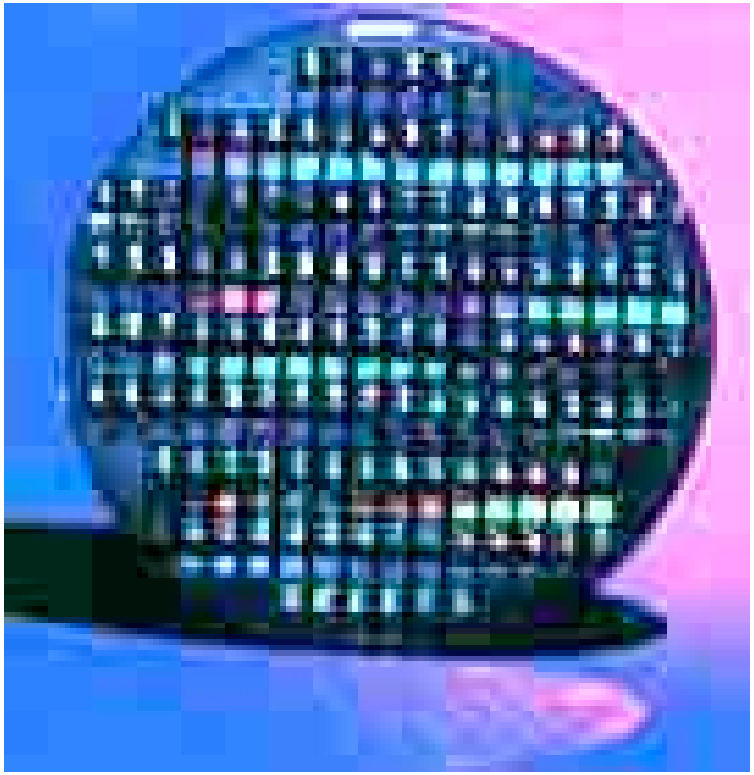
Wafer Processing



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Wafer Processing

- Why the trend to larger wafers?
  - More chips per wafer
  - Less waste
- After slicing
  - Lapping
  - Polishing
  - Defect detection

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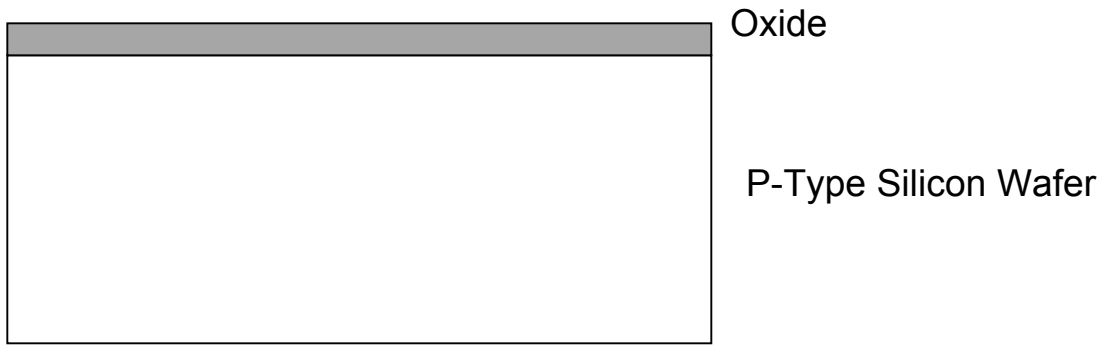
Semiconductor Processing

- Oxide Layer - SiO_2 (sand)
  - Heat Wafer in an oxidizing atmosphere - water vapor or pure oxygen gas



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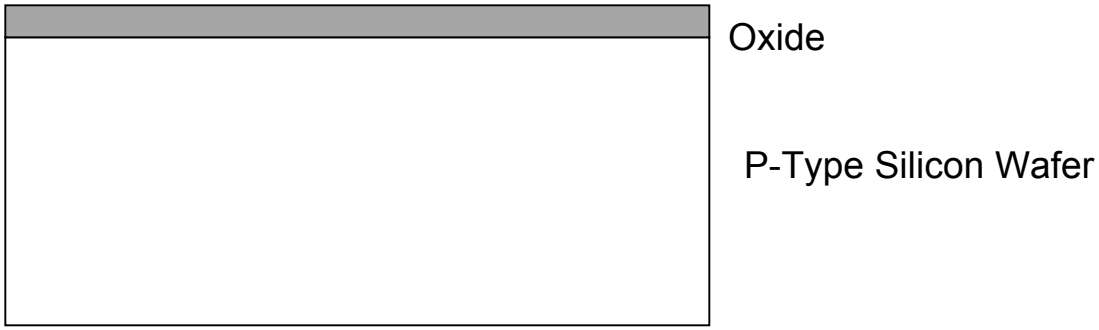
Semiconductor Processing

- How do you control where the features get placed?
  - Photolithography masks



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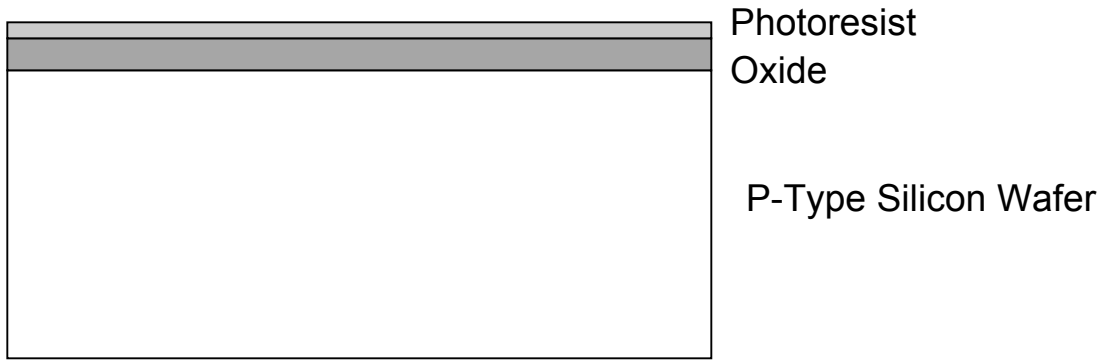
Semiconductor Processing

- Need to remove the oxide layer



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Semiconductor Processing

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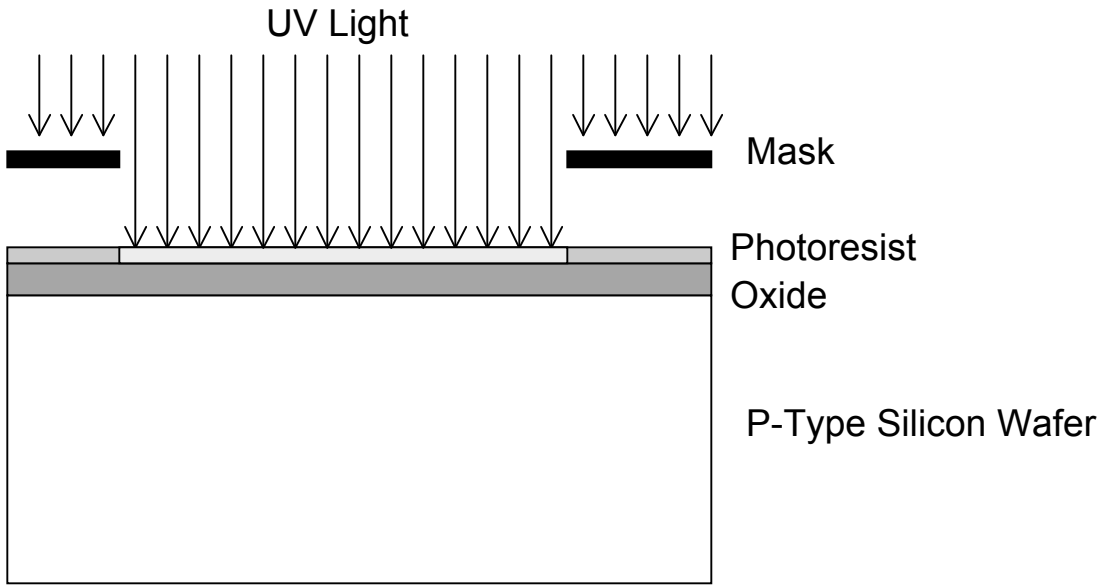

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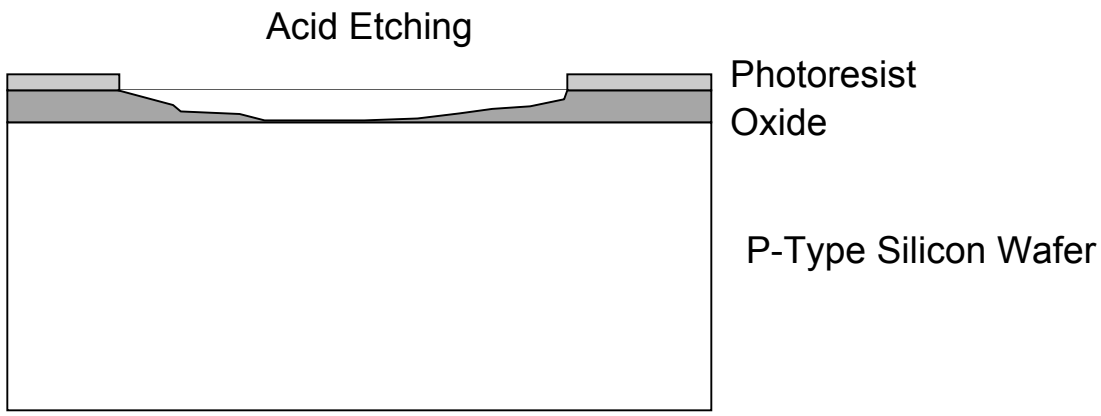
Semiconductor Processing

- Need to remove the oxide layer



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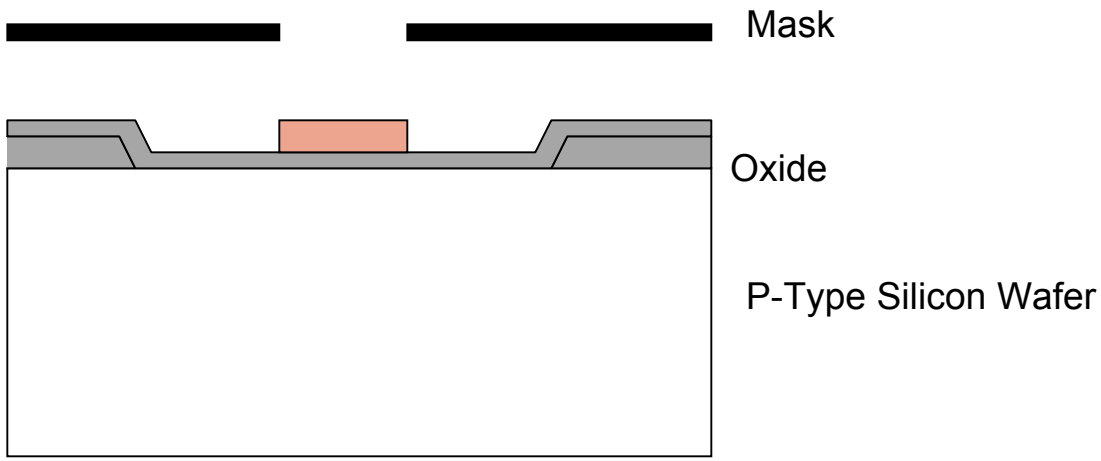
Semiconductor Processing

- Add polysilicon layer for gate



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Semiconductor Processing

- Impurity injection
  - Diffusion
    - Wafers are placed in a heated tube with dopant gas
    - At high temperatures (~1000ºC), the dopant diffuses into the exposed regions of the wafer
  - Ion Implantation
    - Dopants are introduced as ions into material by sweeping a beam across the material
    - Depth of implantation and density is controlled by the acceleration and exposure time
    - High energy implantation can cause lattice damage
  - Deposition
    - Deposit a gas or vapor (CVD) on the wafer at high temperatures

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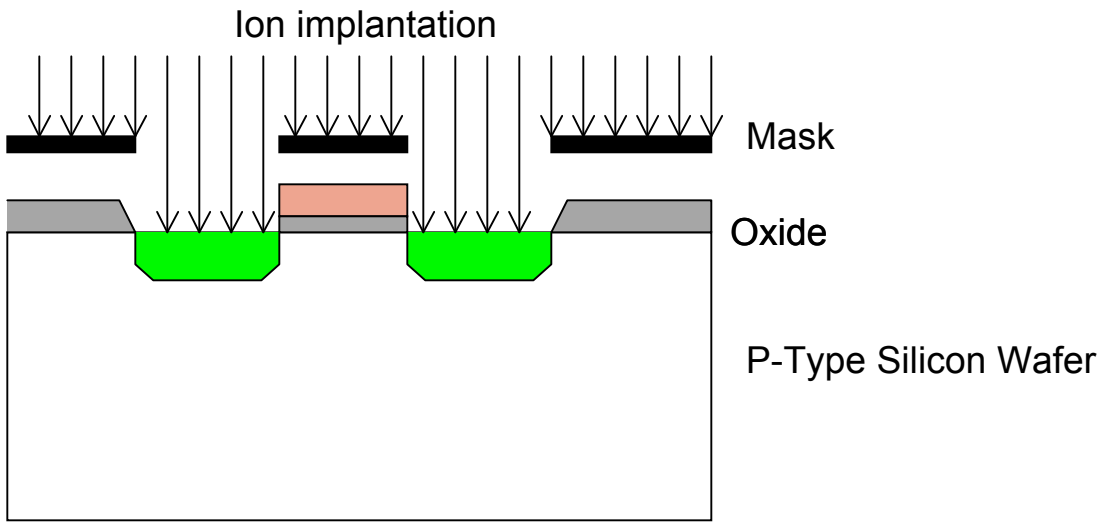
Semiconductor Processing

- Impurity injection



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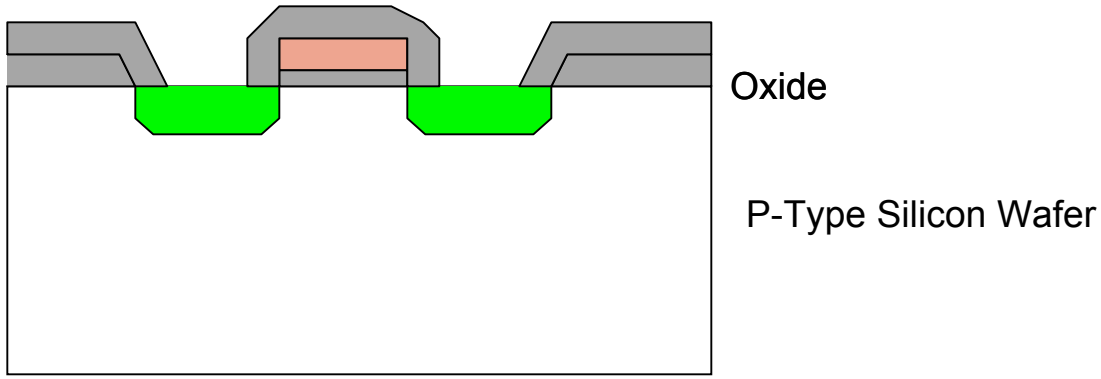
Semiconductor Processing

- Add Oxide insulation layer



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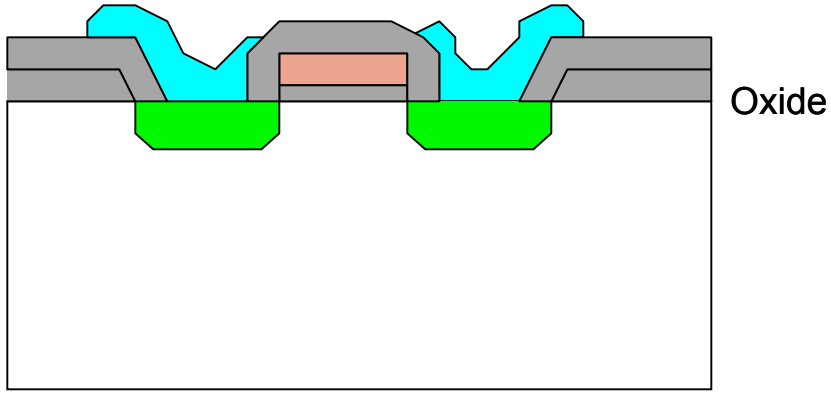
Semiconductor Processing

- Add Metal layer



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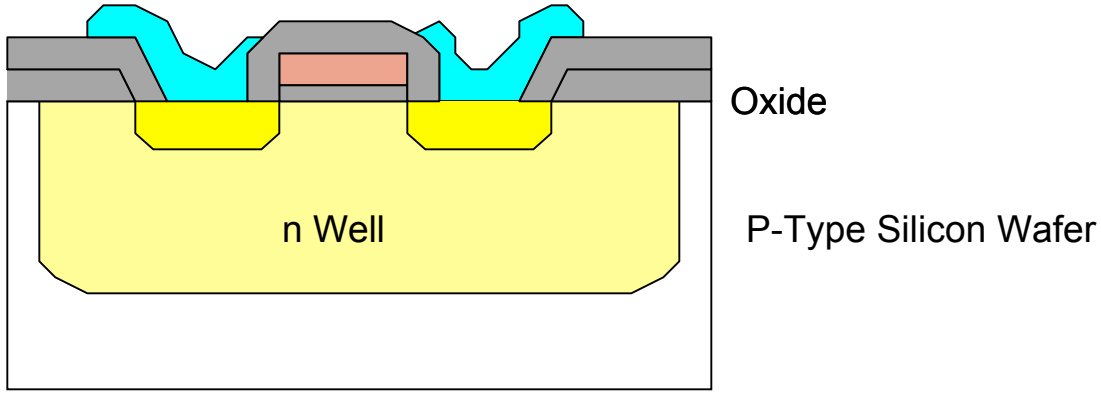
Semiconductor Processing

- pMOS Transistor



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Interconnect

- Polysilicon to Metal contacts
- Diffusion to Metal contacts
- Diffusion to Polysilicon silicide contacts
- Metal to Metal vias

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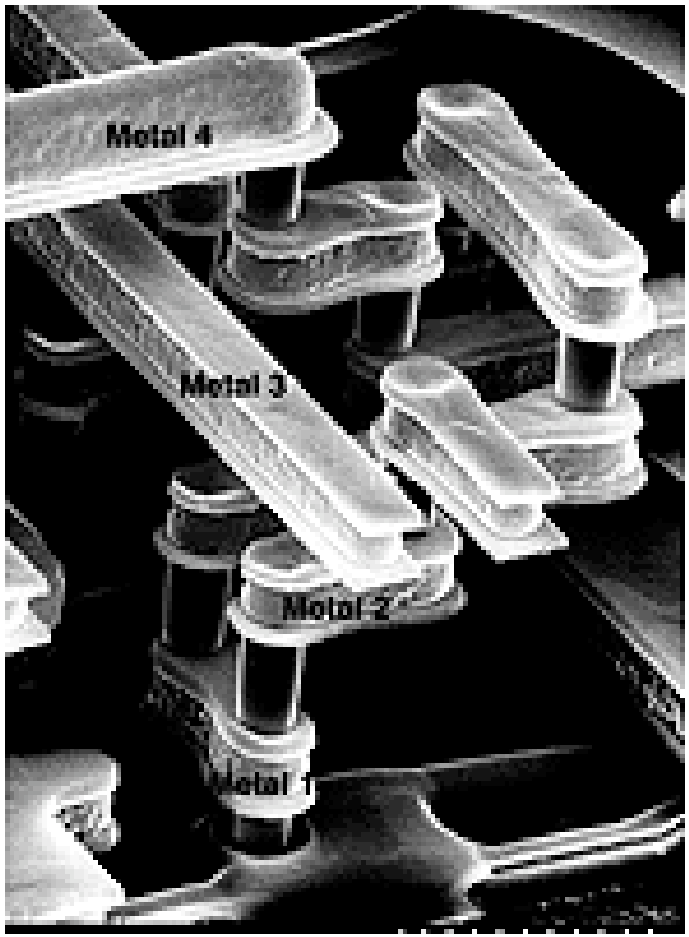
Metallization



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Packaging Requirements

- **Electrical: Low parasitics**
- **Mechanical: Reliable and robust**
- **Thermal: Efficient heat removal**
- **Economical: Cheap**

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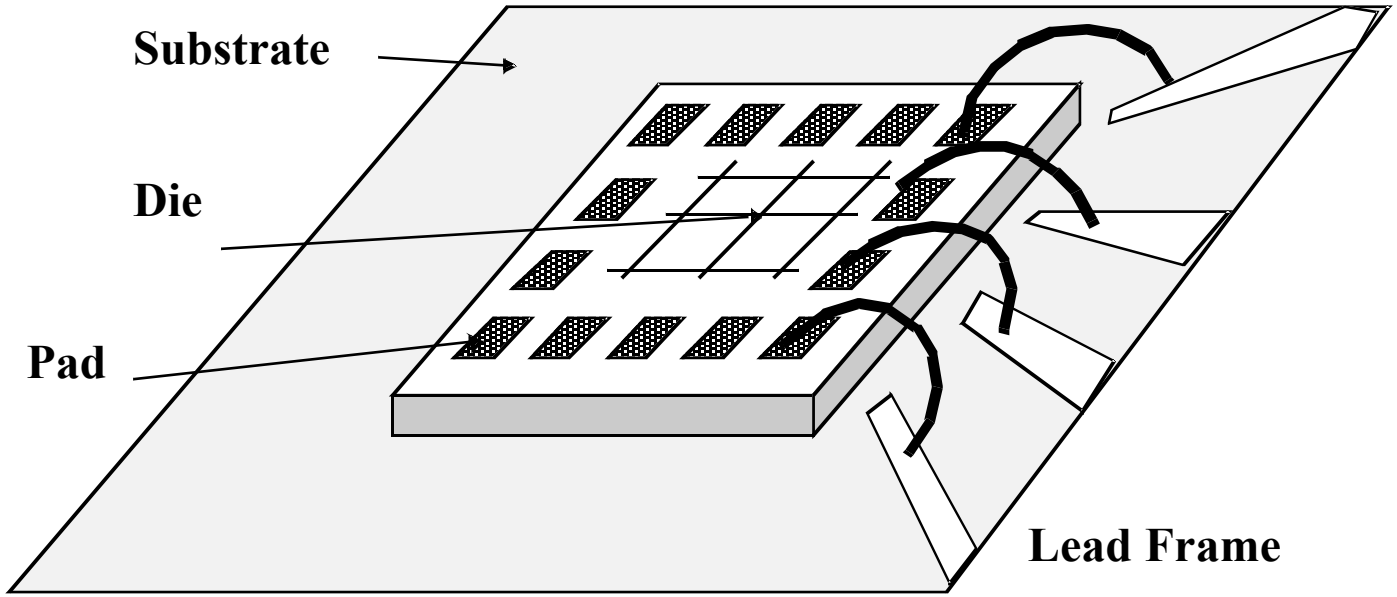
Bonding Techniques

Wire Bonding



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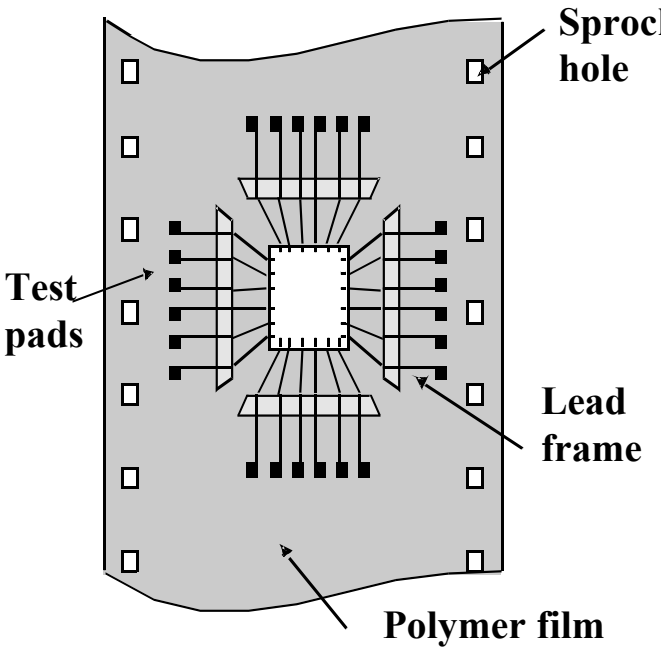
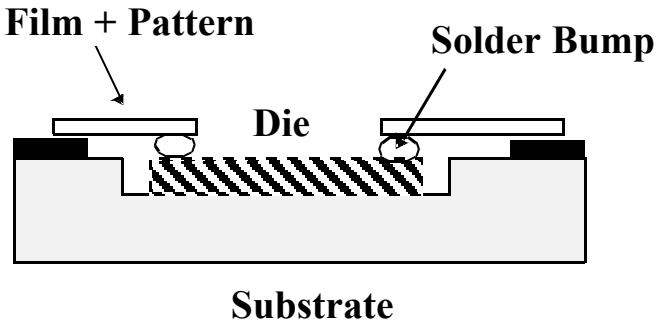
Tape-Automated Bonding (TAB)



(a) Polymer Tape with imprinted wiring pattern.



(b) Die attachment using solder bumps.

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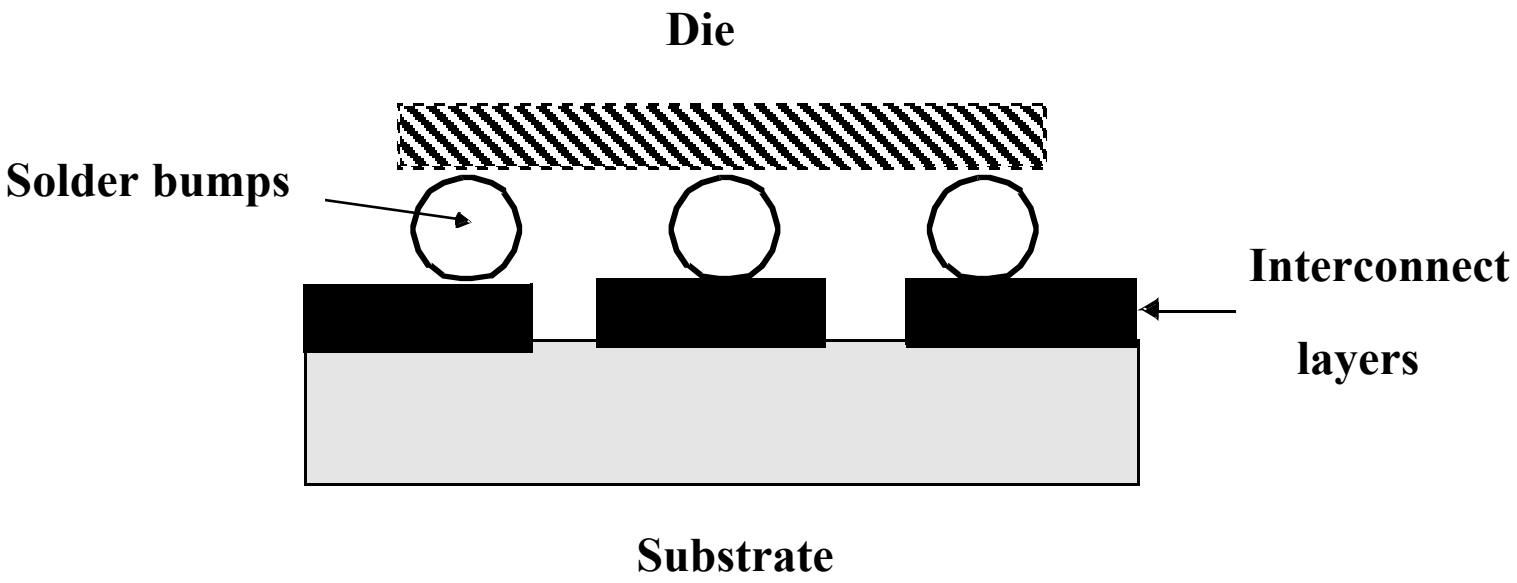
Flip-Chip Bonding



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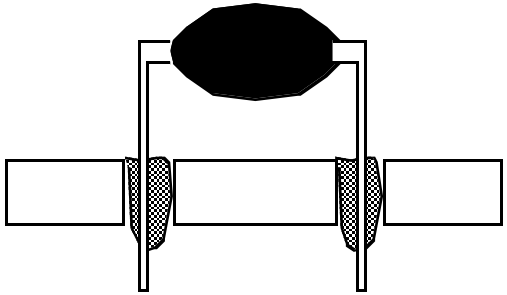
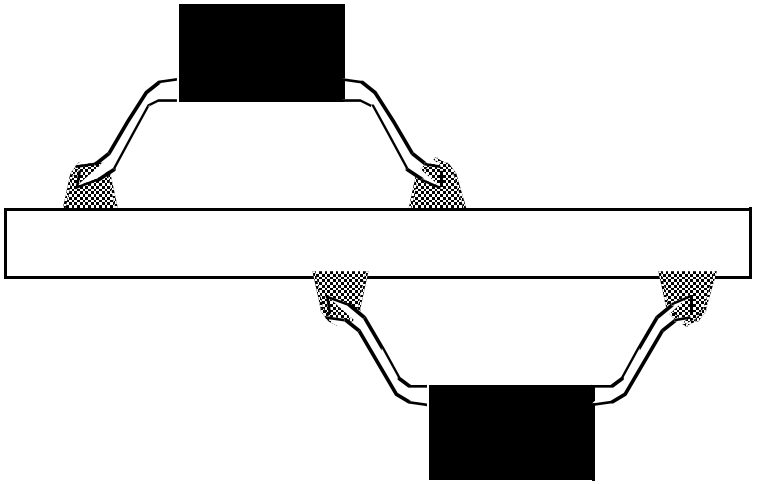
Package-to-Board Interconnect



(a) Through-Hole Mounting



(b) Surface Mount

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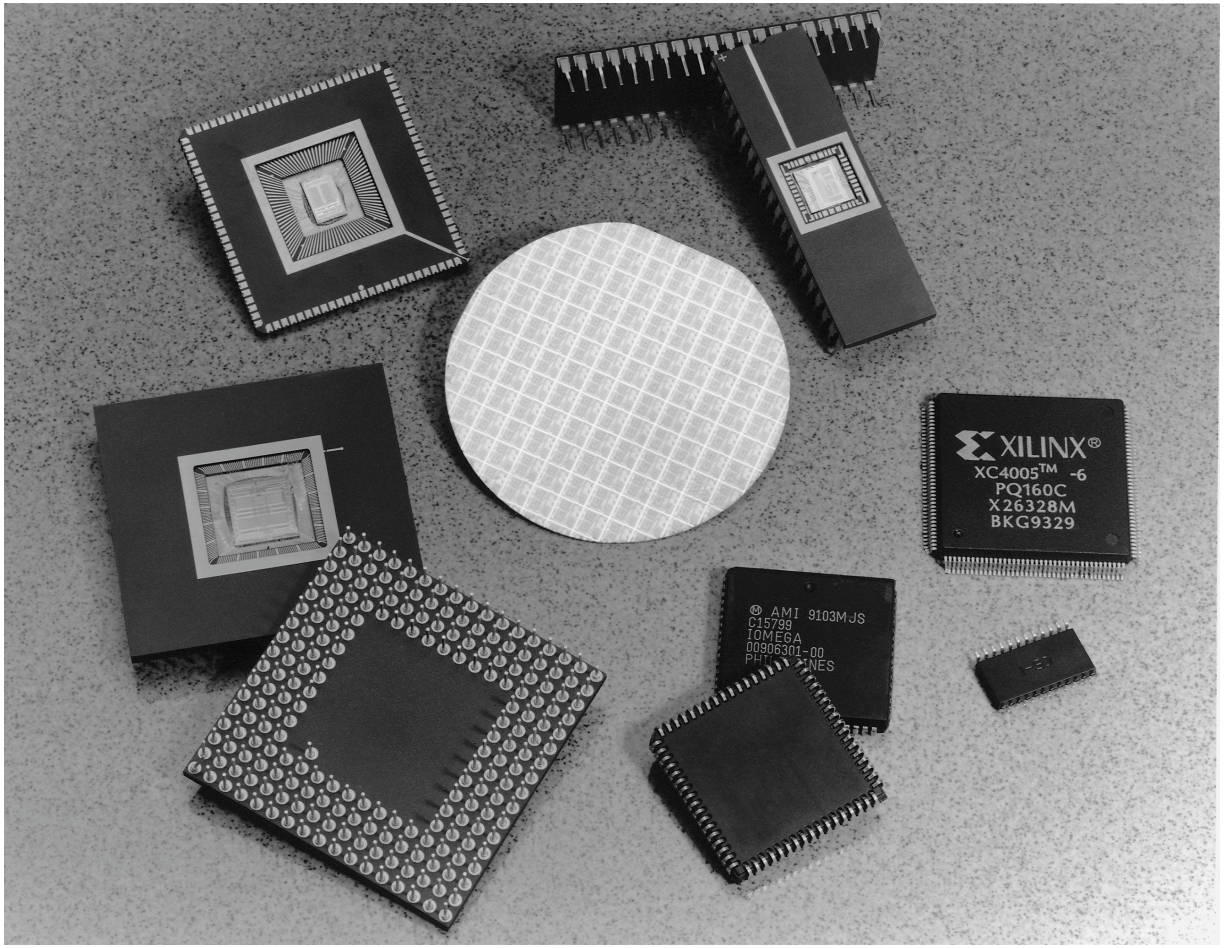
Package Types



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Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

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Trends in Process Technology

- Copper Conductors
- Silicon on Insulator
- Strained Silicon
- Three-dimensional ICs

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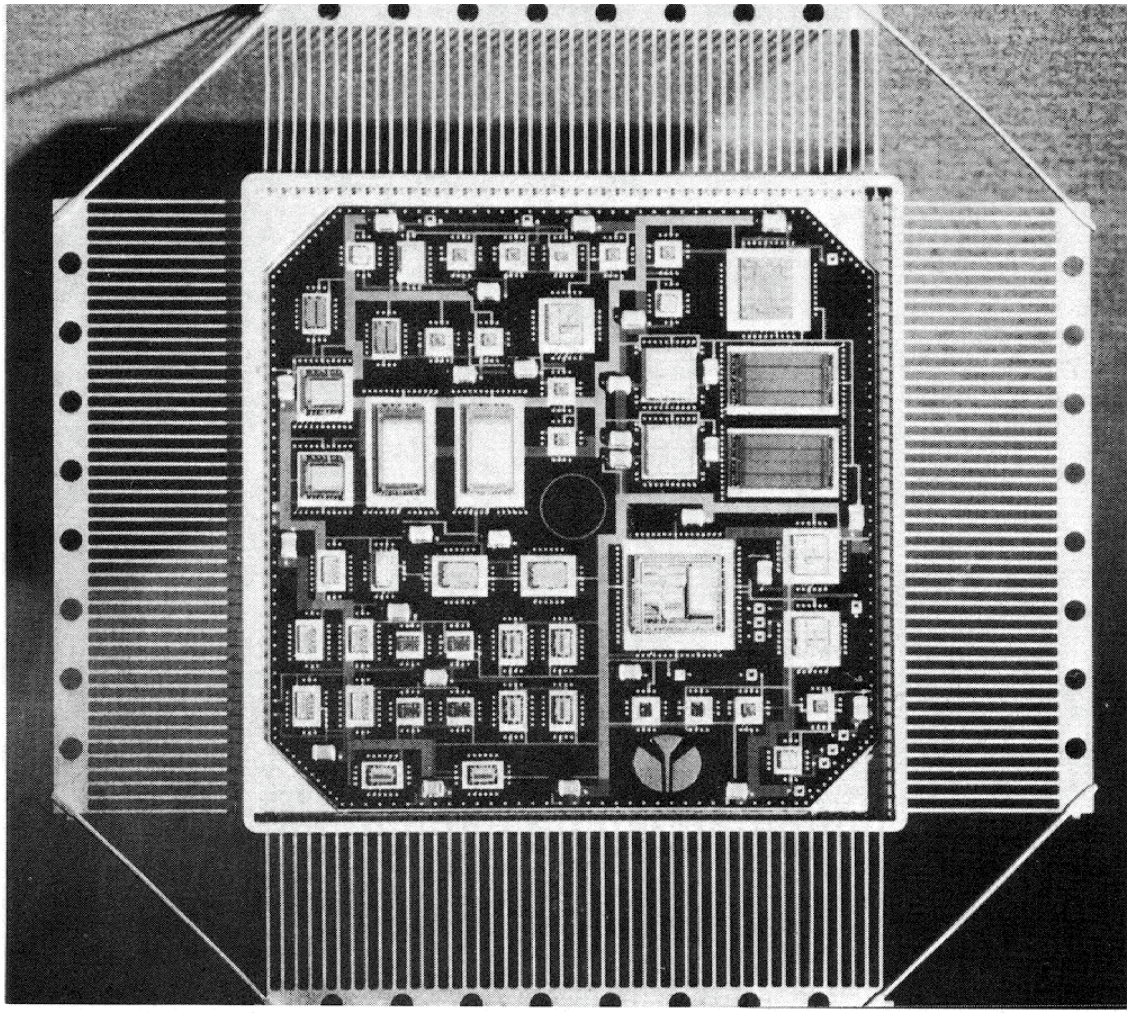
Multi-Chip Modules



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CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

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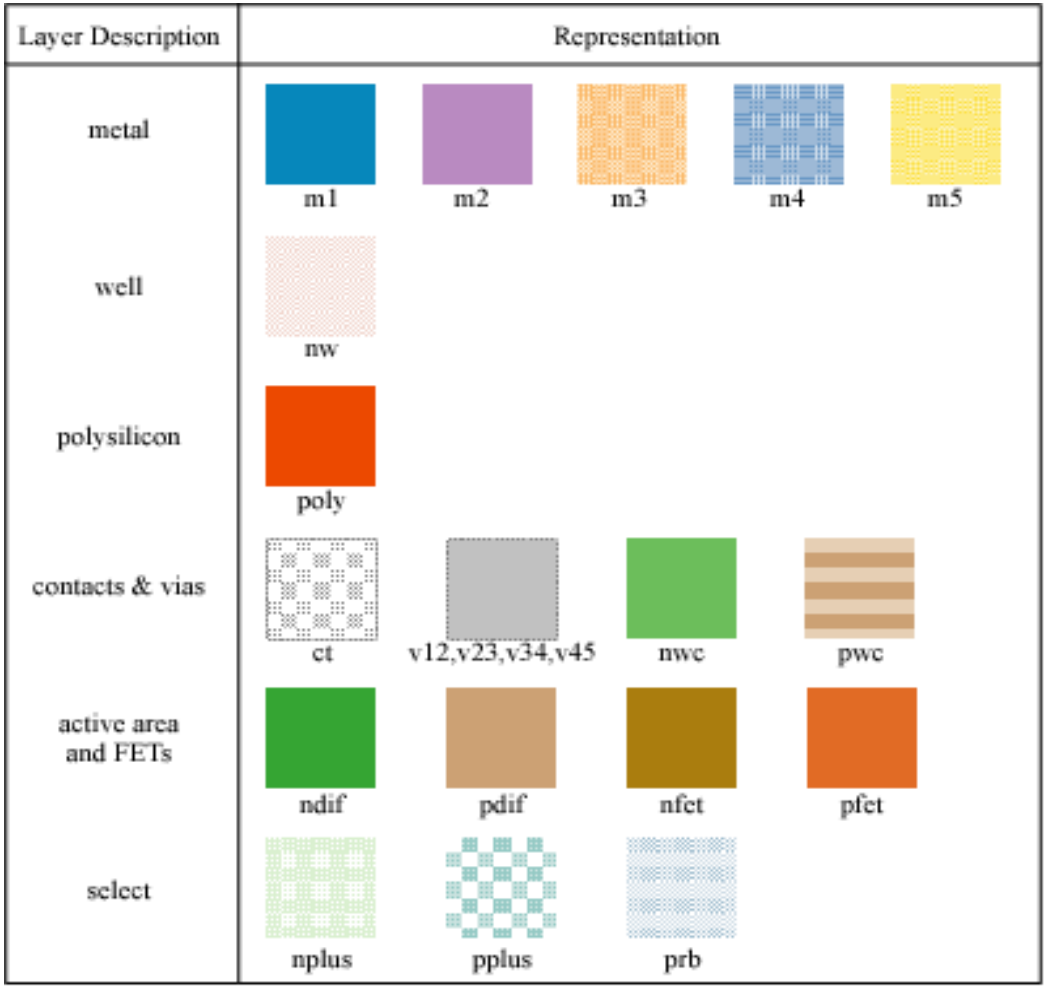
Layers in 0.25 μm CMOS process



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Semiconductor Masks

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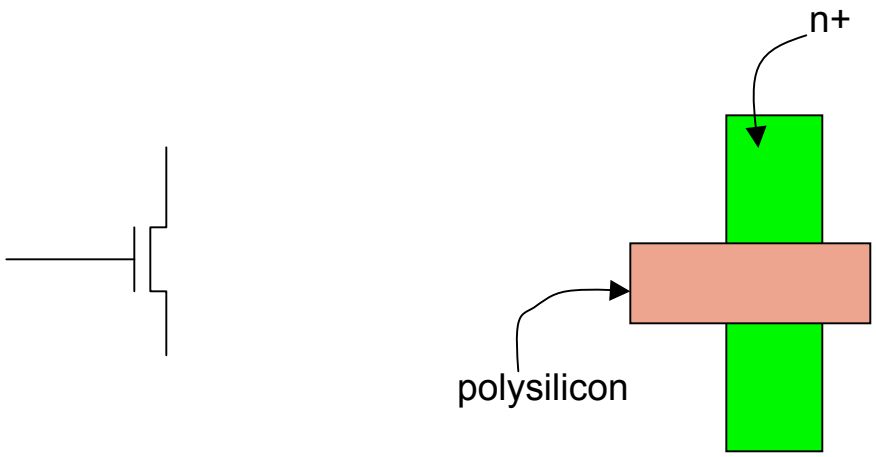
Semiconductor Masks



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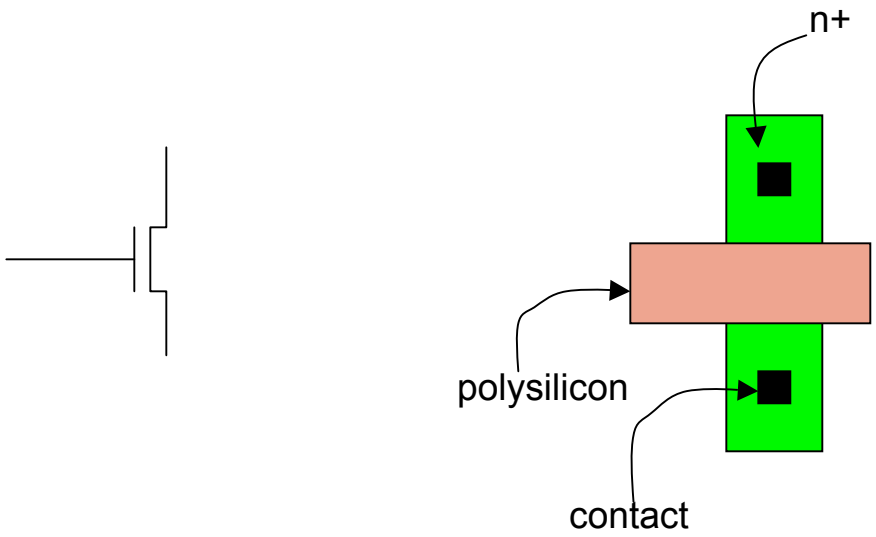
Semiconductor Masks



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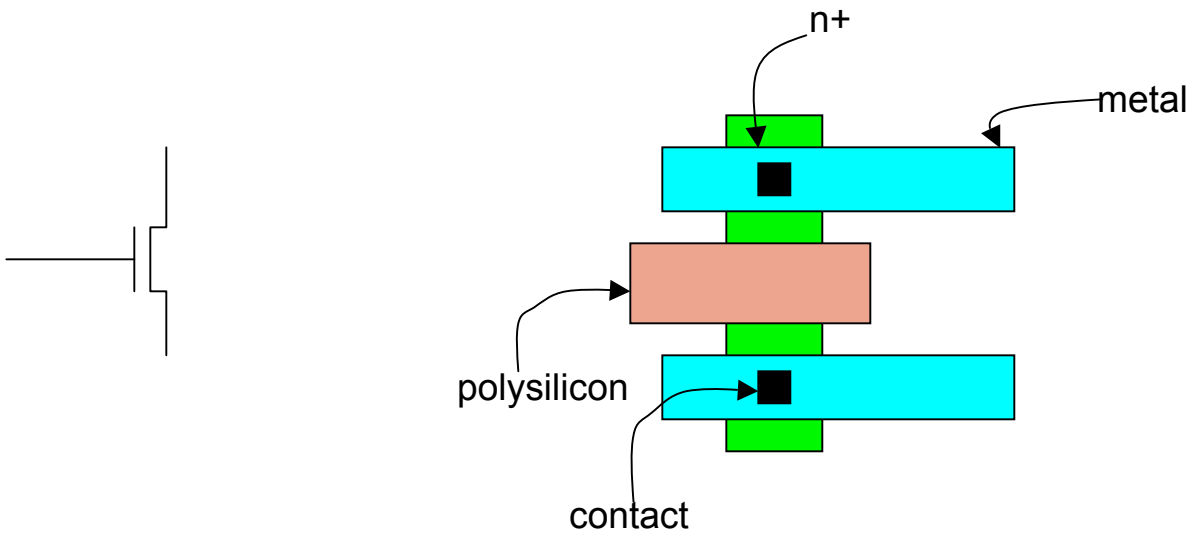
Semiconductor Masks



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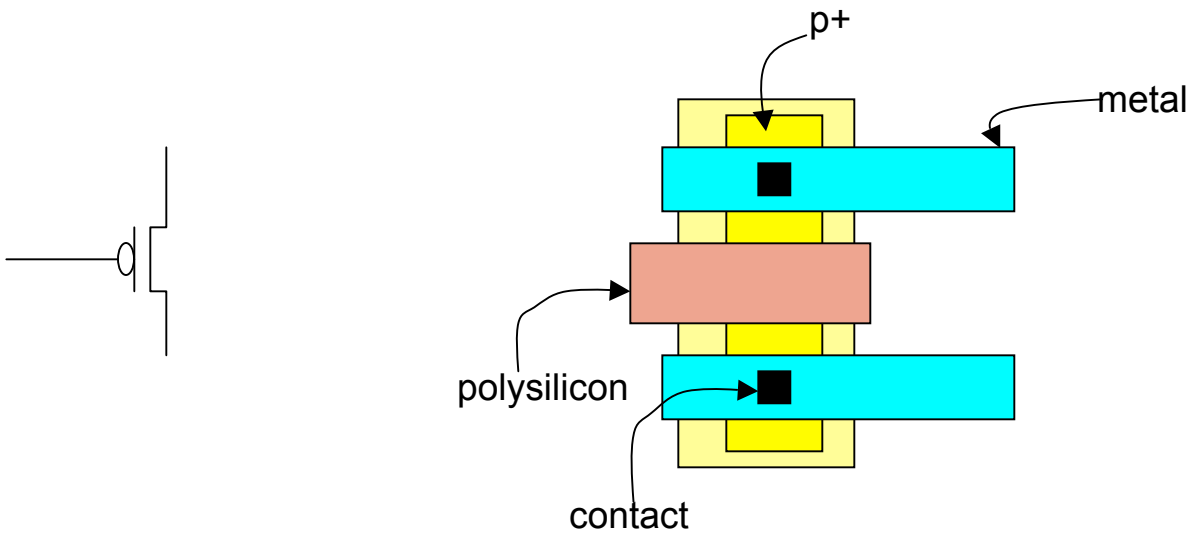
Semiconductor Masks



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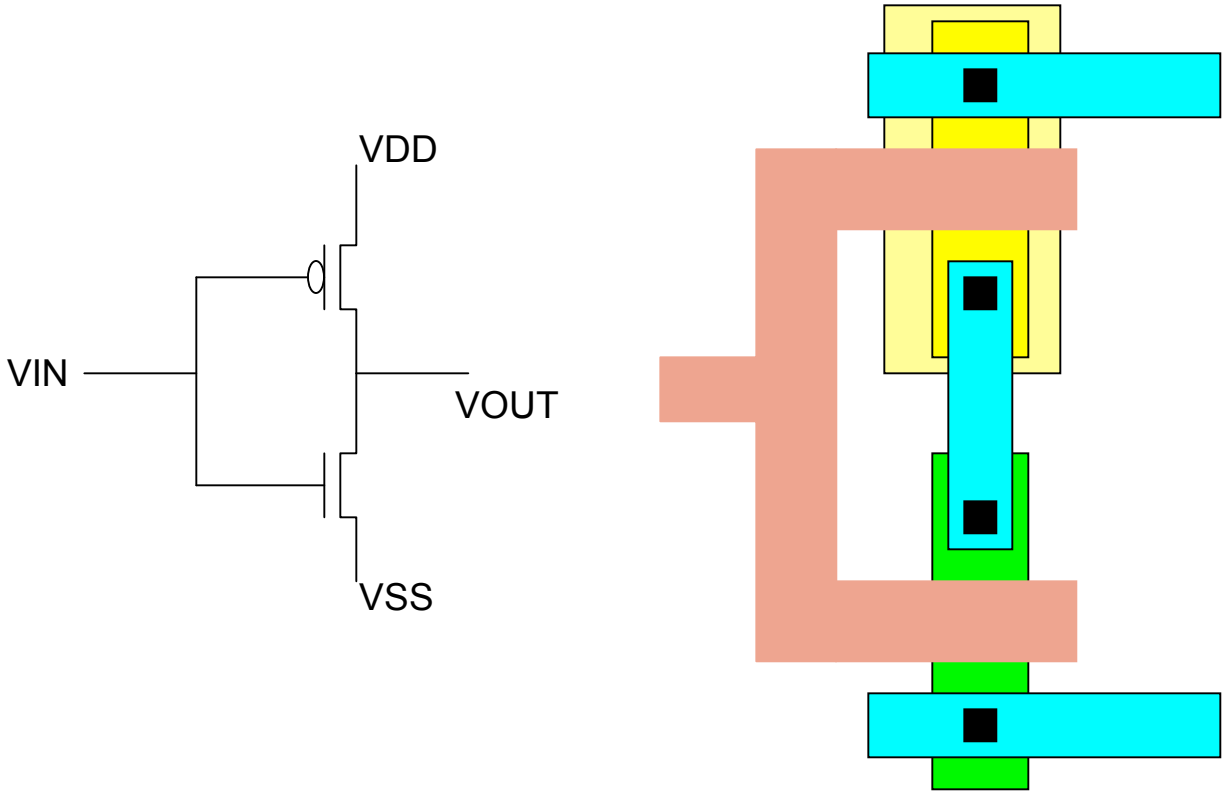
Semiconductor Masks



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Design rules

- Design rules are critical to proper operation of the circuit
- They place restrictions on the sizes of layers and the distance between layers
- Often expressed in terms of λ - half the minimum feature size

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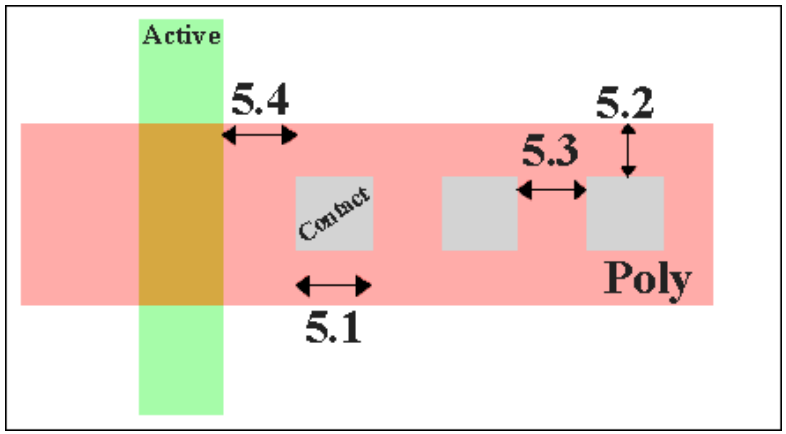
Design Rules

MOSIS SCMOS Design Rules		
5.1	Contact size	2x2
5.2	Minimum poly overlap	1.5
5.3	Minimum contact spacing	2
5.4	Minimum spacing to gate of transistor	2



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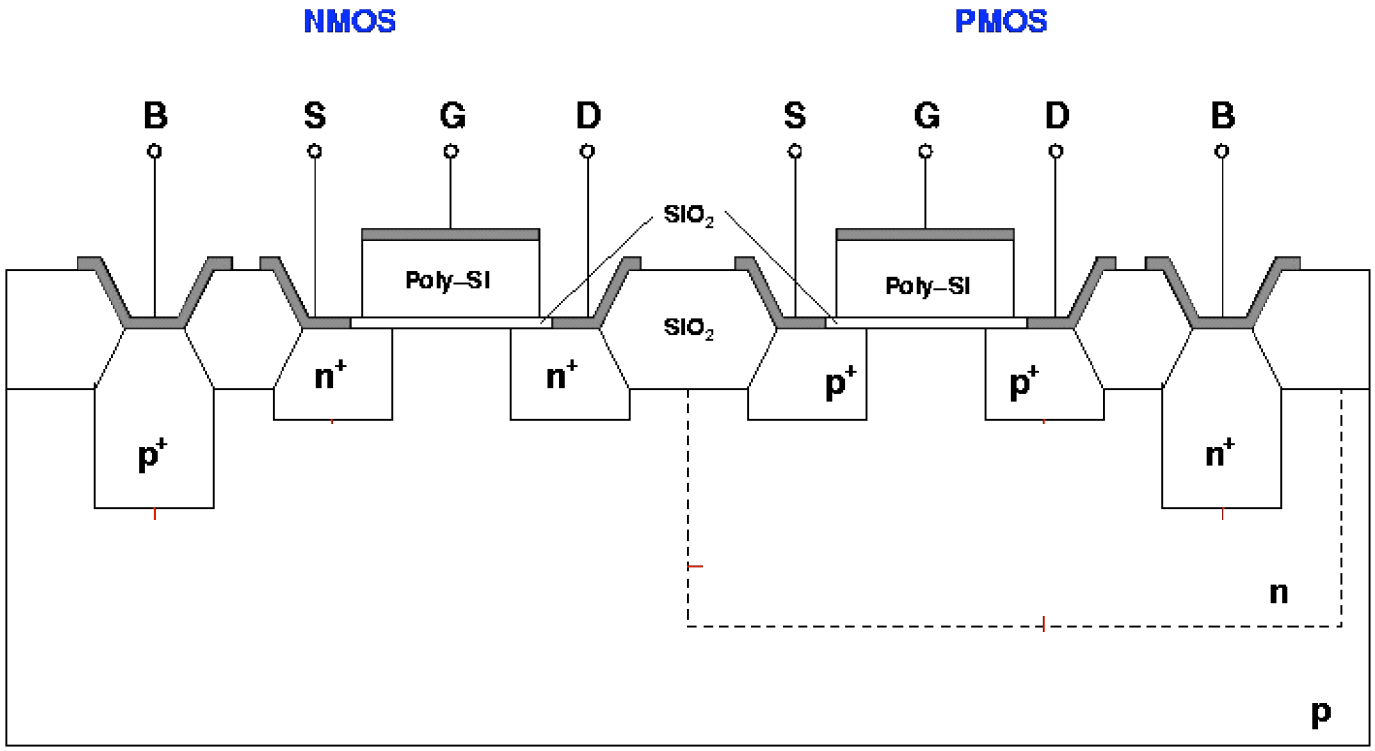
CMOS Latchup



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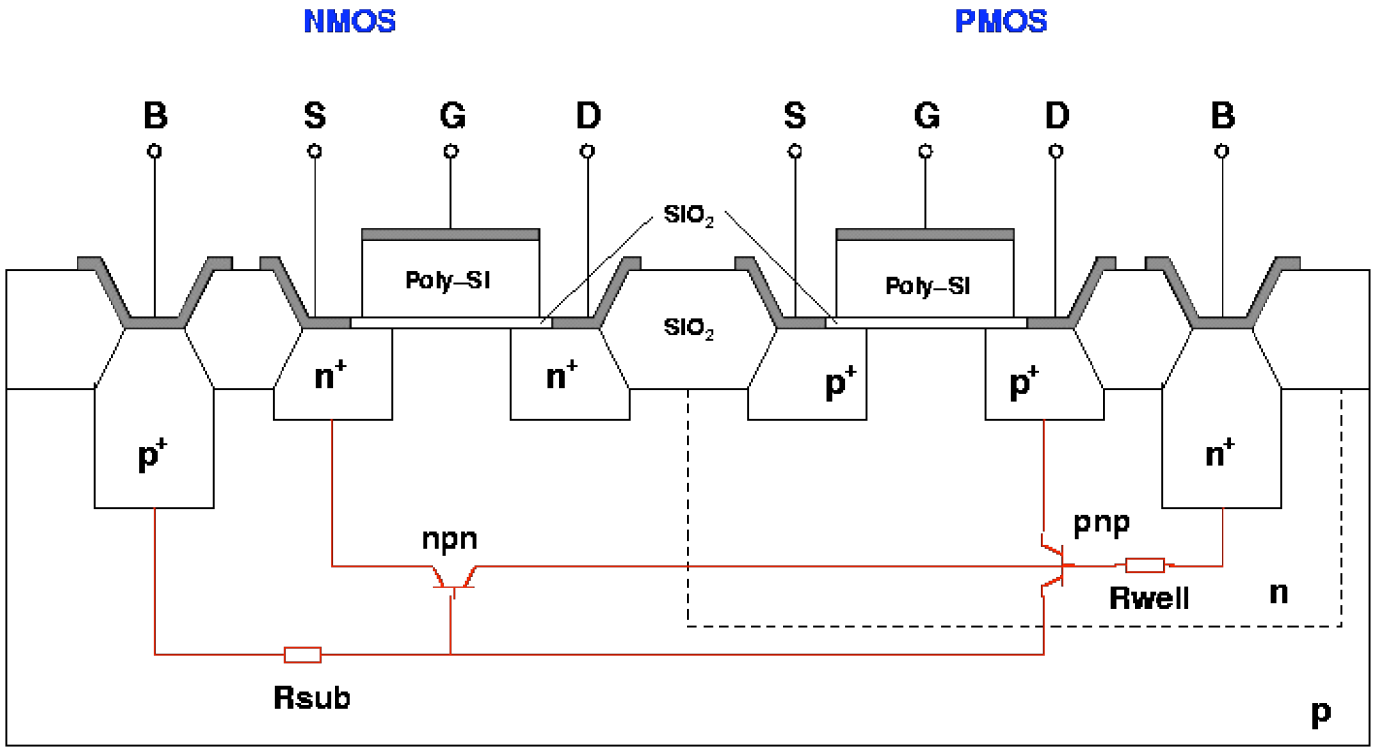
CMOS Latchup



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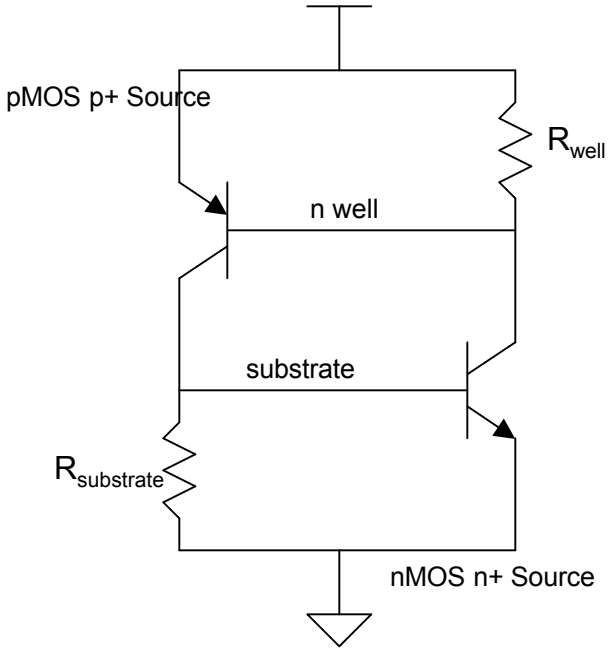
CMOS Latchup



- Acts like a SCR (silicon controlled rectifier)
- As long as both transistors are off, everything is fine

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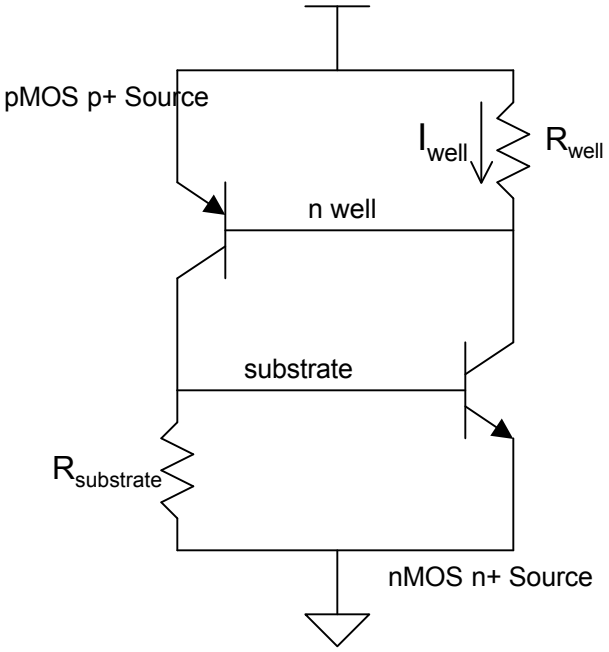
CMOS Latchup



- External disturbance causes current flow in R_{sub} or R_{well}
- Feedback loop will cause the current draw to increase dramatically

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CMOS Latchup

- External disturbances
  - ESD (electrostatic discharge) stress
  - Cosmic rays/alpha particles
  - Sudden transients on Vdd or Gnd
  - I/O pads interfacing with large currents off chip

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CMOS Latchup

- Avoiding latchup
  - Decrease R_{sub} and R_{well} so that it is harder to turn on the BJT transistors
    - Place substrate and well contacts close together
    - Keep pMOS transistors close to Vdd and nMOS transistors close to ground
    - Surround transistors in I/O pads with guard rings
  - Decrease β of BJT transistors
    - Space the pMOS and nMOS transistors apart

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Next Class

- Performance Characterization
- Read Chapter 4

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