VLSI Design and Simulation

Lecture 5

Performance Characterization

Topics

- Performance Characterization
  - Resistance Estimation
  - Capacitance Estimation
  - Inductance Estimation

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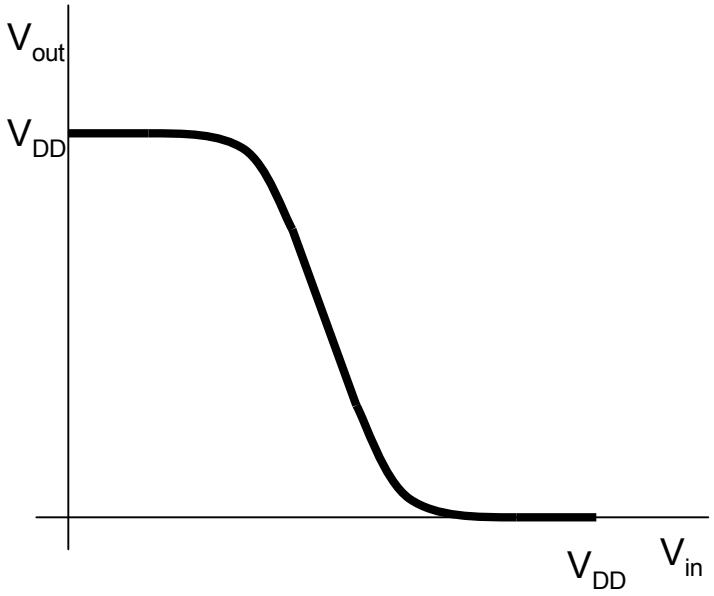
Performance Characterization

- Inverter Voltage Transfer Curve



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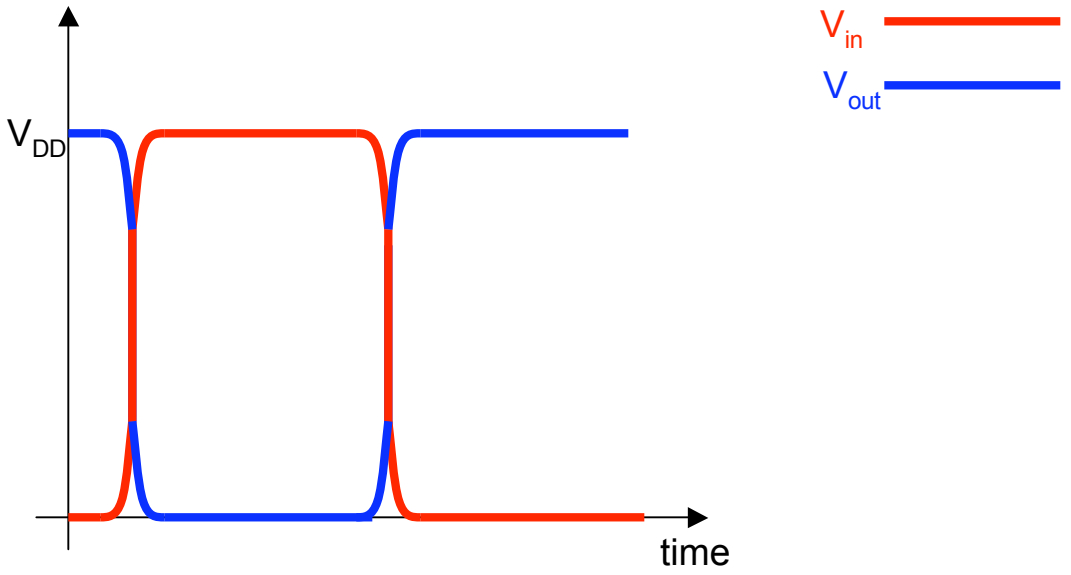
Performance Characterization

- Voltage versus Time curve (ideal)



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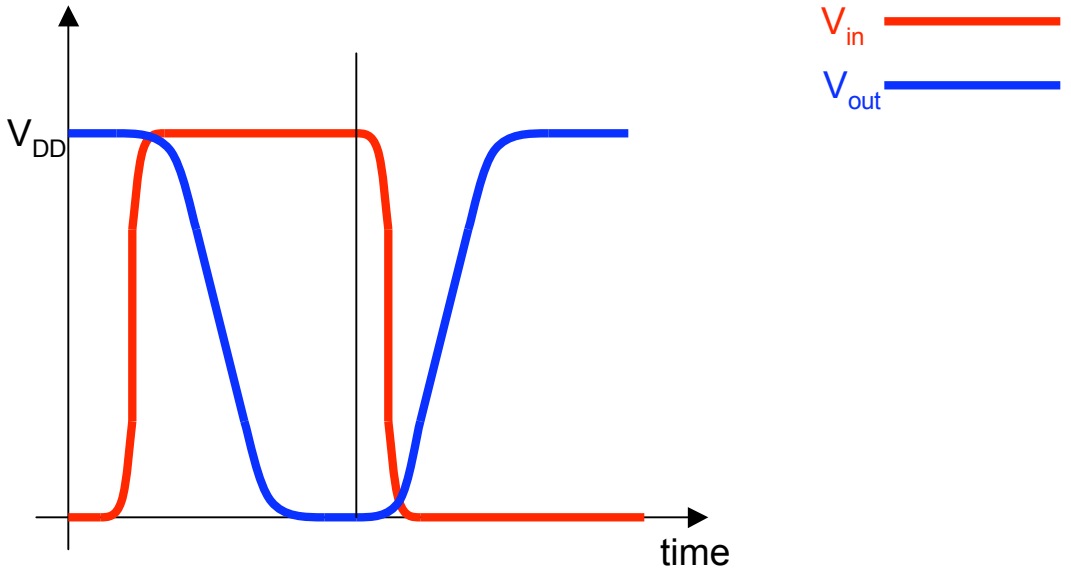
Performance Characterization

- Gate delay
- Voltage versus Time curve



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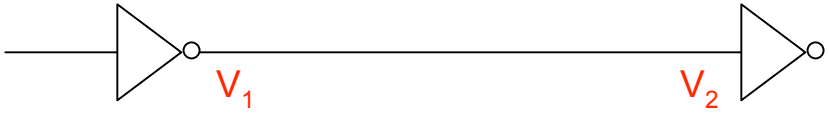
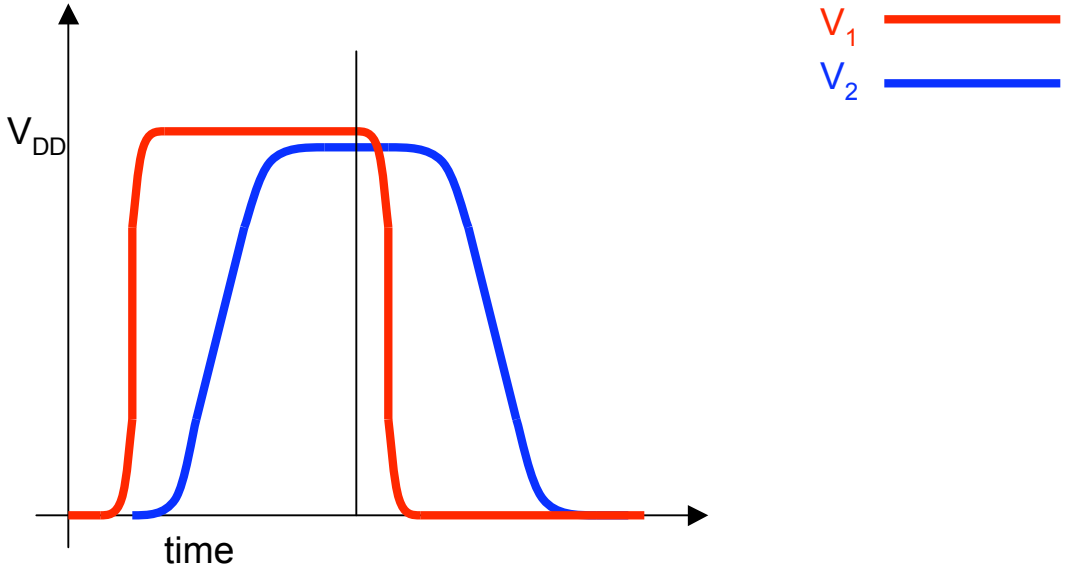
Performance Characterization

- Interconnect delay





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Performance Characterization

- Delay
  - Primary determinant of the speed of a circuit
  - Due to resistances and capacitances
    - Intrinsic resistance and capacitance
    - Extrinsic resistance and capacitance

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Resistance Estimation

- Dependent on resistivity of material
- Directly proportional to length
- Inversely proportional to cross-sectional area

$$R = \rho \frac{l}{A}$$

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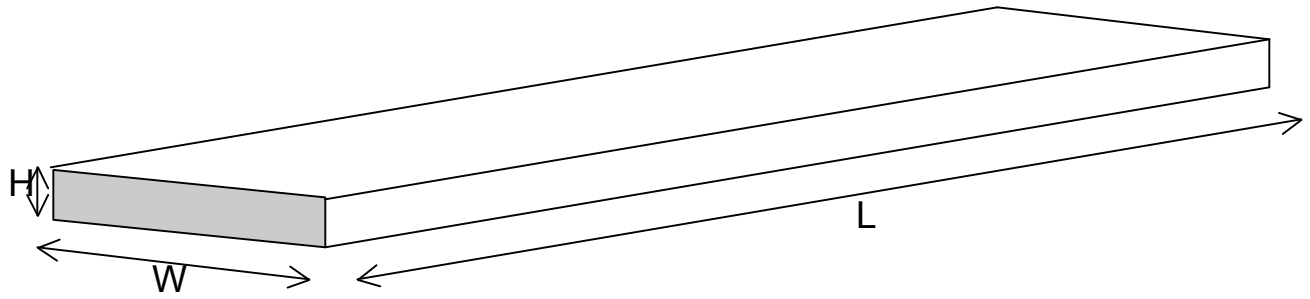
Resistance Estimation

$$R = \rho \frac{L}{A} = \frac{\rho}{H} \frac{L}{W} = R_S \frac{L}{W}$$



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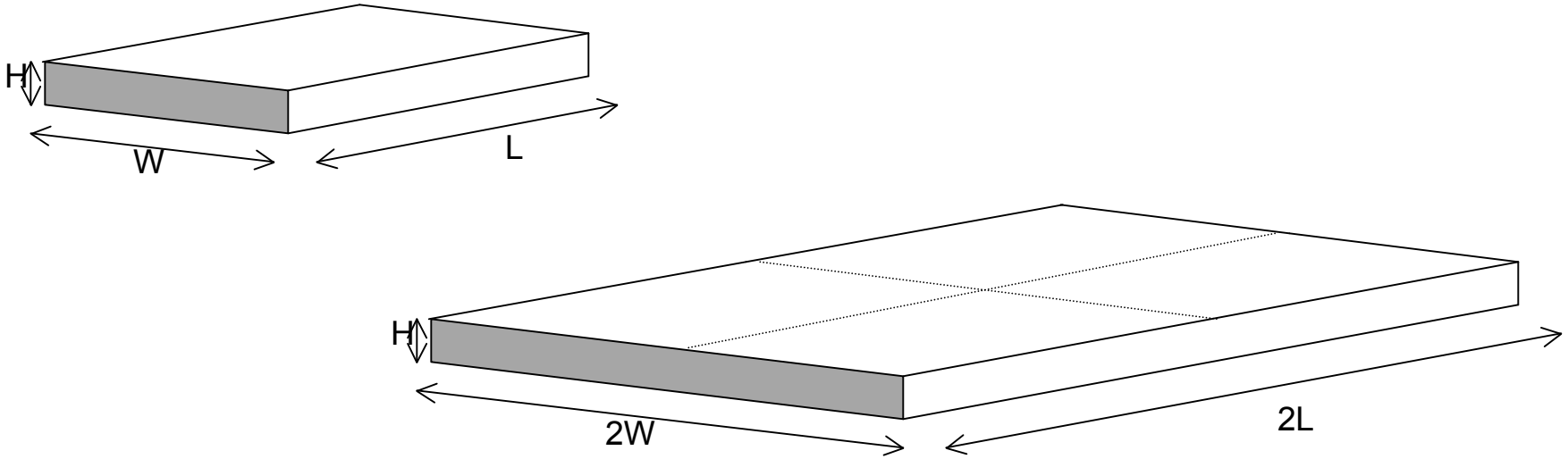
Resistance Estimation

- R_S is the sheet resistance expressed in terms of $\Omega/\square$



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Resistance Estimation

Interconnect Material	Typical Resistance (Ω/□)
Top metal	0.05-0.1
Polysilicon	150-200
Diffusion	50-150

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Resistance Estimation

- Intrinsic resistance
- In linear region

$$I_{DS} = k\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$R_{eq} = \frac{1}{k\left(V_{GS} - V_T\right)} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)} = \frac{1}{\mu C_{ox}\left(V_{GS} - V_T\right)}\frac{L}{W}$$

$$R_S = \frac{1}{\mu C_{ox}\left(V_{GS} - V_T\right)}$$

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Resistance Estimation

- Intrinsic resistance
  - Dependent on C_{ox} and carrier mobility
  - Temperature variant
  - Typically 1000-30000 Ω/□

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Capacitance Estimation

- Capacitance in concert with interconnect resistance is the primary determinant of interconnect delays
- Intrinsic capacitance
- Interconnect capacitances

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MOS device capacitances

- Overlap related capacitance
- Channel related capacitances
  - Dependent on region of operation
- Diffusion to substrate capacitances

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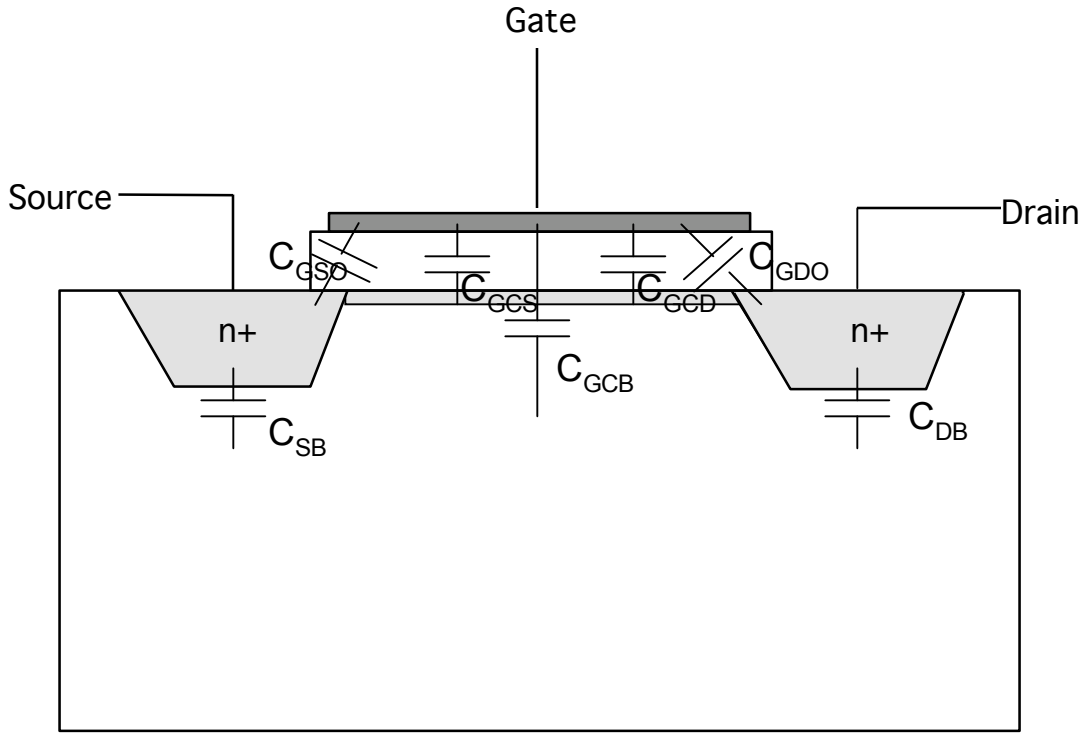
MOS device capacitances



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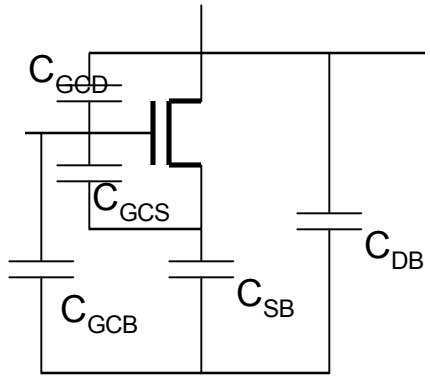
MOS device capacitances



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MOS device capacitances

- Overlap related capacitance

$$C_{GSO} = C_{DSO} = \frac{\varepsilon_{ox}}{t_{ox}} A_{overlap} = C_{ox} x_D W$$

- Usually can be ignored since x_D is very small

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MOS device capacitances

- Channel related capacitances
  - Cutoff
    - No channel
    - Therefore, no gate to source or drain capacitances

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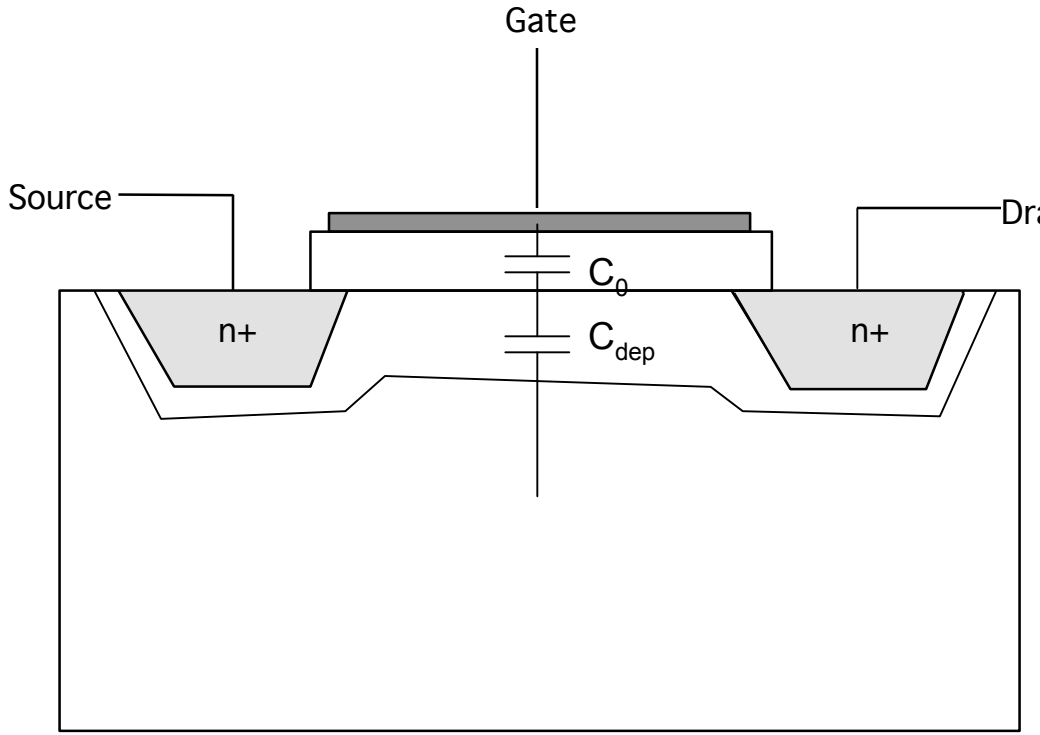
MOS device capacitances



$$C_{GCB} = \frac{C_0 C_{dep}}{C_0 + C_{dep}}$$

$$C_0 = C_{ox} WL$$

$$C_{dep} = \frac{\varepsilon_{silicon}}{d} WL$$

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MOS device capacitances

- Channel related capacitances
  - Cutoff
    - No channel
    - Therefore, no gate to source or drain capacitances
  - As gate voltage increases, depletion region deepens, causing C_{dep} to decrease, and thus decrease the gate to body capacitance
  - As gate voltage nears V_T, inversion channel forms causing a barrier for the gate to body capacitance

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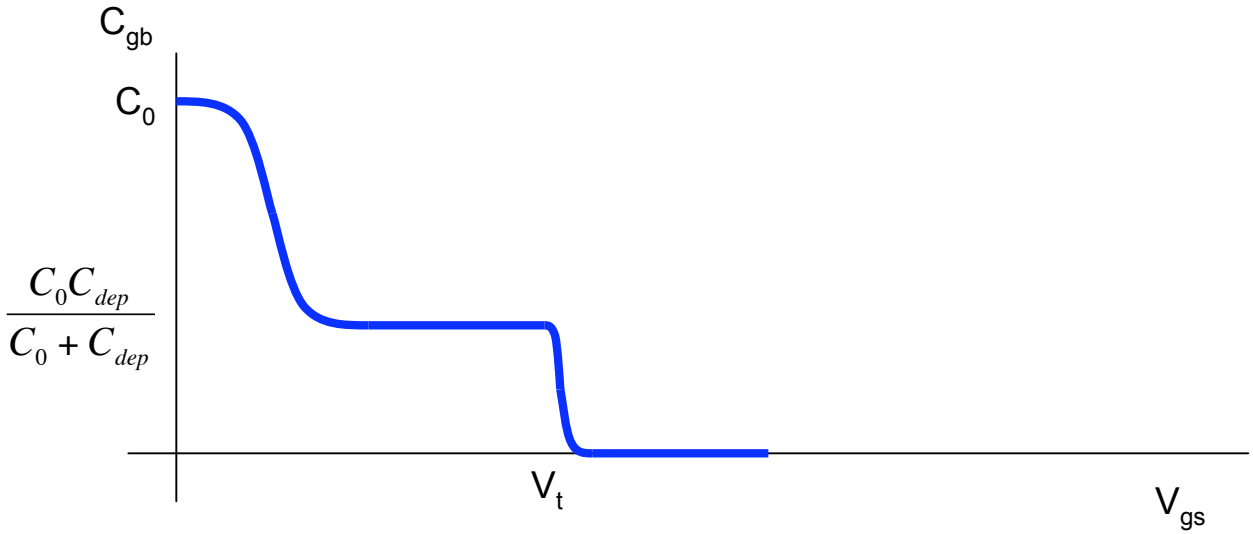
MOS device capacitances



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MOS device capacitances

- Channel related capacitances
  - Saturation
    - Channel is pinched off
    - Gate to source capacitance exists
    - Gate to drain capacitance is zero

$$C_{GCB} = \frac{2}{3} C_{ox} WL$$

$$C_{GCD} = 0$$

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MOS device capacitances

- Channel related capacitances
  - Linear
    - Channel is formed
    - Therefore, no gate to body capacitance

$$C_{GCS} = C_{GCD} = \frac{C_{ox}WL}{2}$$

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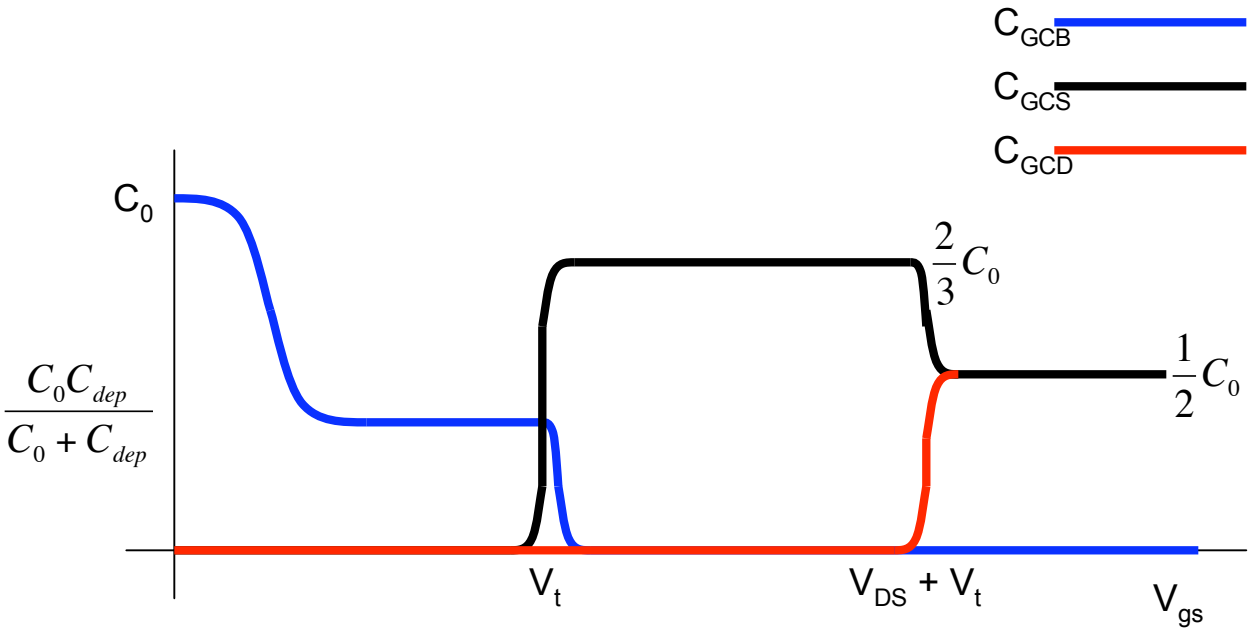
MOS device capacitances



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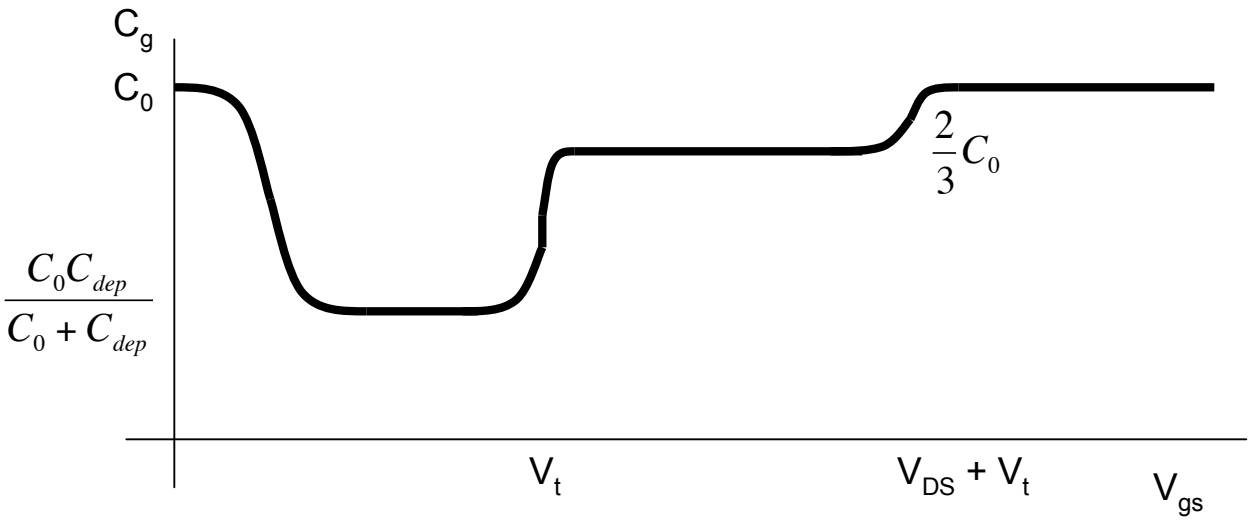
MOS device capacitances



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MOS device capacitance

- Channel related capacitance
- Worst case $C_g = C_{ox} WL$
- C_{ox} ranges from 1.7-6 fF/μm^2
- For a 1.5μ by 1.5μ channel

$$C_g = (6)(1.5)(1.5)$$
$$= 13.5\, fF$$

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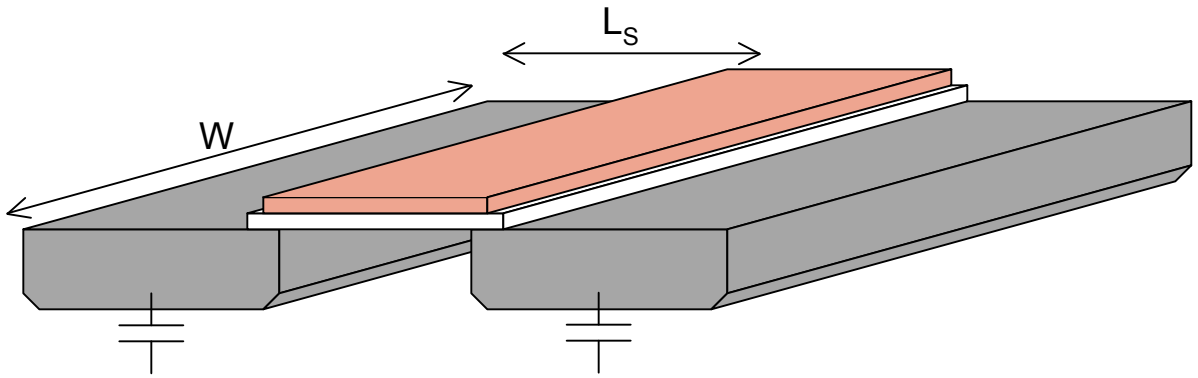
MOS device capacitances

- Diffusion to substrate capacitance
- Junction capacitance



$$C_{diff} = C_j L_S W$$

- C_j is the bottom-plate capacitance per area

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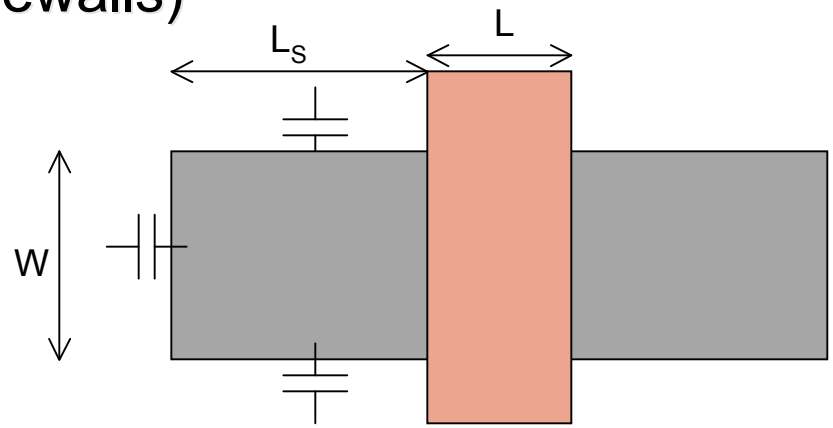
MOS device capacitances

- Side wall or periphery capacitance (drain and source sidewalls)



$$C_{diff} = C_{jsw}(2L_S + W)$$

- C_{jsw} is the side wall capacitance per linear distance

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MOS device capacitances

- C_j is typically .5-2 fF/μm^2
- C_{jsw} is typically .28-.4 fF/μm
- For a 1.5μ by 1.5μ diffusion region

$$\begin{aligned} C_{diff} &= C_j L_S W + C_{jsw}(2L_S + W) \\ &= 2(1.5)(1.5) + .28(3.0 + 1.5) \\ &= 5.8\, fF \end{aligned}$$

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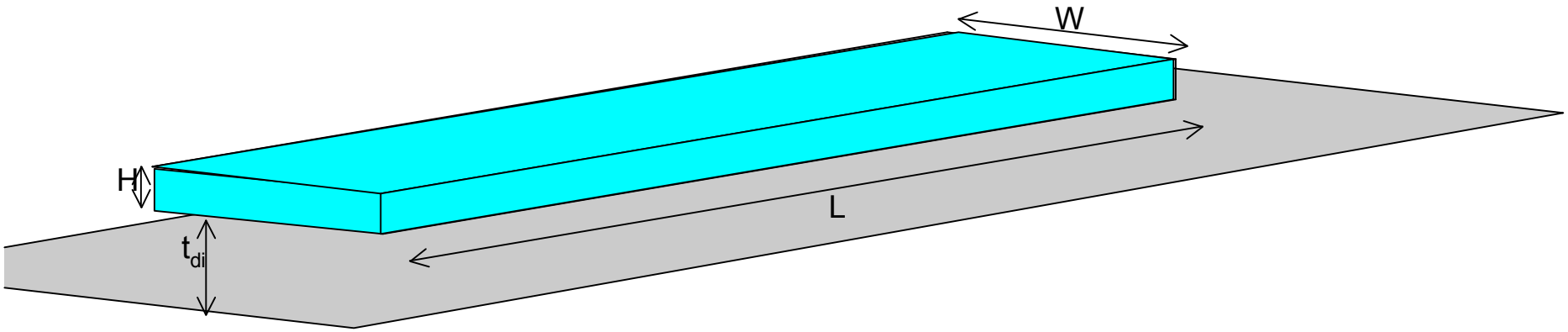
Interconnect capacitances



$$C_{plate} = \frac{\varepsilon_{di}}{t_{di}} WL$$

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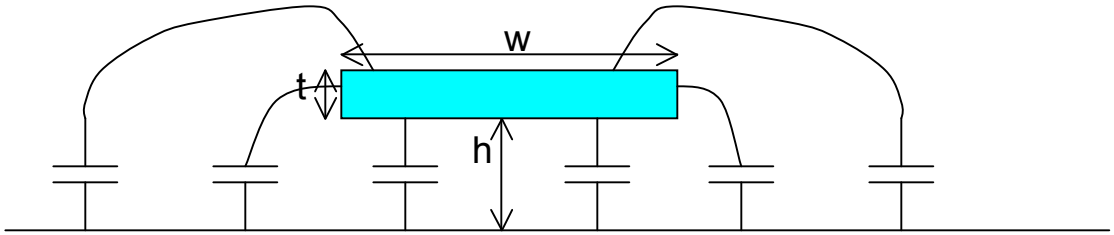
Interconnect capacitances



- When h is comparable in magnitude to t, fringing electric fields can increase the total effective parasitic capacitance
- The effect is magnified as the ratio of w to h decreases
- If w=h, the effective capacitance can be up to 10 times C_{plate}

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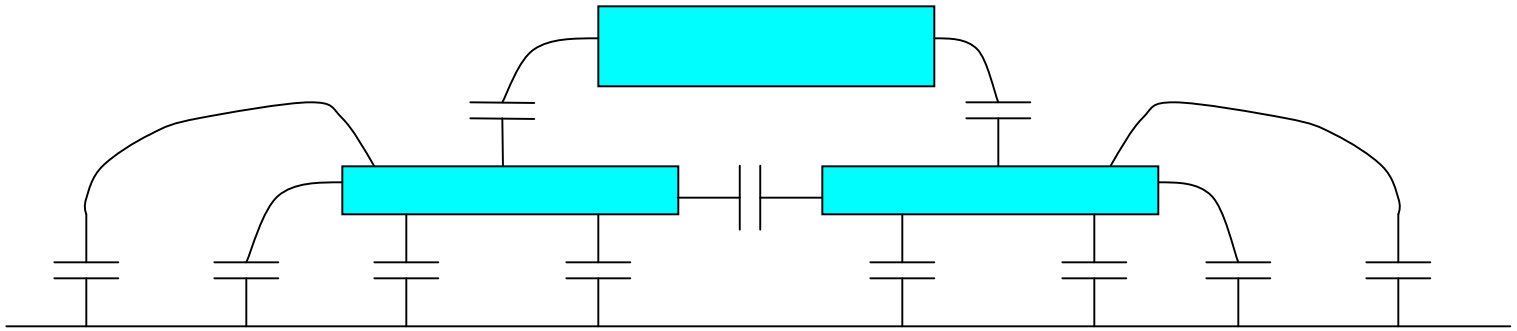
Cross-Interconnect capacitances



- Can be very difficult to compute
- Requires three dimensional field simulations
- Usually provided by process measurements

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Cross Interconnect Capacitances

.25μm process	Area (fF/μm$^{2)}$	Perimeter (fF/μm$^{)}$
Poly over oxide	.088	.054
Metal1 over oxide	.030	.040
Metal2 over oxide	.013	.025
Metal1 over poly	.057	.054
Metal2 over poly	.017	.029
Metal2 over Metal1	.036	.045

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Interconnect capacitances

- Can dominate the effect of the gate capacitance
- Example: 100μm metal1 line over oxide
  - Area capacitance: 100μm x 1μm x .030fF/μm^2 = 3 fF
  - Fringing capacitance: 100μm x 2 x .040fF/μm = 8.0 fF
  - Total capacitance: 11 fF

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Inductance

- For the most part is not an issue
- Wire inductance is on the order of 10s of pH per mm
- Small enough to ignore except for very high performance chips
- Inductance is usually higher for I/O interfaces

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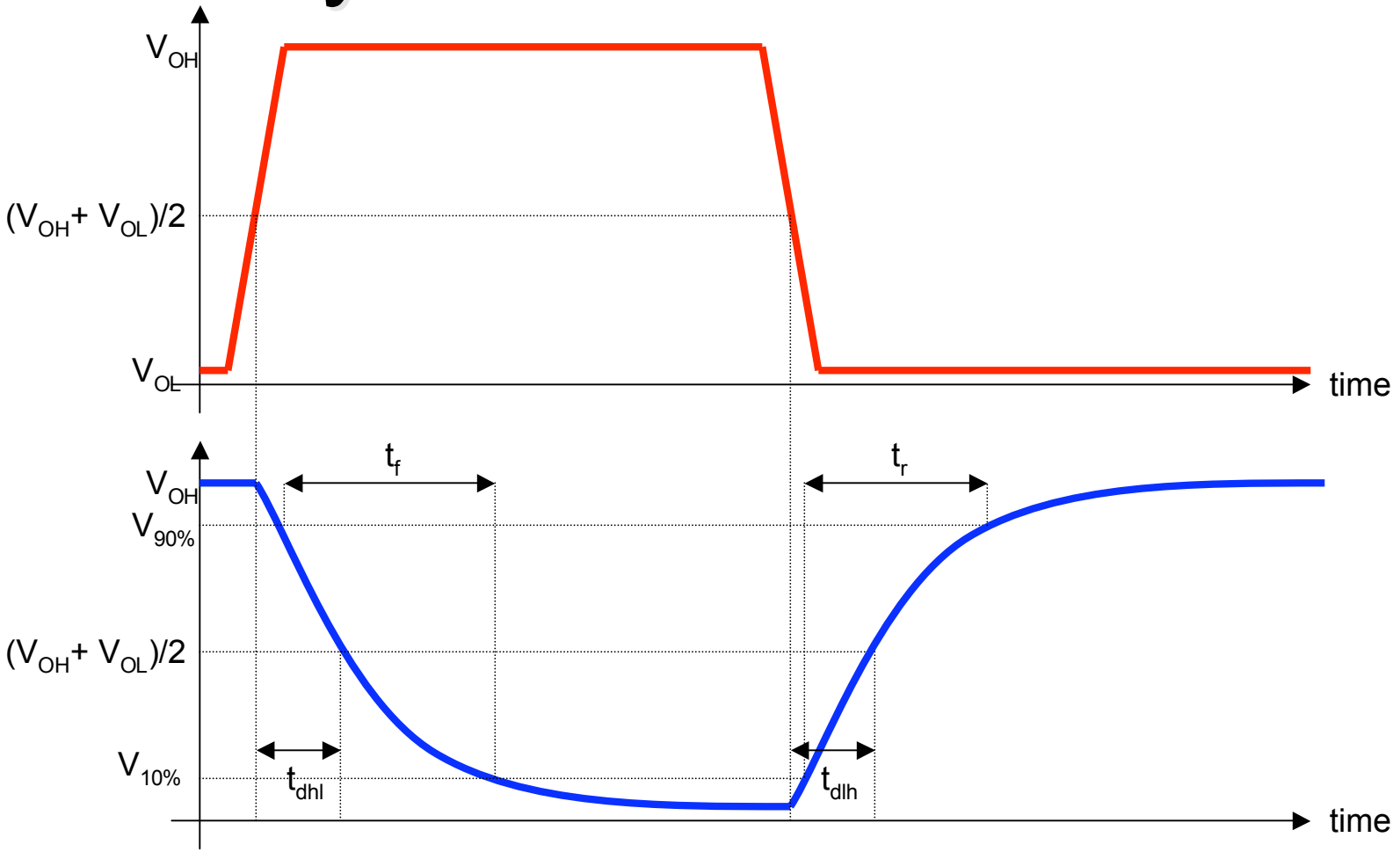
Delay Definitions



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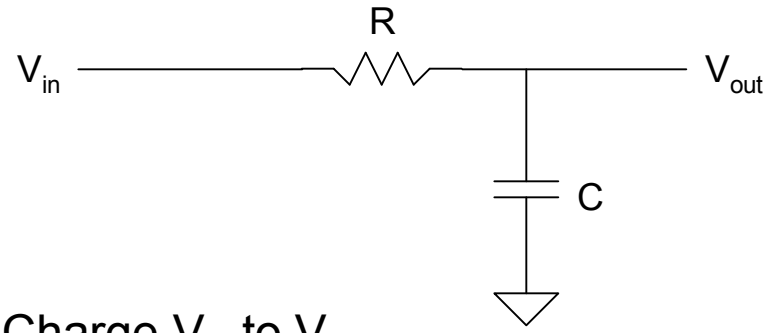
Interconnect delay



•Lumped RC model

•Charge V_{in} to V_{DD}

•The transient output voltage is $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t_{dlh}}{RC}}\right)$$

$$\frac{t_{dlh}}{RC} = -\ln\left(\frac{1}{2}\right)$$

$$t_{dlh} \approx .69RC$$

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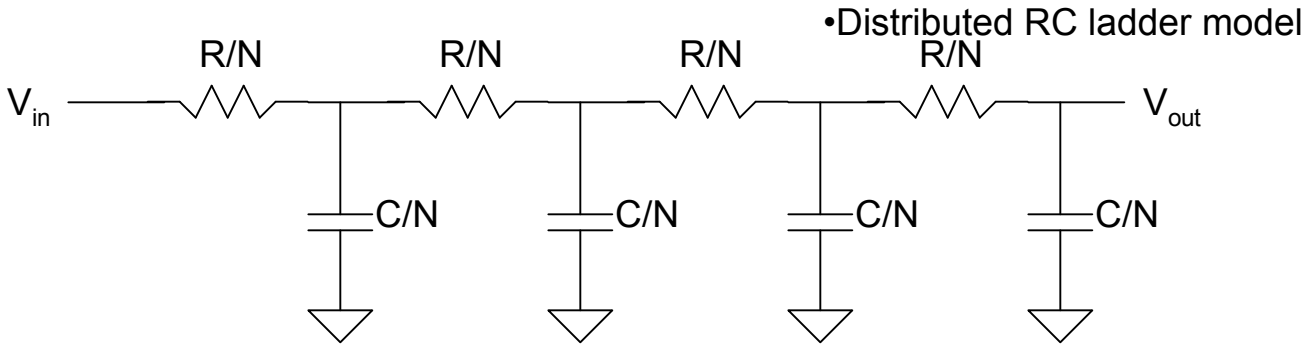
Interconnect delay



- More accurate than lumped RC model
- More difficult to solve for large N
- Need full-scale SPICE simulation

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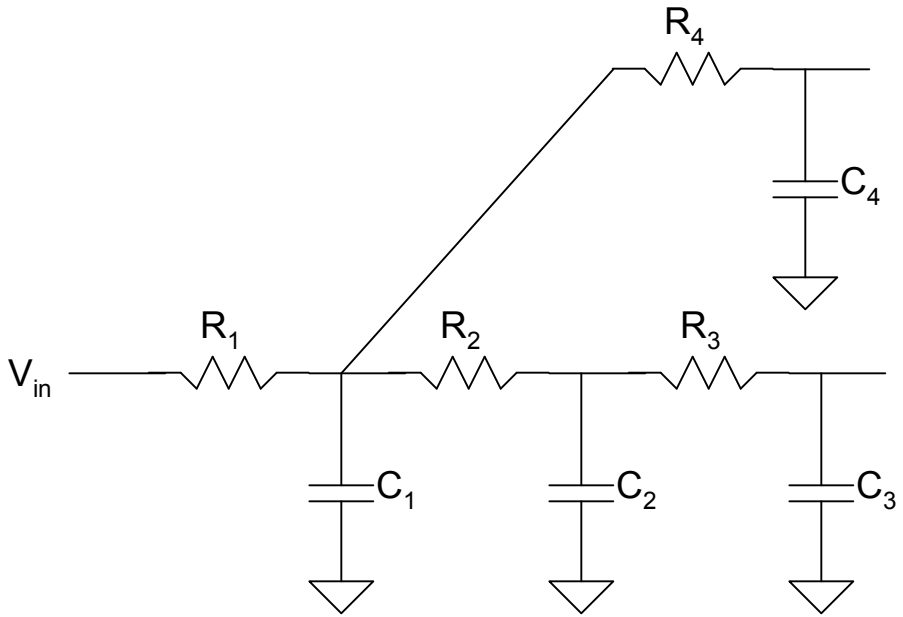
Elmore Delay

- Single line model not useful for generalized RC tree networks



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Next class

- More Performance Characterization

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