Topics

- Performance Characterization
  - Interconnect Delay
  - Gate Delay
  - Switching Characteristics

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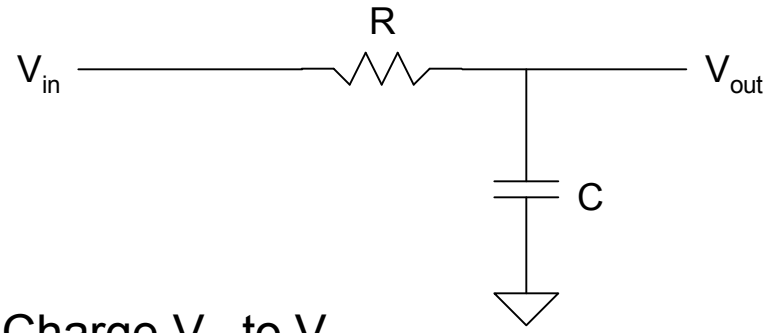
Interconnect delay



•Lumped RC model

•Charge V_{in} to V_{DD}

•The transient output voltage is $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$

$$\frac{V_{DD}}{2} = V_{DD}\left(1 - e^{-\frac{t_{dlh}}{RC}}\right)$$

$$\frac{t_{dlh}}{RC} = -\ln\left(\frac{1}{2}\right)$$

$$t_{dlh} \approx .69RC$$

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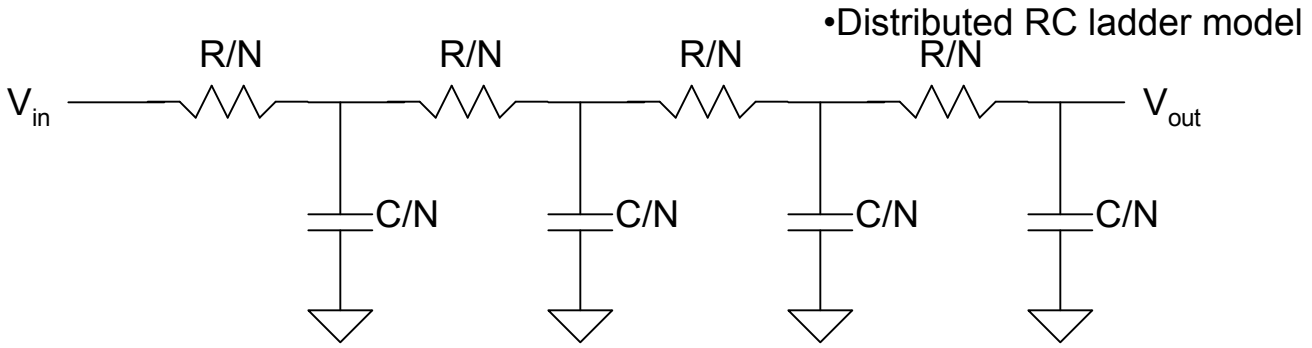
Interconnect delay



- More accurate than lumped RC model
- More difficult to solve for large N
- Need full-scale SPICE simulation

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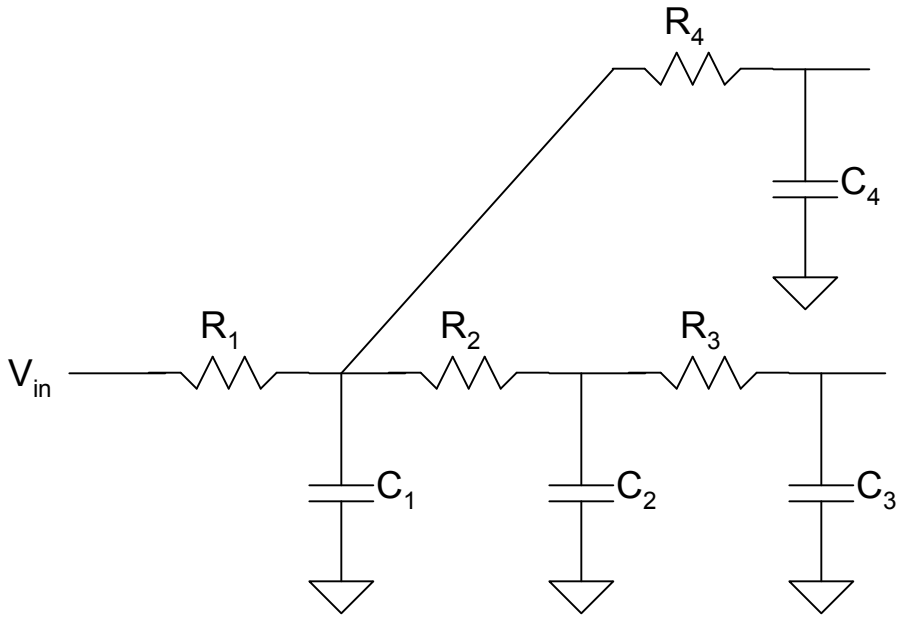
Elmore Delay

- Single line model not useful for generalized RC tree networks



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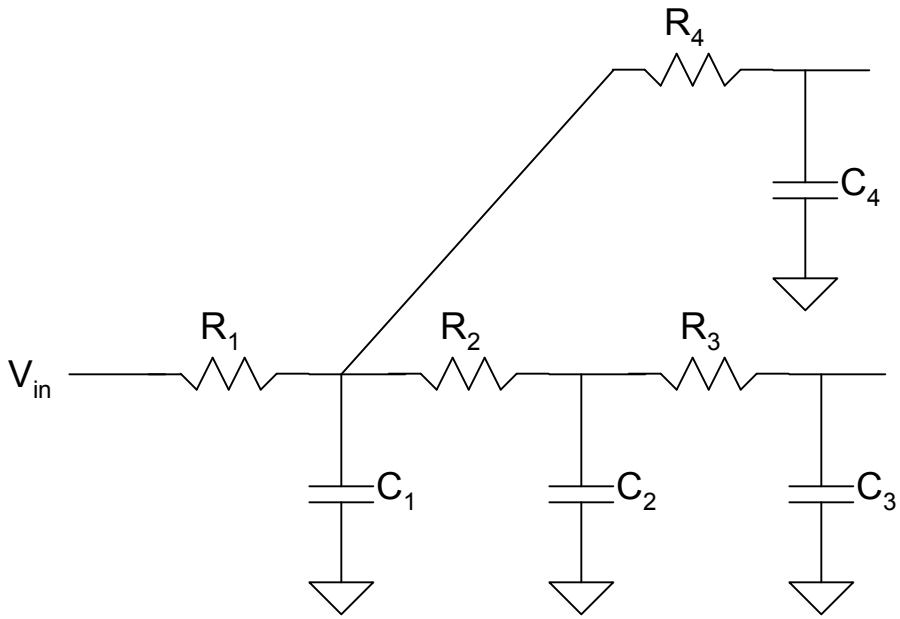
Elmore Delay

- First order calculation of time constant of the circuit

$$t_d = \sum_{j=1}^{N} C_j \sum_{k \in path} R_k$$



$$t_{d3} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + R_1C_4$$

$$t_{d4} = R_1C_1 + R_1C_2 + R_1C_3 + (R_1 + R_4)C_4$$

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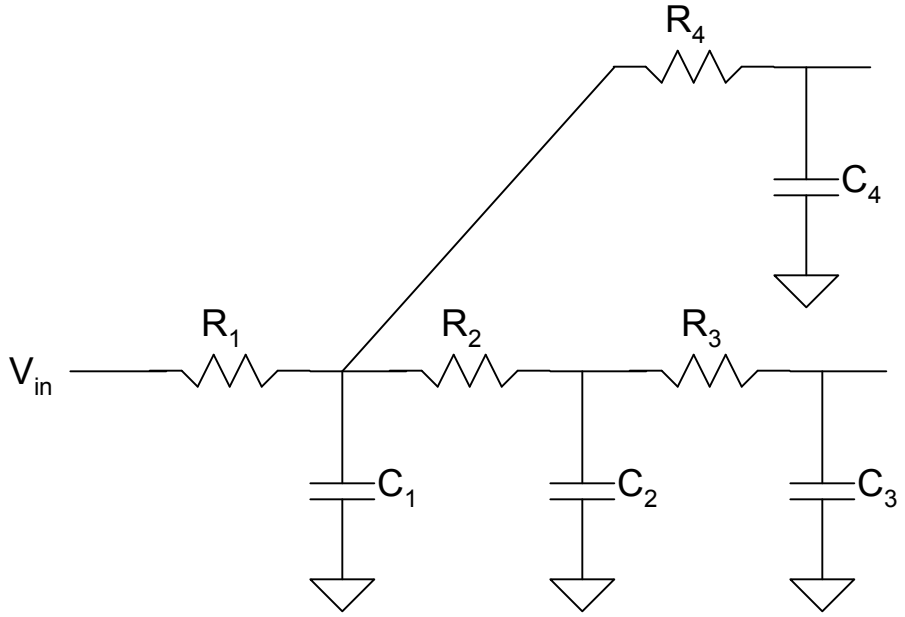
Elmore Delay

$$t_d = \sum_{j=1}^{N} C_j \sum_{k \in path} R_k$$

$$t_{d3} = R_1\left(C_1 + C_2 + C_3 + C_4\right) + R_2\left(C_2 + C_3\right) + R_3 C_3$$

$$t_{d4} = R_1\left(C_1 + C_2 + C_3 + C_4\right) + R_4 C_4$$



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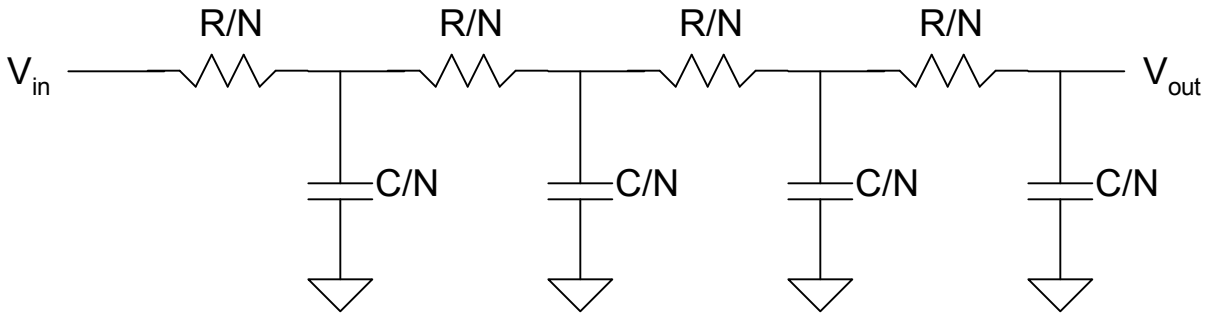
Elmore Delay



$$t_d = \sum_{j=1}^{N} \frac{C}{N} \sum_{k=1}^{j} \frac{R}{N}$$

$$= \frac{C}{N}\frac{R}{N}\frac{N(N+1)}{2} = RC\left(\frac{N+1}{2N}\right)$$

$$t_d = \frac{RC}{2} \quad \text{for} \quad N \to \infty$$

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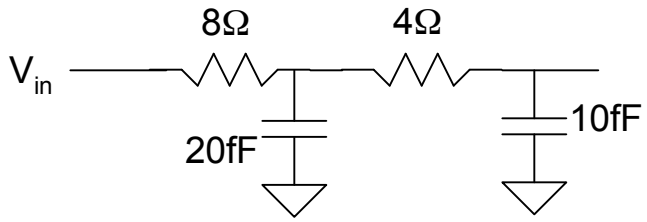
Interconnect Delay

$$t_d = 8\Omega\left(20\,fF + 10\,fF\right) + 4\Omega\left(10\,fF\right)$$
$$= .28\,ps$$



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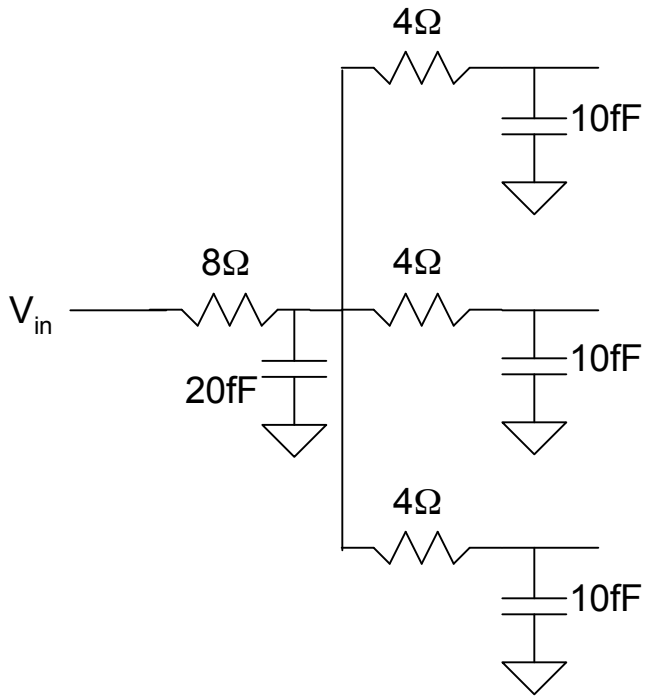
Interconnect Delay

$$t_d = 8\Omega\left(20\,fF + 10\,fF + 10\,fF + 10\,fF\right) + 4\Omega\left(10\,fF\right)$$
$$= .44\,ps$$



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Interconnect Delay

- Fanout Effects
  - Lines with multiple loads will have longer delays
    - Clocks
    - Data buses
    - Control lines
  - Solutions
    - Wider and thicker lines for special signals
    - Buffer drivers

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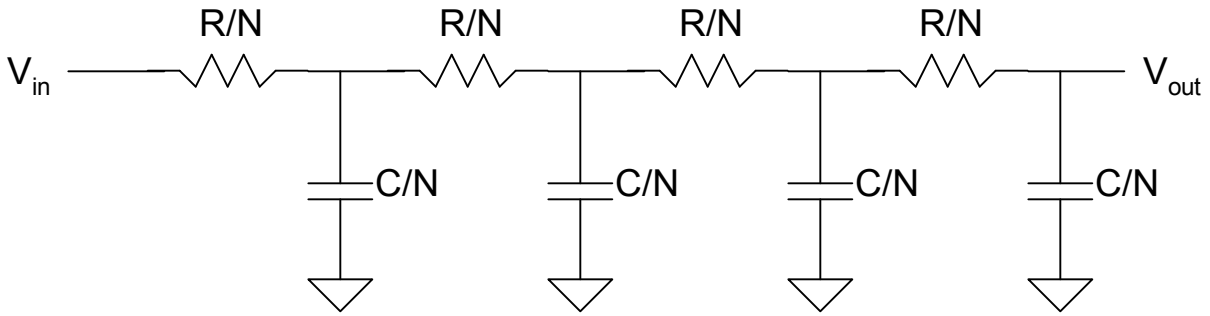
Interconnect Delay



$$t_d = \sum_{j=1}^{N} \frac{C}{N} \sum_{k=1}^{j} \frac{R}{N}$$

$$= \frac{C}{N}\frac{R}{N}\frac{N(N+1)}{2} = RC\left(\frac{N+1}{2N}\right)$$

$$t_d = \frac{RC}{2} \quad \text{for} \quad N \rightarrow \infty$$

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Interconnect Delay

$$
\begin{aligned}
t_d &= \frac{RC}{2} \\
&= \frac{1}{2}\left(r\frac{l}{w}\right)\left(c_a lw + c_p\left(l+w\right)\right) \\
&\approx \frac{1}{2} r c_a l^2
\end{aligned}
$$

- Delay is proportional to the square of the length
- Try to avoid long lines

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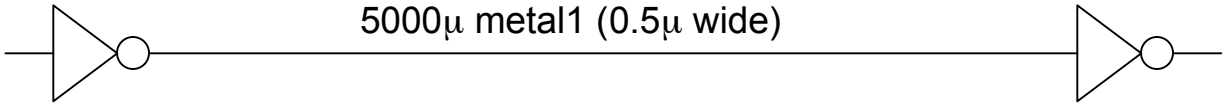
Interconnect Delay



•Interconnect resistance

$$R = .07\frac{5000\mu}{0.5\mu} = 700\Omega$$

•Interconnect capacitance

$$C_{wire} = .03 \cdot 5000\mu \cdot 0.5\mu + .044 \cdot 2 \cdot (5000\mu + 0.5\mu) = 515\,fF$$

•Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

•Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = \frac{700 \cdot 515\,fF}{2} + 700 \cdot 5\,fF = 184\,ps$$

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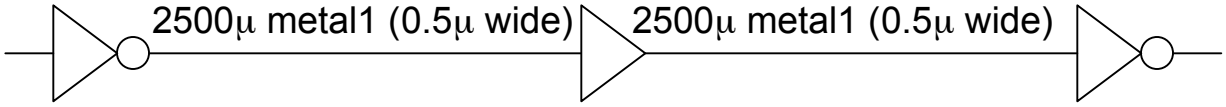
Interconnect Delay

- Avoid long interconnect delays using buffers



•Interconnect resistance

$$R = .07\frac{2500\mu}{0.5\mu} = 350\Omega$$

•Interconnect capacitance

$$C_{wire} = .03 \cdot 2500\mu \cdot 0.5\mu + .044 \cdot 2 \cdot (2500\mu + 0.5\mu) = 258\,fF$$

•Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

•Propagation delay

$$t_p = 2 \cdot \left(\frac{RC_{wire}}{2} + RC_{in}\right) = 2 \cdot \left(\frac{350 \cdot 258\,fF}{2} + 350 \cdot 5\,fF\right) = 94\,ps$$

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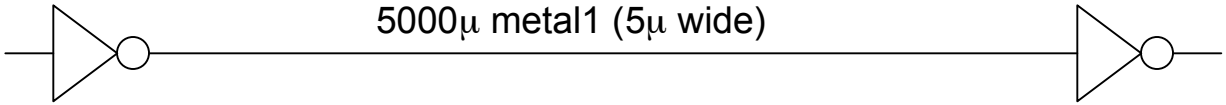
Interconnect Delay

- Avoid long interconnect delays using wider lines



•Interconnect resistance

$$R = .07\frac{5000\mu}{5\mu} = 70\Omega$$

•Interconnect capacitance

$$C_{wire} = .03 \cdot 5000\mu \cdot 5\mu + .044 \cdot 2 \cdot (5000\mu + 5\mu) = 1190\,fF$$

•Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

•Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = \frac{70 \cdot 1190\,fF}{2} + 70 \cdot 5\,fF = 42\,ps$$

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Interconnect delay

- Interconnect sizing
  - Adjust delays
  - Prevent metal migration
  - Power supply noise and signal integrity

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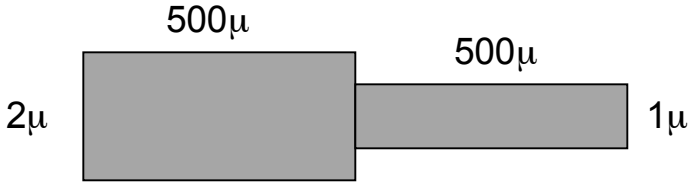
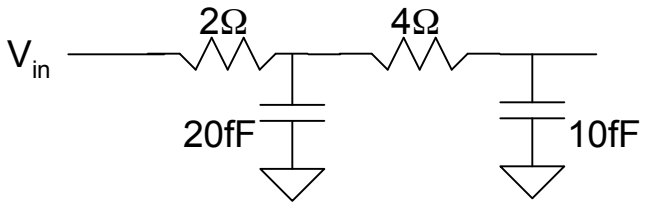
Interconnect Delay

- Directional Behavior

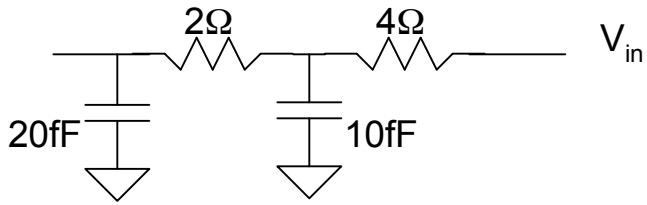


R_S=.08 Ω/□

C_a=.02 fF/μ²



$$t_d = 2\Omega(20\,fF + 10\,fF) + 4\Omega(10\,fF)$$
$$= .10\,ps$$



$$t_d = 4\Omega(10\,fF + 20\,fF) + 2\Omega(20\,fF)$$
$$= .16\,ps$$

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Switching Delay

- The intrinsic delay of a gate
- Transistor sizing can affect the delay
- Extrinsic capacitances can affect the delay

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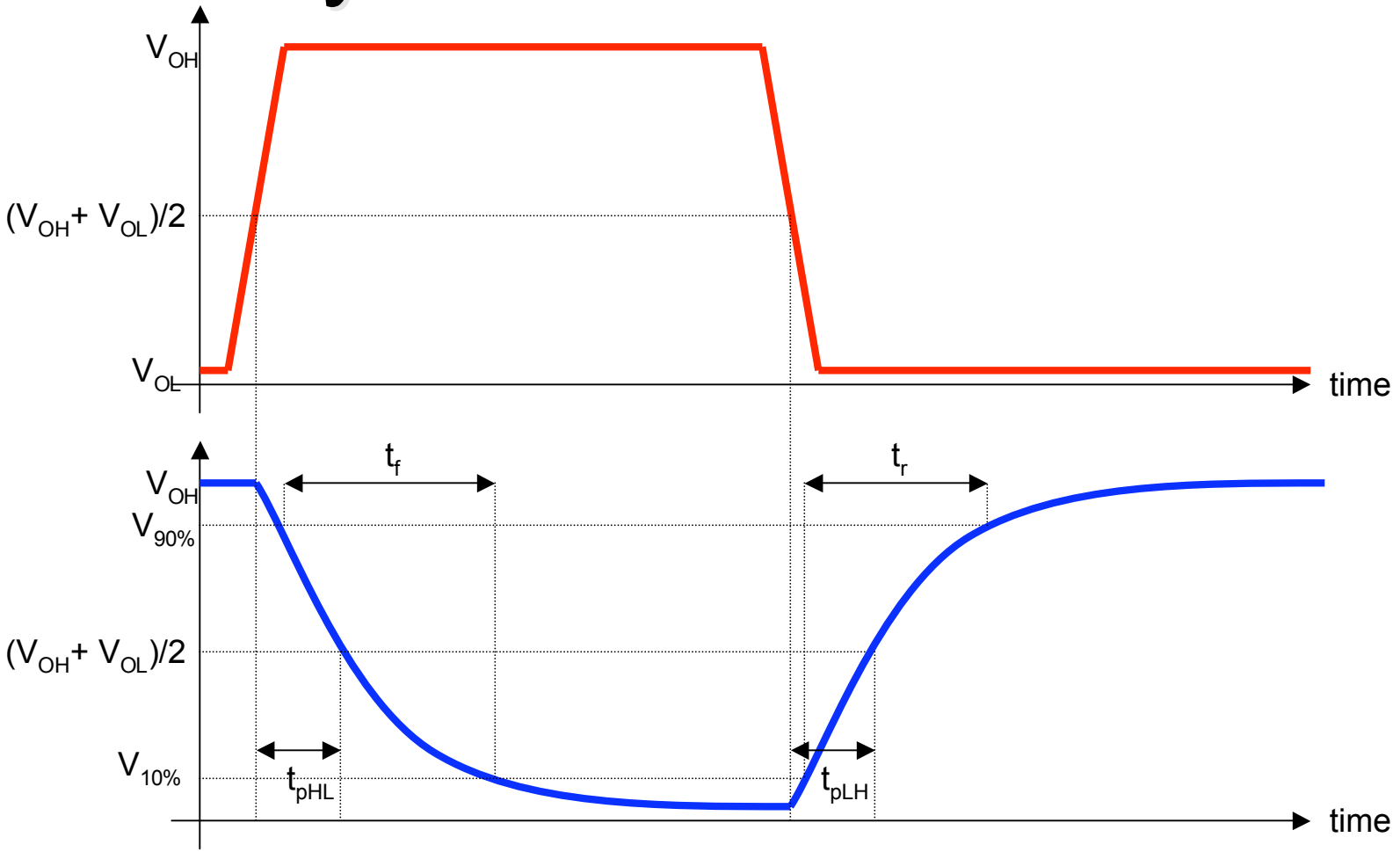
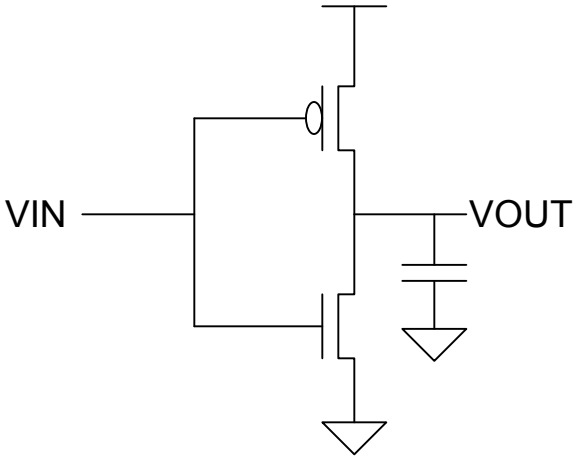
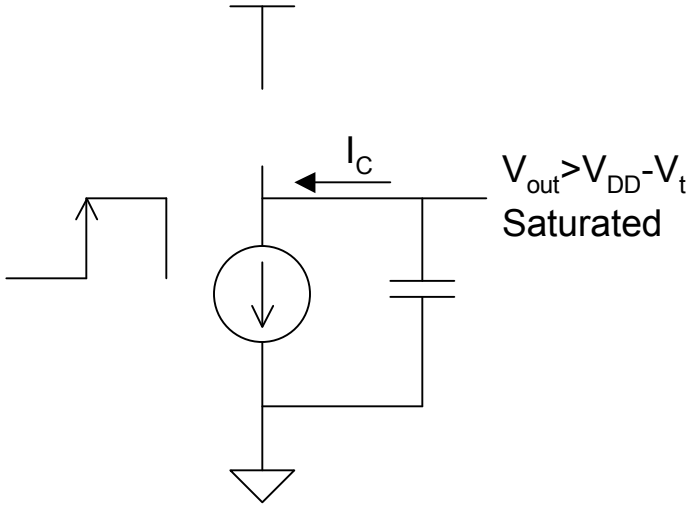
Delay Definitions



Switching Delay

- Fall time analysis





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Fall time analysis

- Saturated Mode

$$I_C = I_{DS}$$

$$-C_L \frac{dV_{out}}{dt} = k_n \frac{\left(V_{DD} - V_{tn}\right)^2}{2}$$

$$dt = -2 \frac{C_L}{k_n \left(V_{DD} - V_{tn}\right)^2} dV_{out}$$

$$t_{f1} = 2 \frac{C_L}{k_n \left(V_{DD} - V_{tn}\right)^2} \int_{V_{DD}-V_{tn}}^{.9V_{DD}} dV_{out}$$

$$t_{f1} = 2 \frac{C_L \left(V_{tn} - .1V_{DD}\right)}{k_n \left(V_{DD} - V_{tn}\right)^2}$$

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Fall time analysis

- Linear Mode

$$I_C = I_{DS}$$

$$-C_L \frac{dV_{out}}{dt} = k_n \left[(V_{DD} - V_{tn}) V_{out} - \frac{{V_{out}}^2}{2} \right]$$

$$dt = \frac{-2C_L}{k_n \left(2(V_{DD} - V_{tn}) V_{out} - {V_{out}}^2 \right)} dV_{out}$$

$$t_{f2} = \frac{-2C_L}{k_n} \int_{.1V_{DD}}^{V_{DD} - V_{tn}} \frac{dV_{out}}{\left(2V_{out}(V_{DD} - V_{tn}) - {V_{out}}^2 \right)}$$

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Fall time analysis

- Linear Mode

$$t_{f2} = \frac{C_L}{k_n\left(V_{DD} - V_{tn}\right)} \ln\left(\frac{V_{out}}{2\left(V_{DD} - V_{tn}\right) - V_{out}} \right) \Bigg|_{.1V_{DD}}^{V_{DD} - V_{tn}}$$

$$= \frac{C_L}{k_n\left(V_{DD} - V_{tn}\right)} \ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}} \right)$$

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Fall time analysis

$$t_f = t_{f1} + t_{f2}$$

$$= \frac{C_L}{k_n\left(V_{DD} - V_{tn}\right)}\left(\frac{2\left(V_{tn} - .1V_{DD}\right)}{V_{DD} - V_{tn}} + \ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}}\right)\right)$$

$$= \frac{C_L}{k_n V_{DD}\left(1-n\right)}\left(\frac{2\left(n - .1\right)}{1-n} + \ln\left(19 - 20n\right)\right) \qquad n = \frac{V_{tn}}{V_{DD}}$$

$$K = \frac{1}{\left(1-n\right)}\left(\frac{2\left(n - .1\right)}{1-n} + \ln\left(19 - 20n\right)\right)$$

$$t_f = K\frac{C_L}{k_n V_{DD}}$$

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Fall time analysis

- Fall time is proportional to load capacitance and inversely proportional to V_{DD} and k_n
- Decreasing the supply voltage will increase the fall time
- Increasing the transistor width will increase k which will reduce the fall time
- Changing these three parameters can cause conflicting goals

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Rise time analysis

$$t_r = \frac{C_L}{k_p V_{DD}(1-p)}\left(\frac{2(p-.1)}{1-p} + \ln(19-20p)\right)$$

$$K_p = \frac{1}{(1-p)}\left(\frac{2(p-.1)}{1-p} + \ln(19-20p)\right) \qquad p = \frac{-V_{tp}}{V_{DD}}$$

$$t_r = K_p \frac{C_L}{k_p V_{DD}}$$

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Rise time analysis

- For equal fall times and rise times

$$t_f = t_r$$

$$K_n \frac{C_L}{k_n V_{DD}} = K_p \frac{C_L}{k_p V_{DD}}$$

$$k_n = k_p$$

$$\mu_n C_{ox}\left(\frac{W_n}{L}\right) = \mu_p C_{ox}\left(\frac{W_p}{L}\right)$$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \approx 2 - 3$$

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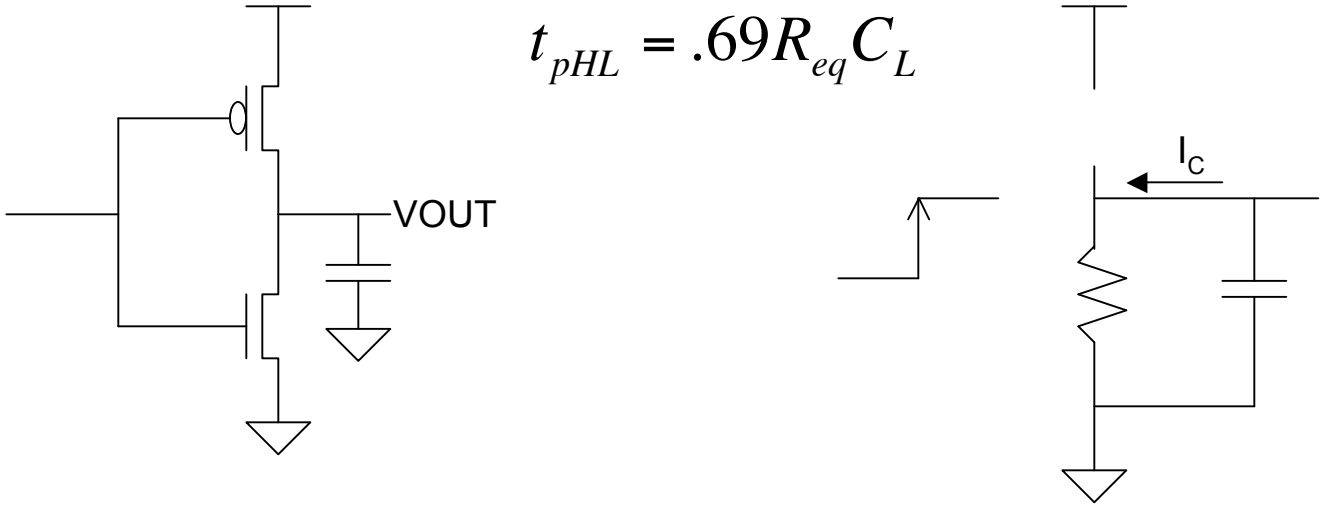
Propagation Delay

- As with interconnect delay, find the equivalent resistance and load capacitance of the transistor

$$t_{pHL} = .69 R_{eq} C_L$$



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Propagation Delay

$$R_{eq} = \text{average}\left(R_{on}(t)\right) = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2}\frac{V_{DS}(t)}{I_{DS}(t)}$$

- Propagation delay is the time for voltage to reach half way point - so integrate from V_{DD} to $V_{DD}/2$

$$R_{eq} = \frac{1}{V_{DD}/2 - V_{DD}}\int_{V_{DD}}^{V_{DD}/2}\frac{V_{DS}(t)}{I_{DS}(t)}dV_{DS}$$

- For the output range we are interested in, the transistor is always in saturation

$$R_{eq} = \frac{-2}{V_{DD}}\int_{V_{DD}}^{V_{DD}/2}\frac{V_{DS}}{I_{DSAT}\left(1+\lambda V_{DS}\right)}dV_{DS}$$

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Propagation Delay

$$R_{eq} = \frac{-2}{V_{DD}} \int_{V_{DD}}^{V_{DD}/2} \frac{V_{DS}}{I_{DSAT}\left(1+\lambda V_{DS}\right)} dV_{DS}$$

$$= \frac{2}{V_{DD}\lambda^2 I_{DSAT}} \left(\lambda V_{DS} - \ln\left(1+\lambda V_{DS}\right)\right)\Big|_{V_{DD}/2}^{V_{DD}}$$

$$= \frac{2}{V_{DD}\lambda^2 I_{DSAT}} \left(\lambda V_{DS} - \left(\lambda V_{DS} - \frac{\lambda^2 V_{DS}^2}{2} + \frac{\lambda^3 V_{DS}^3}{3} - \cdots\right)\right)\Big|_{V_{DD}/2}^{V_{DD}}$$

$$= \frac{2}{V_{DD} I_{DSAT}} \left(\frac{V_{DS}^2}{2} - \frac{\lambda V_{DS}^3}{3} + \cdots\right)\Big|_{V_{DD}/2}^{V_{DD}}$$

$$= \frac{2}{V_{DD} I_{DSAT}} \left(\frac{3V_{DD}^2}{8} - \frac{7\lambda V_{DD}^3}{24} + \cdots\right)$$

$$\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

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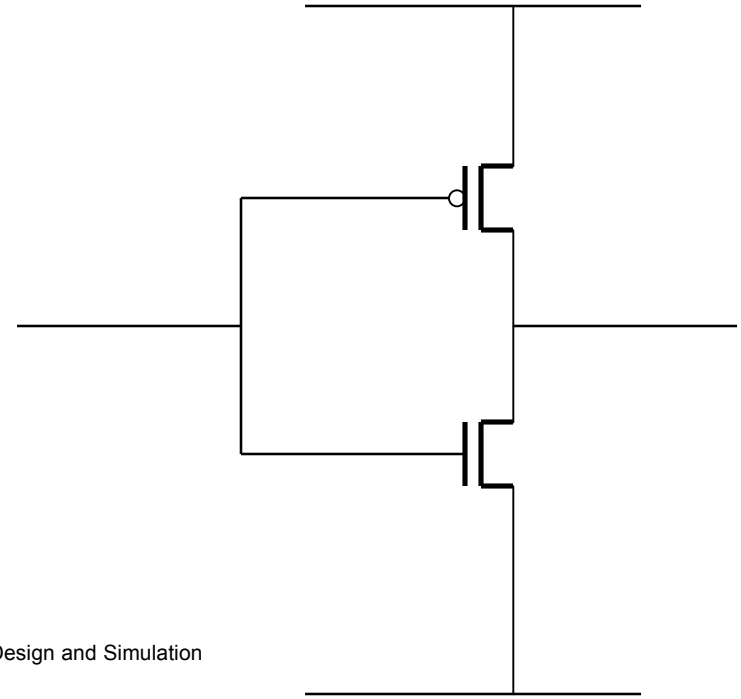
Propagation Delay

- Load capacitance



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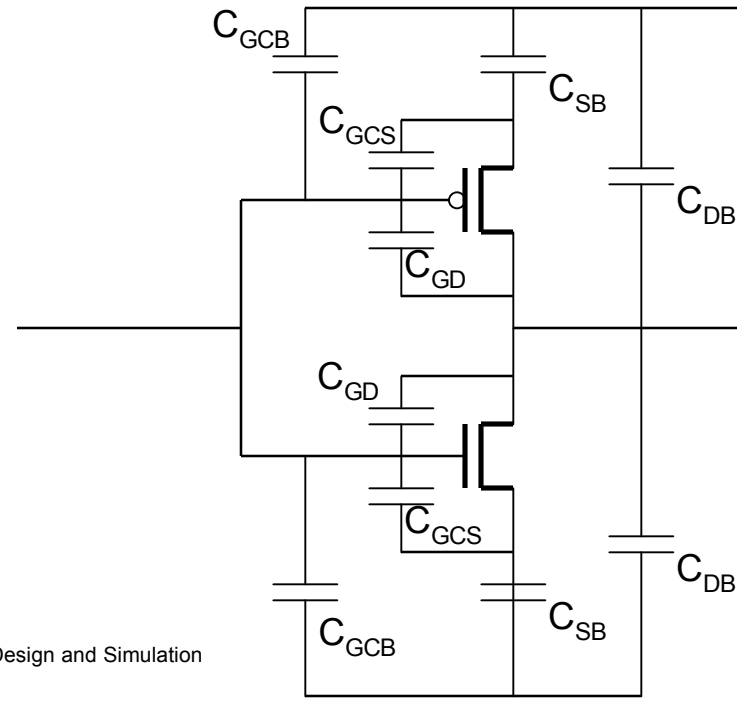
Propagation Delay

- Load capacitance
  - Intrinsic capacitance - sum of capacitances at drain - C_{GD}+ C_{DB}



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Propagation Delay

- Intrinsic Capacitance
  - C_{GD} is composed solely of overlap capacitance
    - The transistors are either in cutoff or in saturation, so no channel capacitance exists
  - The actual load capacitance relative to ground is $2C_{GDO}$ because of Miller efffect

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Propagation Delay

$$t_{pLH} = 0.69 R_{eq}\left(2C_{GDOn} + 2C_{GDOp} + C_{DBn} + C_{DBp} + C_{ext}\right)$$

- Extrinsic capacitance is composed of wire capacitance and input capacitance of fanout
- Input capacitance is composed of overlap capacitance and channel capacitance
  - Overlap capacitance is $C_{GDO} + C_{GSO}$. Miller effect is ignored because V_{out} is assumed to be constant
  - Channel capacitance is $C_{ox}WL$. Assume worst case
- All capacitances are roughly proportional to W
- Equivalent resistance is inversely proportional to W

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Next class

- Delay Analysis
- CMOS Logic Design
- Chapter 6.1 and 6.2

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