Topics

- Performance Characterization
  - Delay Analysis
  - Transistor Sizing
- Digital Design Review
- CMOS Logic Design

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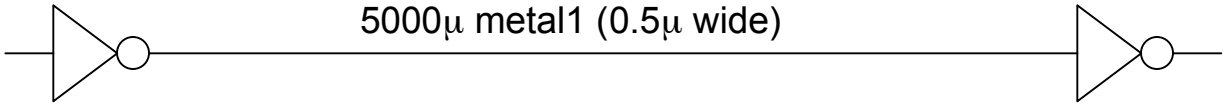
Interconnect Delay



•Interconnect resistance

$$R = .07\frac{5000\mu}{0.5\mu} = 700\Omega$$

•Interconnect capacitance

$$C_{wire} = .03 \cdot 5000\mu \cdot 0.5\mu + .044 \cdot 2 \cdot (5000\mu + 0.5\mu) = 515\,fF$$

•Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

•Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = \frac{700 \cdot 515\,fF}{2} + 700 \cdot 5\,fF = 184\,ps$$

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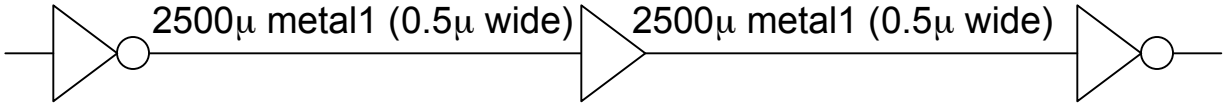
Interconnect Delay

- Avoid long interconnect delays using buffers



•Interconnect resistance

$$R = .07\frac{2500\mu}{0.5\mu} = 350\Omega$$

•Interconnect capacitance

$$C_{wire} = .03 \cdot 2500\mu \cdot 0.5\mu + .044 \cdot 2 \cdot (2500\mu + 0.5\mu) = 258\,fF$$

•Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

•Propagation delay

$$t_p = 2 \cdot \left(\frac{RC_{wire}}{2} + RC_{in}\right) = 2 \cdot \left(\frac{350 \cdot 258\,fF}{2} + 350 \cdot 5\,fF\right) = 94\,ps$$

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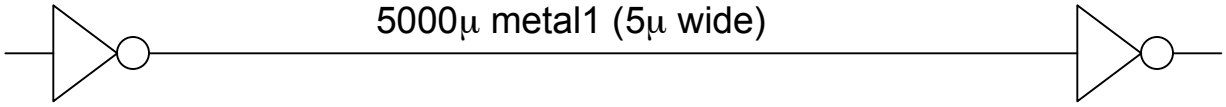
Interconnect Delay

- Avoid long interconnect delays using wider lines



•Interconnect resistance

$$R = .07\frac{5000\mu}{5\mu} = 70\Omega$$

•Interconnect capacitance

$$C_{wire} = .03 \cdot 5000\mu \cdot 5\mu + .044 \cdot 2 \cdot (5000\mu + 5\mu) = 1190\,fF$$

•Intrinsic load capacitance

$$C_{in} \approx 5\,fF$$

•Propagation delay

$$t_p = \frac{RC_{wire}}{2} + RC_{in} = \frac{70 \cdot 1190\,fF}{2} + 70 \cdot 5\,fF = 42\,ps$$

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Delay time analysis

- Propagation delay is proportional to intrinsic resistance and load capacitance

$$t_{pHL} = 0.69 R_{eqn} C_L$$

- Take average of p and n delays for overall propagation delay

$$t_p = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

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Delay time analysis

- Propagation delay is inversely proportional to k

$$t_{pHL} = 0.69\left(\frac{3}{4}\frac{V_{DD}}{I_{DSATn}}\right)C_L$$

$$= 0.52\left(\frac{V_{DD}}{k_n\frac{\left(V_{DD}-V_{Tn}\right)^2}{2}}\right)C_L$$

$$\approx\left(\frac{C_L}{k_n V_{DD}}\right)$$

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Delay time analysis

- Propagation delay is inversely proportional to k
  - When device is velocity saturated

$$t_{pHL} = 0.69\left(\frac{3}{4}\frac{V_{DD}}{I_{DSATn}}\right)C_L$$

$$= 0.52\left(\frac{V_{DD}}{k_n V_{DSATn}\left(V_{DD} - V_{Tn} - \frac{V_{DSATn}}{2}\right)}\right)C_L$$

$$\approx 0.52\left(\frac{C_L}{k_n V_{DSATn}}\right)$$

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Delay time analysis

- Like the fall time and rise times, the delay time is affected by the load capacitance and the transistor k's
- Reduce delay by
  - Reducing C_L
  - Increasing k or increasing W/L ratio
  - Increasing V_{DD} (to a point)

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Delay time analysis

- In order to equalize the rise and fall delays, the transistor equivalent resistances must be equal
- Typically that means the pMOS width must be 2-3 times the width of the nMOS to have equal falling and rising delay times
- However, this does not mean that overall delay has been minimized

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Delay time analysis

- Assume that the inverter is cascaded to another inverter

$$t_p = 0.69 R_{eq}\left(\left(C_{dp1} + C_{dn1}\right) + \left(C_{gp2} + C_{gn2}\right) + C_W\right)$$

- Scale the pmos transistors by a factor of β

$$t_p = 0.69\left(\frac{R_{eqn} + R_{eqp}/\beta}{2}\right)\left(\left(\beta C_{dn1} + C_{dn1}\right) + \left(\beta C_{gn2} + C_{gn2}\right) + C_W\right)$$

$$= 0.345\left(R_{eqn} + \frac{R_{eqp}}{\beta}\right)\left(\left(\beta + 1\right)\left(C_{dn1} + C_{gn2}\right) + C_W\right)$$

- Optimal β

$$\beta = \sqrt{\frac{R_{eqp}}{R_{eqn}}} \approx \sqrt{\frac{k_n V_{DSATn}}{k_p V_{DSATp}}}$$

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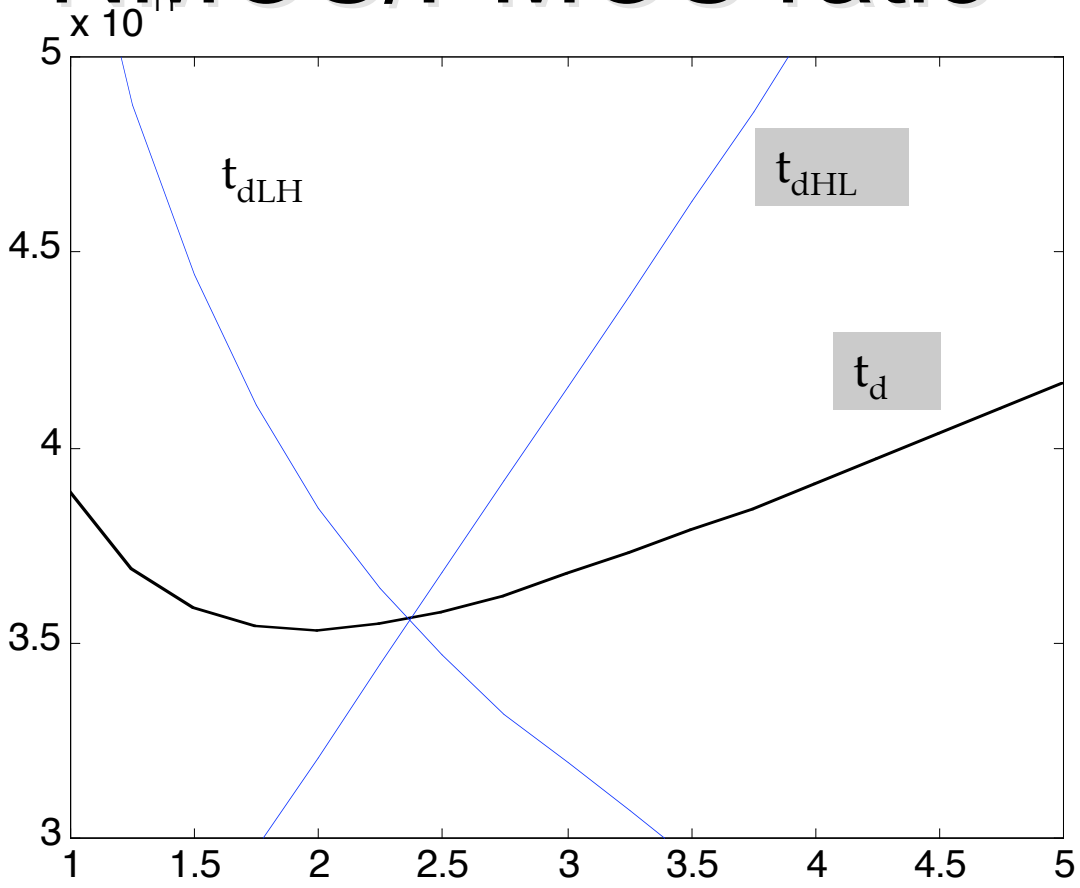
NMOS/PMOS ratio



W_p/W_n

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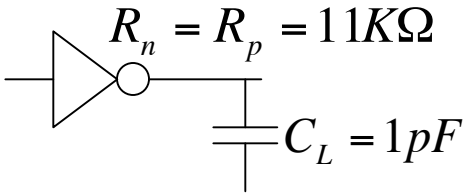
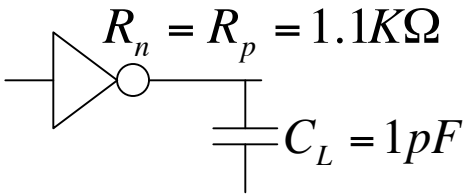
Transistor Sizing

- Size the transistors based on delay requirements and capacitor load



$$t_d = 11ns$$



$$t_d = 1.1ns$$

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Transistor Sizing

- Increasing transistor size allows us to drive large capacitances
- Problems
  - Increases area
  - Increases input capacitance

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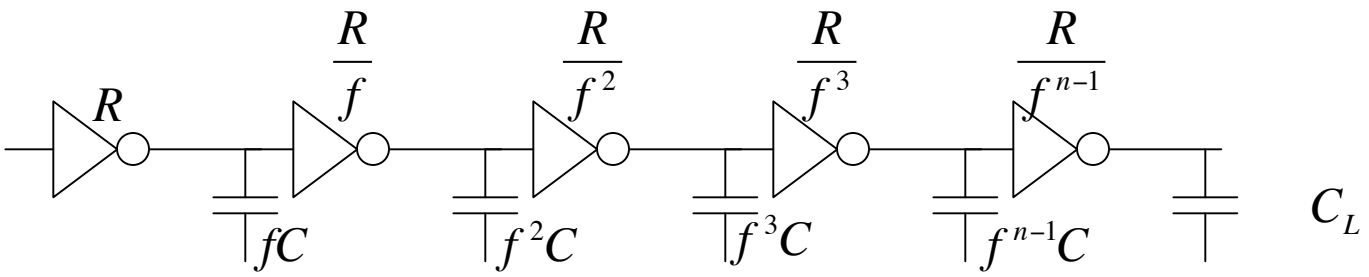
Transistor Sizing

- Use cascaded inverters



$$t_f = (n-1) fRC + \frac{R}{f^{n-1}} C_L$$

•If we equalize the delays, then $f^n = \frac{C_L}{C}$

$$t_p = nfRC$$

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Transistor Sizing

$$t_p = nfRC$$

$$= \frac{\ln\left(\frac{C_L}{C}\right)}{\ln f} fRC$$

- Minimum delay is reached when f is equal to e*(~2.72)*
- At optimum, $n = \ln\left(\frac{C_L}{C}\right)$

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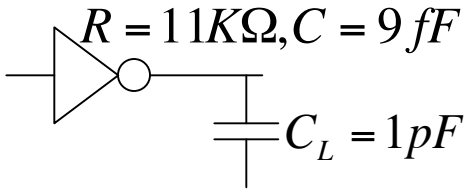
Transistor Sizing



$$n = \ln\left(\frac{C_L}{C}\right) = \ln\left(\frac{1pF}{9fF}\right) = 4.71$$

Set n=5, and f =3 to use integral values

$$t_p = (n-1)fRC + \frac{R}{f^{n-1}}C_L$$

$$= (5-1)\cdot 3 \cdot 11K\Omega \cdot 9fF + \frac{11K\Omega}{3^{5-1}}1pF$$

$$= 1.32ns$$

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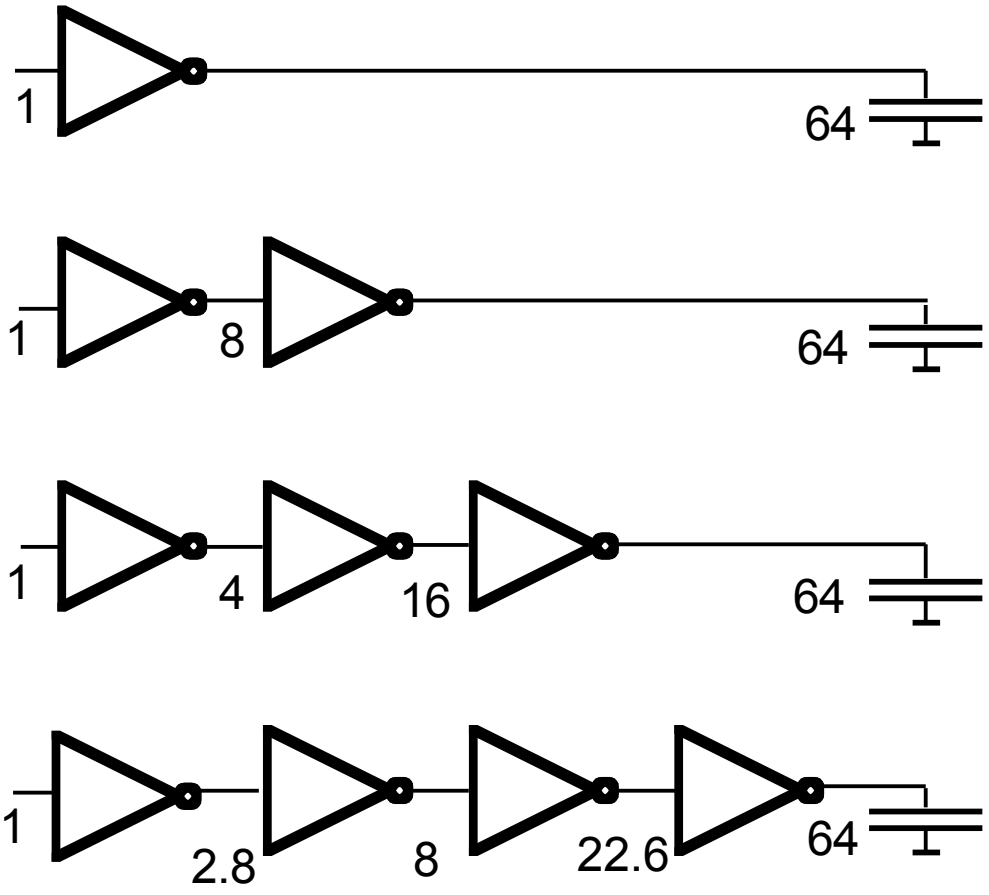
Buffer Design



N	f	t_p
1	**64**	**65**
2	**8**	**18**
3	**4**	**15**
4	**2.8**	**15.3**

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Transistor Sizing

- Cascaded inverter staging will use more area than a single inverter
- The input capacitance is much lower
- The number of stages and stage ratio can be adjusted to get faster delay times or smaller area
- When you take into account intrinsic capacitance, the optimal f is a little closer to 3.6

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Topics

- Digital Design Review
- CMOS Design

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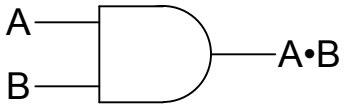
Boolean Algebra

- Basic operators
  - AND

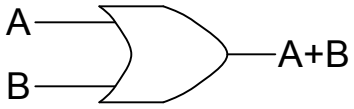
$$f(A,B) = A \cdot B = A \bigcap B$$



A	B	A•B
0	0	0
0	1	0
1	0	0
1	1	1

  - OR

$$f(A,B) = A + B = A \bigcup B$$



A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

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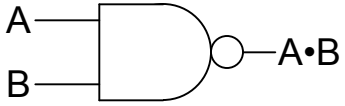
Boolean Algebra

- Basic operators
  - NAND

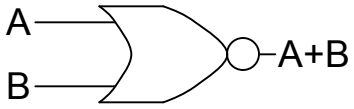
$$f(A,B) = \overline{A \cdot B} = \overline{A \cap B}$$



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

  - NOR

$$f(A,B) = \overline{A + B} = \overline{A \cup B}$$



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

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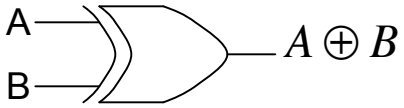
Boolean Algebra

- Basic operators
  - XOR

$$f(A,B) = A \oplus B$$



A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

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Boolean Algebra

- Unity operators

$$A + 0 = A$$

$$A \cdot 1 = A$$

- Complement

$$A + \overline{A} = 1$$

$$A \cdot \overline{A} = 0$$

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Boolean Algebra

- Commutativity

$$A + B = B + A$$

$$A \cdot B = B \cdot A$$

- Associativity

$$A + (B + C) = (A + B) + C$$

$$A \cdot (BC) = (AB) \cdot C$$

- Distributive Law

$$A \cdot (B + C) = AB + AC$$

$$A + BC = (A + B) \cdot (A + C)$$

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Boolean Algebra

- Duality

$$f(A,B,1,0,\cdot,+) = \overline{f(\overline{A},\overline{B},0,1,+,\cdot)}$$

$$A + A = A \qquad A \cdot A = A$$

$$1 + A = 1 \qquad 0 \cdot A = 0$$

$$A + AB = A \qquad A \cdot (A + B) = A$$

$$A + \overline{A}B = A + B \qquad A \cdot (\overline{A} + B) = A \cdot B$$

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Boolean Algebra

- Duality
  - Consensus

$$AB + \overline{A}C + BC = AB + \overline{A}C$$

$$(A + B) \cdot (\overline{A} + C) \cdot (B + C) = (A + B) \cdot (\overline{A} + C)$$

  - DeMorgan's Theorem

$$\overline{A + B} = \overline{A}\,\overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

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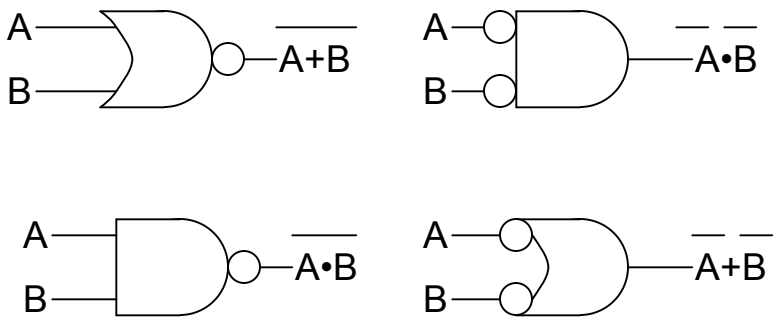
Boolean Algebra

- DeMorgan's Theorem

$$\overline{A + B} = \overline{A}\,\overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$



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Digital Logic

- Truth Tables

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

- Representation of the function to be realized
- Sum of Products representation
  - Sum of minterms

$$F = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + A\overline{B}C + AB\overline{C}$$

- Product of Sums representation
  - Product of maxterms

$$F = \left(A + B + C\right) \cdot \left(A + \overline{B} + \overline{C}\right) \cdot \left(\overline{A} + \overline{B} + \overline{C}\right)$$

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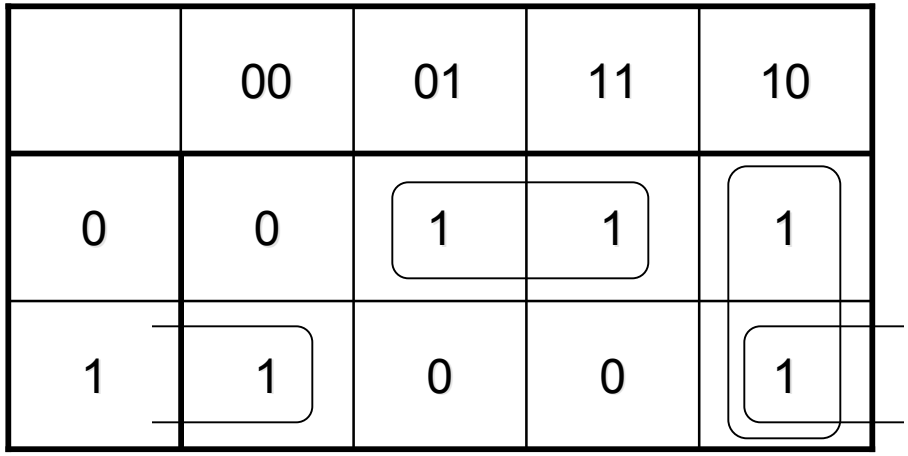
Logic Minimization

- Minimizing SOP representation to MSP
- Using Karnaugh Map

$$F = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + A\overline{B}C + AB\overline{C}$$



$$F = B\overline{C} + A\overline{B} + \overline{B}C$$

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Logic Minimization

- Minimizing POS representation to MPS
- Using Karnaugh Map

$$F = (A + B + C) \cdot (A + \overline{B} + \overline{C}) \cdot (\overline{A} + \overline{B} + \overline{C})$$

	00	01	11	10
0	0	1	1	1
1	1	0	0	1

$$F = (A + B + C) \cdot (\overline{B} + \overline{C})$$

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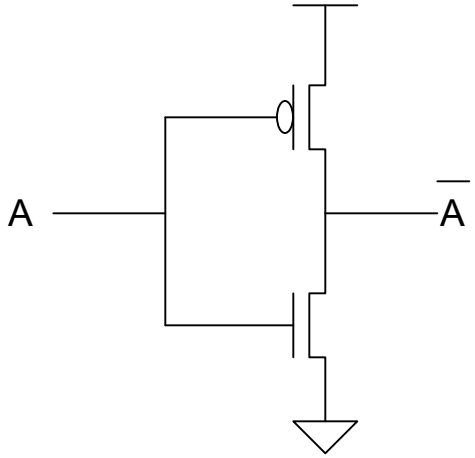
CMOS Logic Implementations

- Inverter



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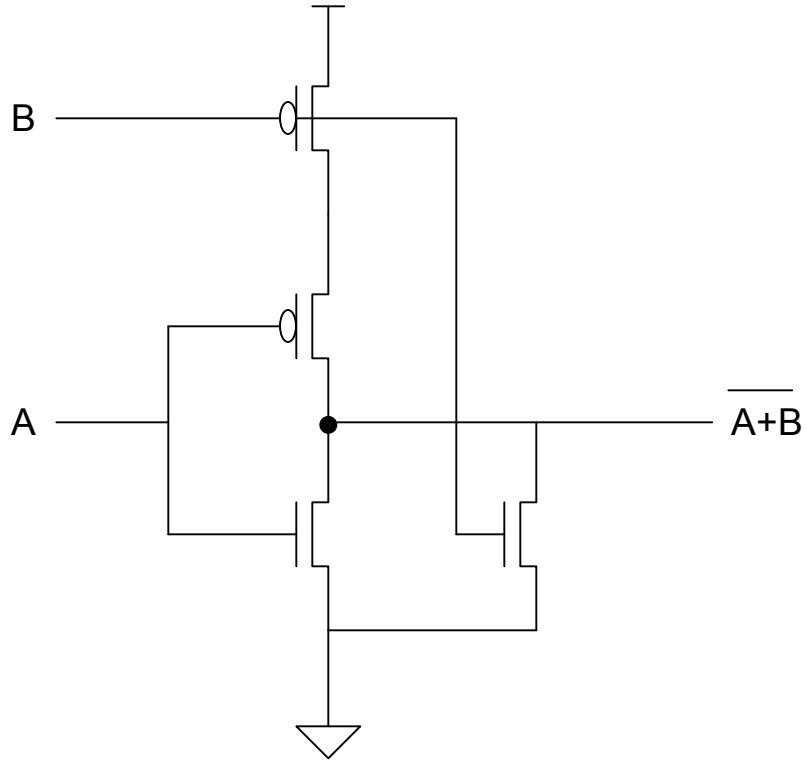
CMOS Logic Implementations

- NOR



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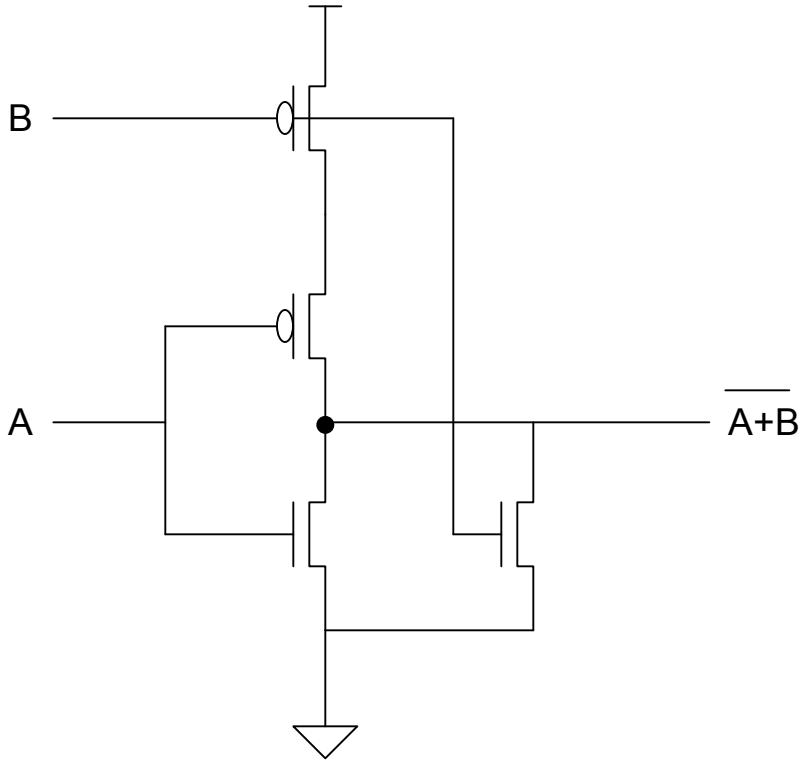
CMOS Logic Implementations

- NOR



Pull-down truth table		
A	B	OUT
0	0	X
0	1	0
1	0	0
1	1	0

Pull-up truth table		
A	B	OUT
0	0	1
0	1	X
1	0	X
1	1	X

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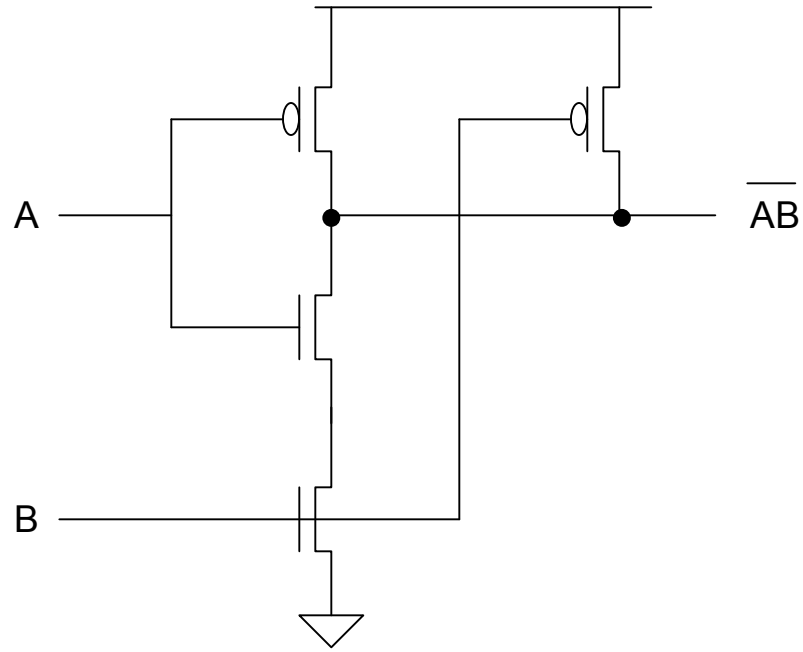
CMOS Logic Implementations

- NAND



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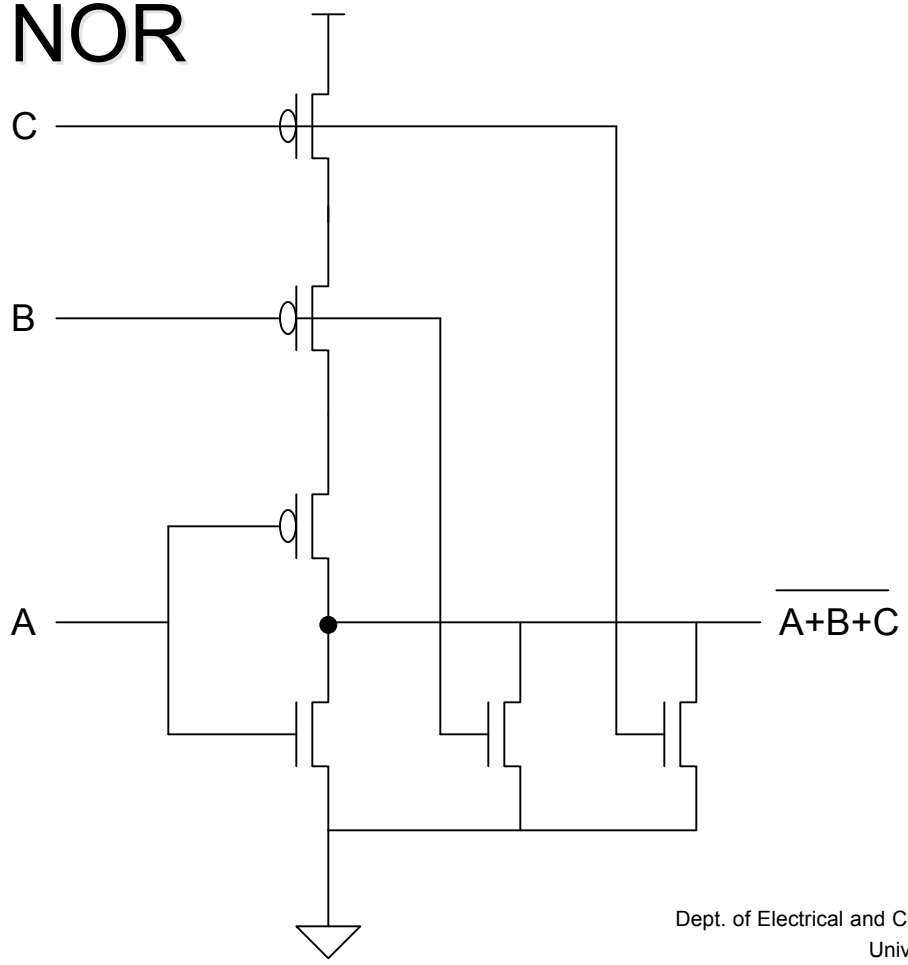
CMOS Logic Implementations

- Multi-input NOR



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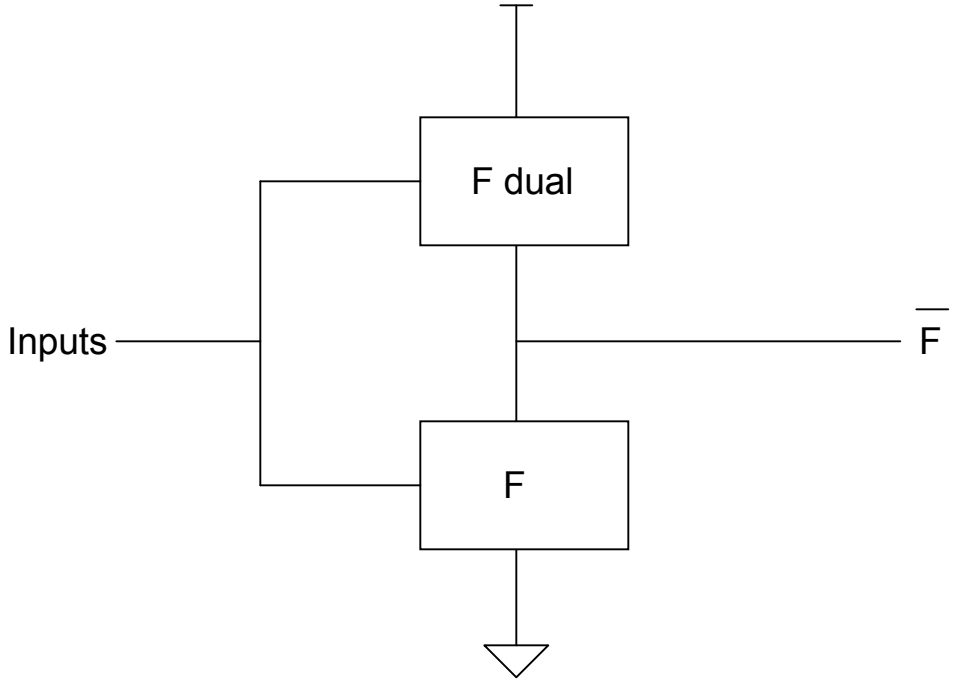
CMOS Logic Implementations

- General CMOS combinational logic



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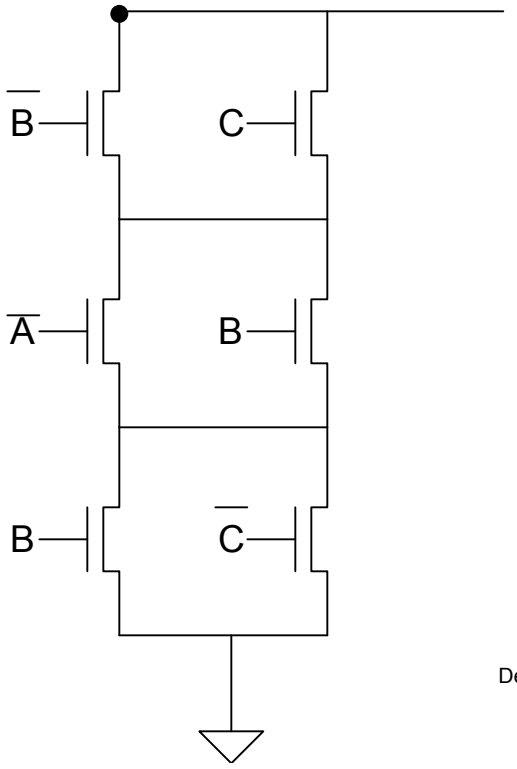
CMOS Logic Implementations

$$F = B\overline{C} + A\overline{B} + \overline{B}C$$

$$= \overline{\left(\overline{B} + C\right) \cdot \left(\overline{A} + B\right) \cdot \left(B + \overline{C}\right)}$$

Pulldown



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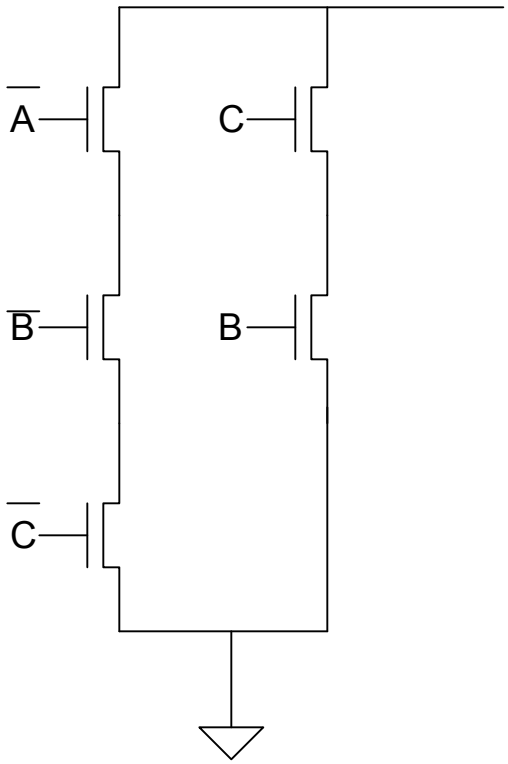
CMOS Logic Implementations

$$F = (A + B + C) \cdot (\overline{B} + \overline{C})$$

$$= \overline{\overline{A}\,\overline{B}\,\overline{C} + BC}$$

Pulldown



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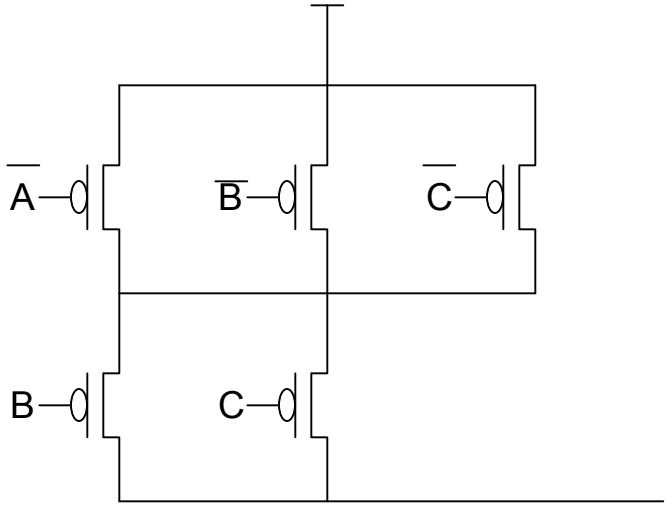
CMOS Logic Implementations

$$F = (A + B + C) \cdot (\overline{B} + \overline{C})$$

$$= \overline{\overline{A}\overline{B}\overline{C} + BC}$$

$$F' = (\overline{A} + \overline{B} + \overline{C}) \cdot (B + C)$$

Pullup



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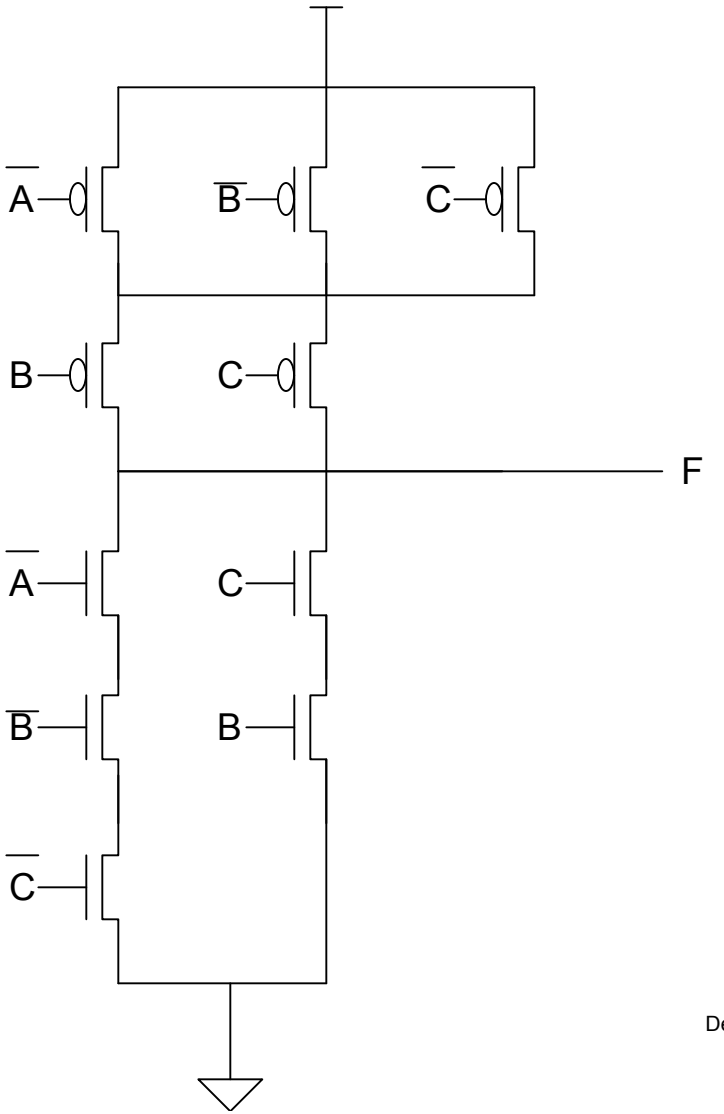
CMOS Logic Implementations



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Next class

- Multi-input delay analysis
- Homework 2 due 2/15
- Chapter 6 and 7

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