Topics

- CMOS Logic Delays
- Logical Effort

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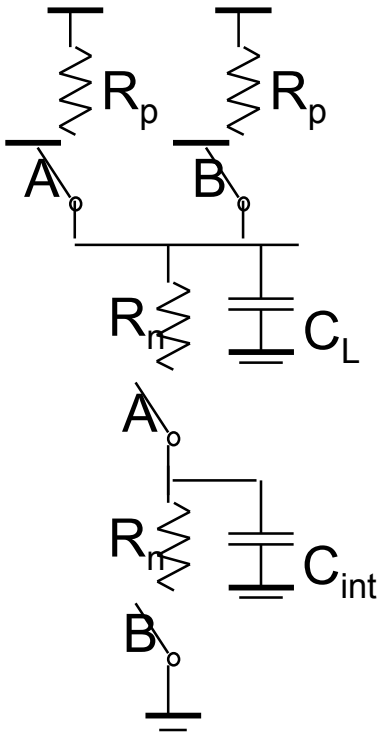
Input Pattern Effects on Delay



- Delay is dependent on the pattern of inputs
- Low to high transition
  - both inputs go low
    - delay is 0.69 $R_p/2$ C_L
  - one input goes low
    - delay is 0.69 R_p C_L
- High to low transition
  - both inputs go high
    - delay is 0.69 $2R_n$ C_L

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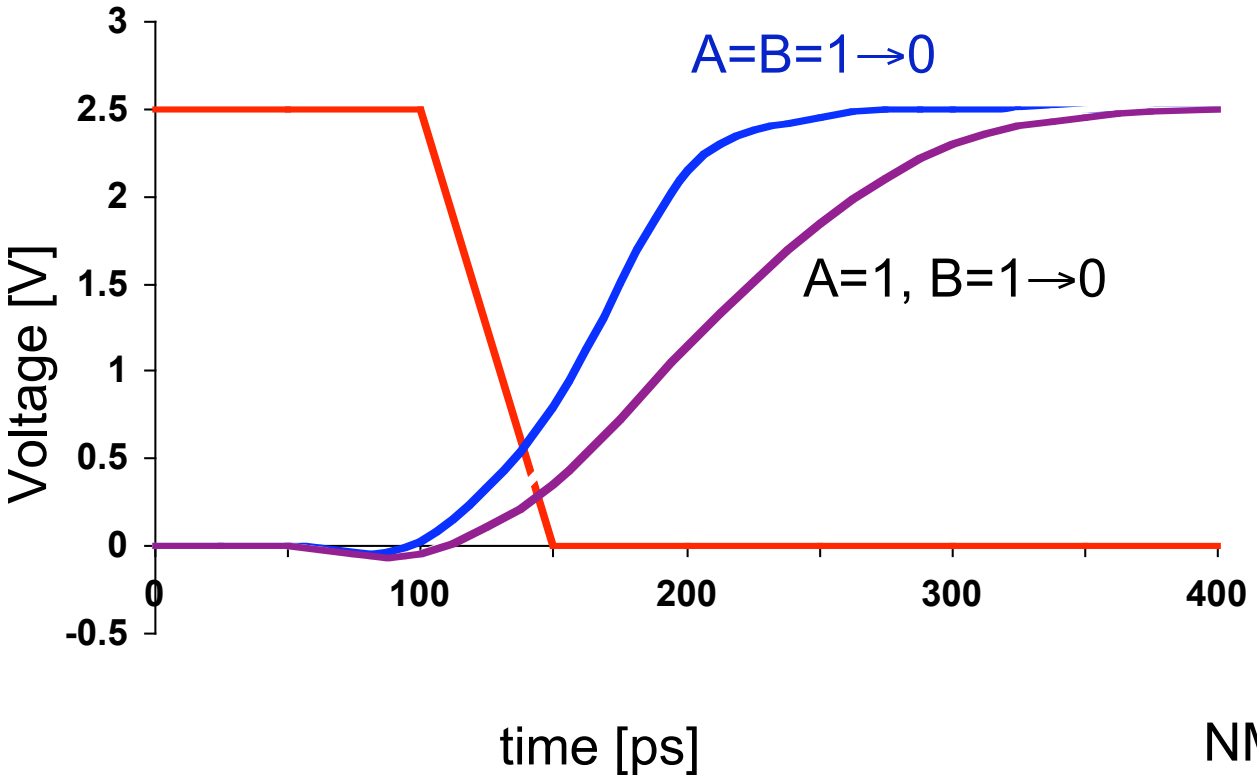
Delay Dependence on Input Patterns



Input Data Pattern	Delay (psec)
00→11	69
10→11	62
01→11	50
11→00	35
11→10	76
11→01	57

NMOS = 0.5μm/0.25 μm
PMOS = 0.75μm/0.25 μm
C_L = 100 fF

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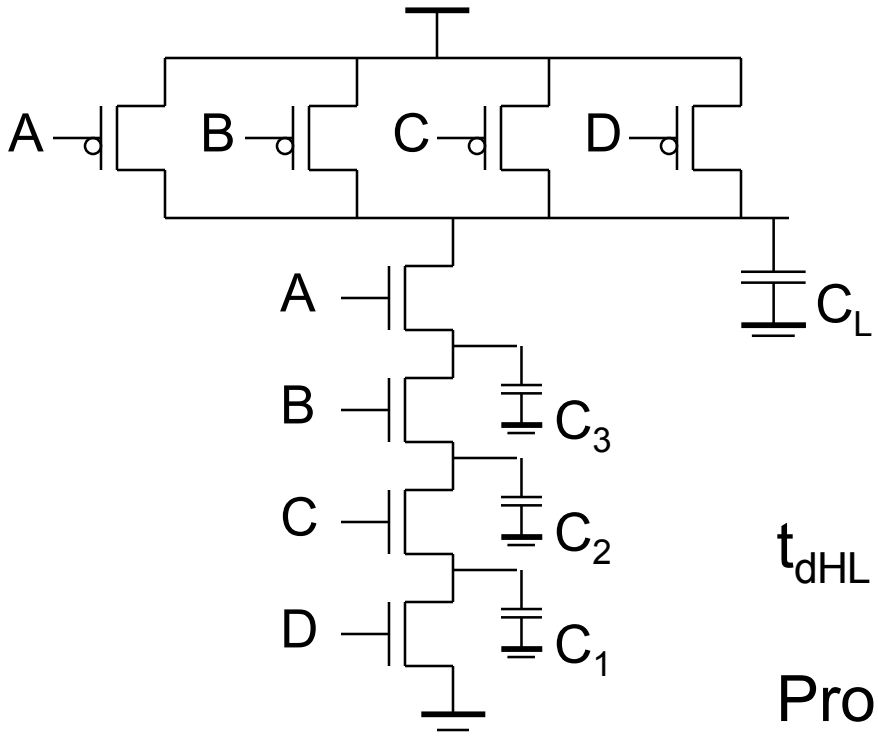
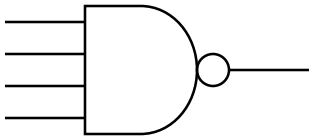
Fan-In Considerations





Distributed RC model
(Elmore delay)

$$t_{dHL} = 0.69\, R_{eqn}(C_1+2C_2+3C_3+4C_L)$$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

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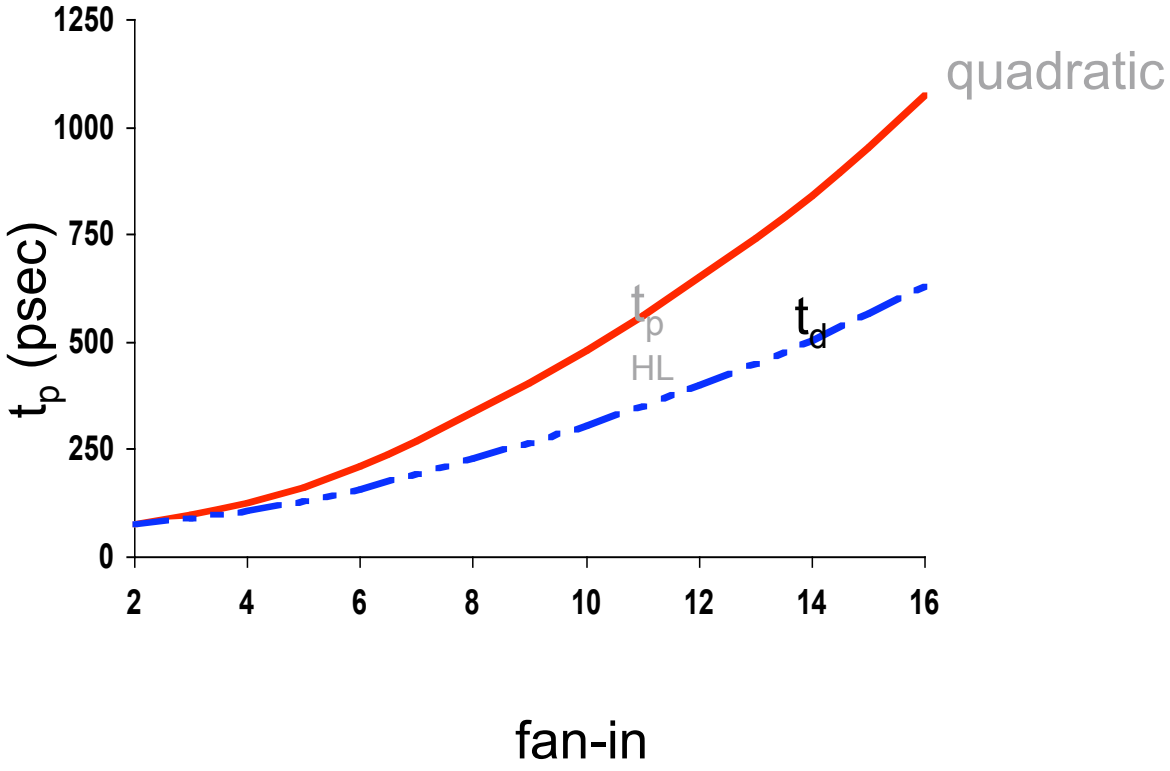
t_p as a Function of Fan-In



Gates with a fan-in greater than 4 should be avoided.

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CMOS Logic Gate Delays

- Using Logical Effort to simplify delay calculation
- Helps in deciding
  - Transistor sizing
  - Number of stages
  - Circuit Topology
- Based on work by Sutherland, Sproull, and Harris (1999)

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Logical Effort

- Characterize process speed with delay parameter t_{p0}
  - $d = d_{abs} / t_{p0}$
  - $t_{p0} \approx 20ps$ for a .25 micron process
- Process independent delay has two components
  - d=p+h
  - h is the effort delay
  - p is the parasitic delay

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Logical Effort

- Effort delay has two components
  - h=g*f
  - g is the logical effort
  - f is the electrical effort or effective fanout
- Parasitic delay is the delay due to intrinsic delay of gate - mostly the drain capacitance
  - Independent of output load and sizing
  - Approximately equal to 1 for an inverter

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Logical Effort

- Logical effort is a measure of the gate's ability to deliver current
  - An inverter has a logical effort of 1
  - Depends only on topology not on process or sizing
- Electrical effort is a measure of fanout
  - C_{out}/C_{in}

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Logical Effort

- Logical Effort assignment
  - Ratio of the gate's input capacitance to the input capacitance of an inverter delivering the same amount of current
  - Can be derived through simulations and accurate measurement
  - Or through estimations based on transistor widths

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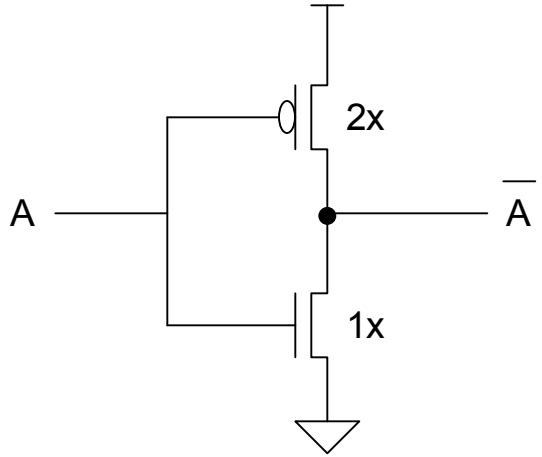
Logical Effort

- Inverter



$$C_{in} = 3$$

$$g = LogicalEffort = 1$$

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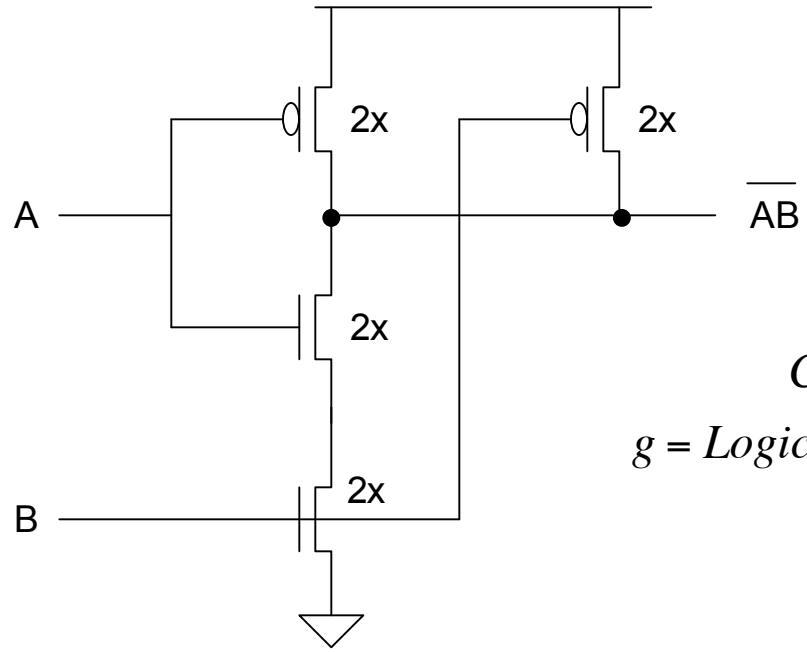
Logical Effort

- NAND



$$C_{in} = 4$$

$$g = LogicalEffort = 4/3$$

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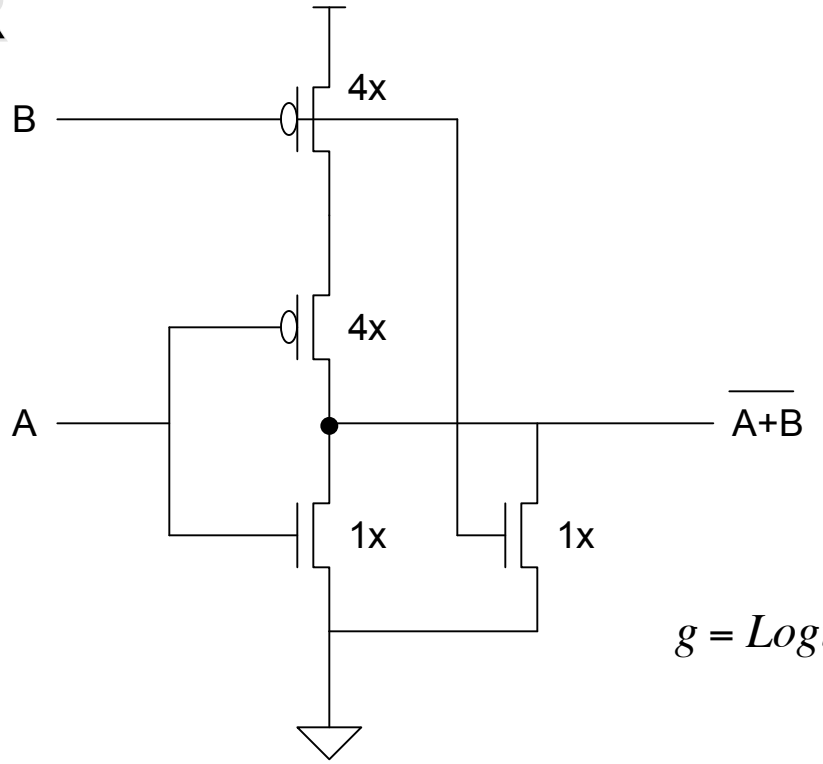
Logical Effort

- NOR



$$C_{in} = 5$$

$$g = LogicalEffort = 5/3$$

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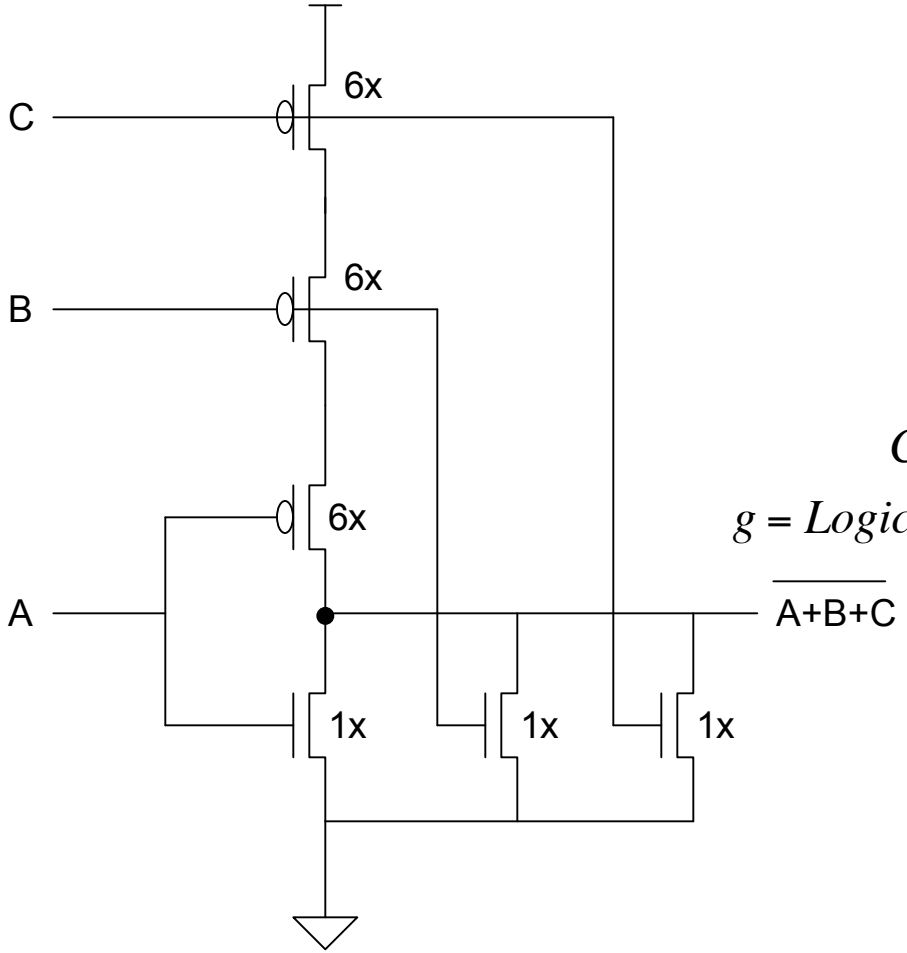
Logical Effort

- NOR



$$C_{in} = 7$$

$$g = LogicalEffort = 7/3$$

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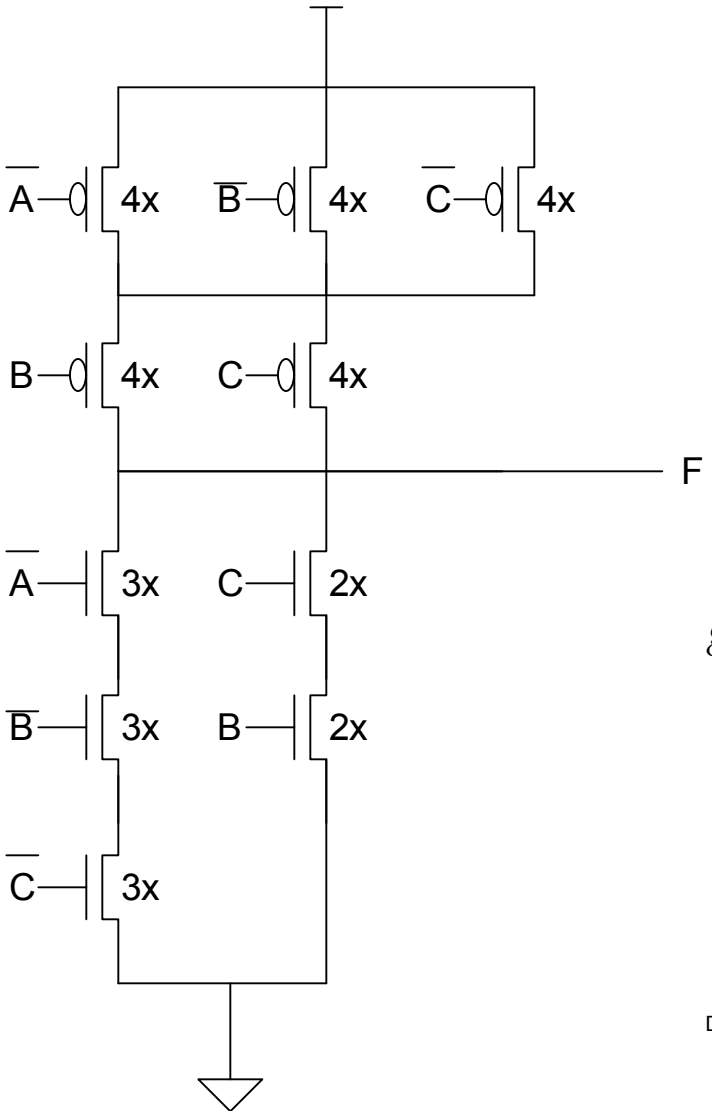
Logical Effort



$$C_{in\,\overline{A}} = 7$$

$$g_{\overline{A}} = LogicalEffort = 7/3$$

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Logical Effort

Number of inputs	1	2	3	n
INV	1			
NAND		4/3	5/3	(n+2)/3
NOR		5/3	7/3	(2n+1)/3

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Logical Effort

- Parasitic delay

Number of inputs	1	2	3	n
INV	p_{inv}			
NAND		$2\ p_{inv}$	$3\ p_{inv}$	$n\ p_{inv}$
NOR		$2\ p_{inv}$	$3\ p_{inv}$	$n\ p_{inv}$

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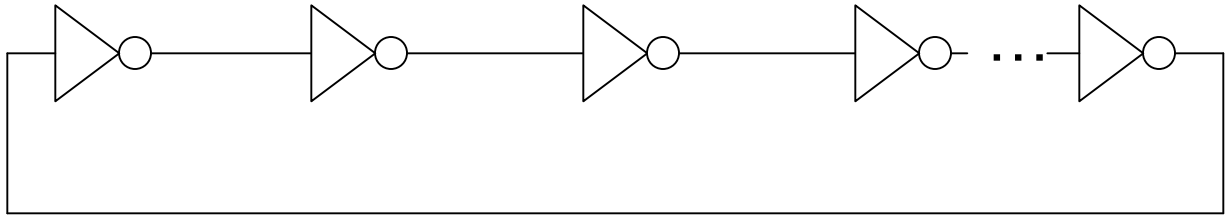
Logical Effort

- Example: Inverter ring oscillator



- Estimate the frequency of the oscillator

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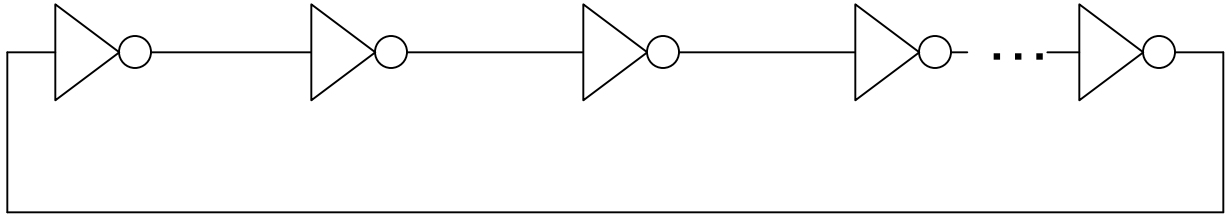
Logical Effort

- Example: Inverter ring oscillator



- $g_i=1$
- $f_i=1$
- $p_i=1$
- $d_i = g_i f_i + p_i = 2$

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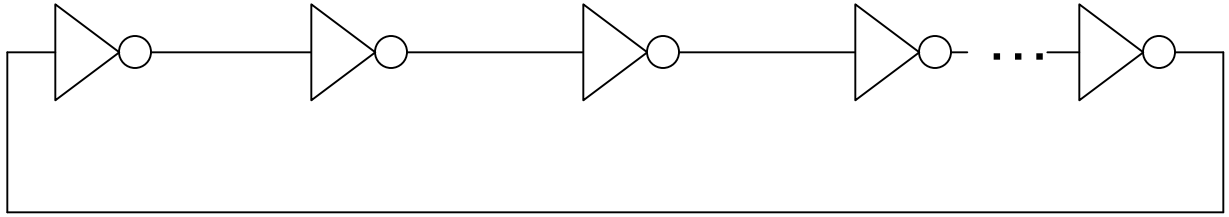
Logical Effort

- Example: Inverter ring oscillator



- Total delay = $N \bullet d_i \bullet t_{p0} = 2N\ t_{p0}$
- Frequency $= 1/(4N\ t_{p0})$

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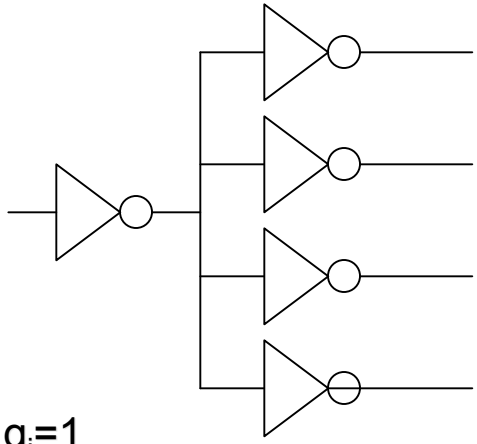
Logical Effort

- Example: FO4 Inverter (Fanout of 4)



- g_i=1
- f_i =4
- p_i =1
- $d_i = g_i f_i + p_i = 5$

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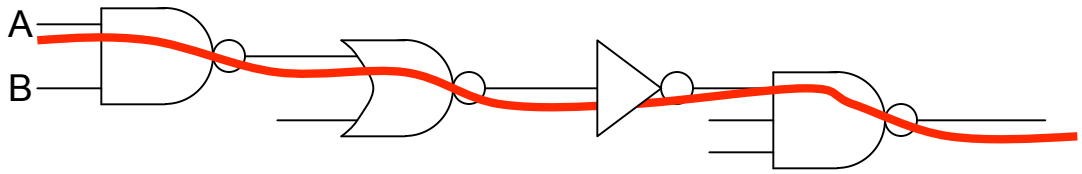
Logical Effort

- Multistage logic networks



- Find path delay

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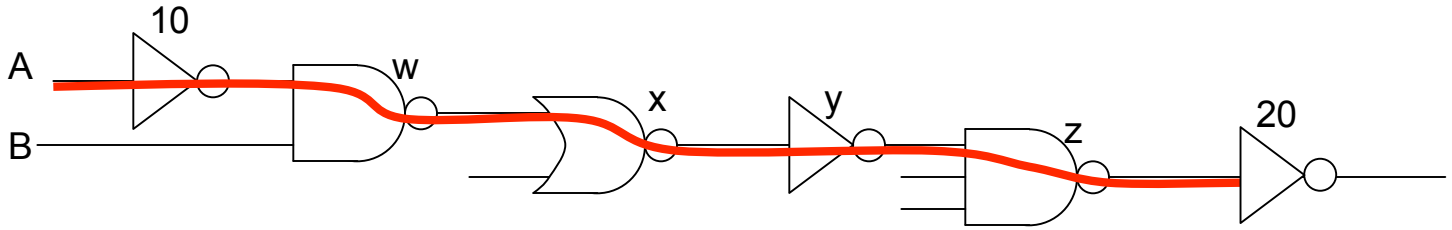
Logical Effort

- Multistage logic networks



g=1	g=4/3	g=5/3	g=1	g=5/3
f=w/10	f=x/w	f=y/x	f=z/y	f=20/z

- Path Parasitic Delay

$$P = \sum p_i$$

- Path Delay

$$D = P + \sum g_i f_i$$

- How do we minimize D? How do we select the sizing?

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Logical Effort

- Path effort is an indirect measure of the path delay
  - Path Electrical Effort $F = \frac{C_{out}}{C_{in}} \neq \prod f_i$
  - Path Logical Effort $G = \prod g_i$
  - Path Effort $H = GF$
- The above does not include any consideration of the effect of fanout within the path
  - H counts only the fanout of the output
  - We need to express the branching behavior along the path

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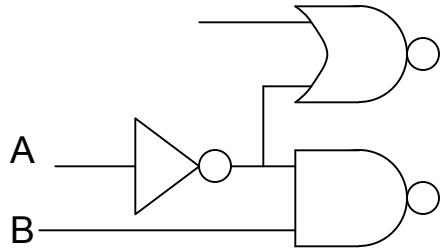
Logical Effort

- Branching Effort



$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}} = \frac{C_{total}}{C_{useful}}$$

$$B = \prod b_i$$

$$FB = \frac{C_{out}}{C_{in}} \prod b_i = \prod f_i$$

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Logical Effort

- Path Effort

$$H = GFB = \prod g_i \prod f_i = \prod g_i f_i$$

- Path Delay

$$D = P + \sum g_i f_i$$

- Minimized when each stage delay is equal

$$g_i f_i = \hat{h} = \sqrt[N]{H}$$

$$D = P + N\hat{h}$$

$$= P + N\sqrt[N]{H}$$

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Logical Effort

- Work backwards to assign sizing

$$g_i f_i = \sqrt[N]{H}$$

$$f_i = \frac{\sqrt[N]{H}}{g_i}$$

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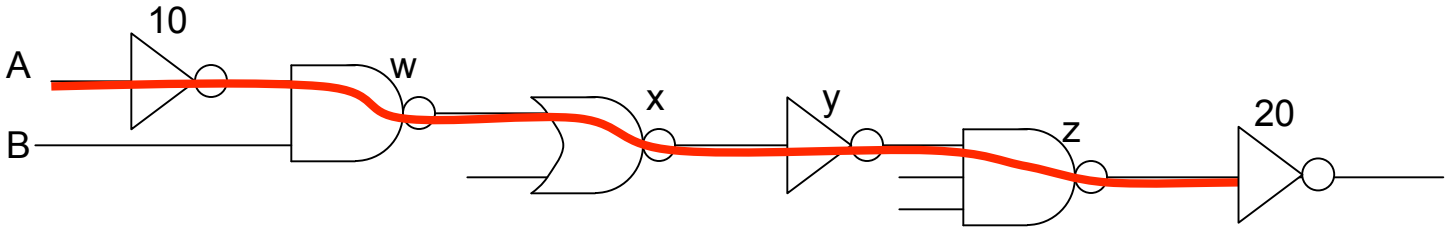
Logical Effort

- Example



g=1	g=4/3	g=5/3	g=1	g=5/3
f=w/10	f=x/w	f=y/x	f=z/y	f=20/z

$$G = \prod g_i = 1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot 1 \cdot \frac{5}{3} = \frac{100}{27}$$

$$F = \frac{C_{out}}{C_{in}} = \frac{20}{10} = 2$$

$$B = 1$$

$$H = GFB = \frac{100}{27} \cdot 2 \cdot 1 = \frac{200}{27}$$

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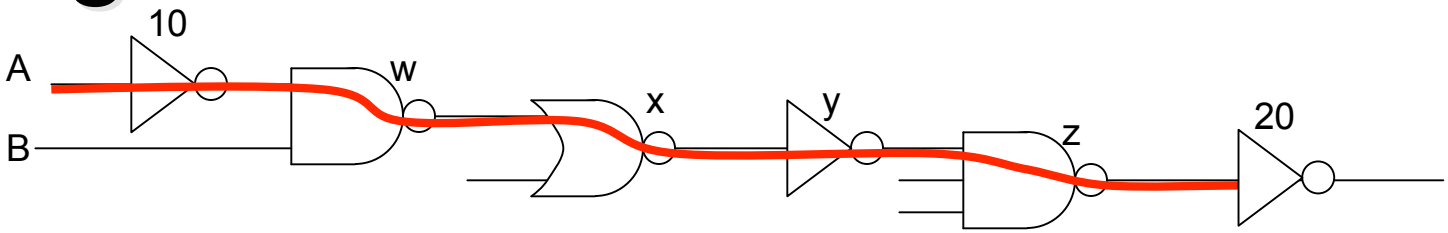
Logical Effort



g=1	g=4/3	g=5/3	g=1	g=5/3
f=w/10	f=x/w	f=y/x	f=z/y	f=20/z

$$\hat{h} = \sqrt[N]{H} = \sqrt[5]{\frac{200}{27}} = 1.49$$

$$\hat{h} = g_5 f_5 = \frac{5}{3} \cdot \frac{20}{z} = 1.49 \Rightarrow z = 22.3$$

$$\hat{h} = g_4 f_4 = 1 \cdot \frac{z}{y} = 1.49 \Rightarrow y = 15.0$$

$$\hat{h} = g_3 f_3 = \frac{5}{3} \cdot \frac{y}{x} = 1.49 \Rightarrow x = 16.8$$

$$\hat{h} = g_2 f_2 = \frac{4}{3} \cdot \frac{x}{w} = 1.49 \Rightarrow w = 15.0$$

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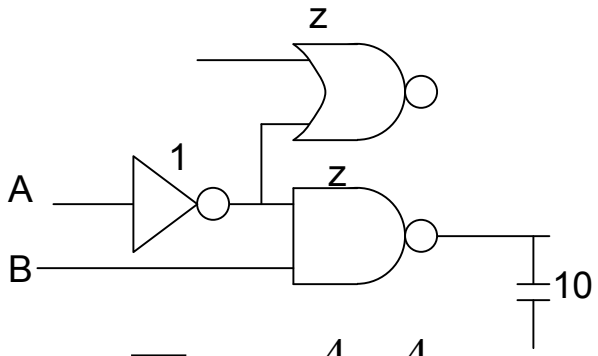
Logical Effort

- Example



$$G = \prod g_i = 1 \cdot \frac{4}{3} = \frac{4}{3}$$

$$F = \frac{C_{out}}{C_{in}} = \frac{10}{1} = 10$$

$$B = \frac{C_{total}}{C_{onpath}} = \frac{2z}{z} = 2$$

$$H = GFB = \frac{4}{3} \cdot 10 \cdot 2 = \frac{80}{3}$$

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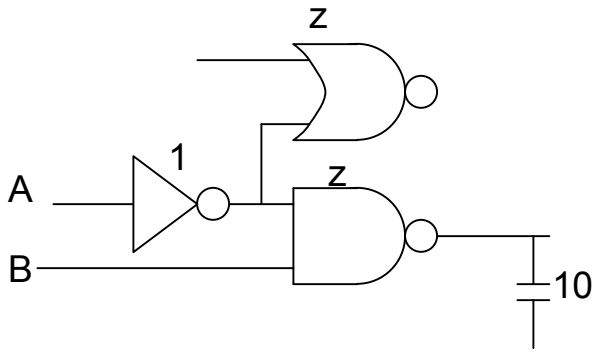
Logical Effort

- Example



$$\hat{h} = \sqrt[N]{H} = \sqrt{\frac{80}{3}} = 5.16$$

$$\hat{h} = g_2 f_2 = \frac{4}{3} \cdot \frac{10}{z} = 5.16 \Rightarrow z = 2.58$$

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Next class

- Layout
- Read Chapter 2.3 and Insert A
- No office hours tomorrow
- Homework 3 on website due 2/22

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