Topics

- Layout Styles
- Layout Strategies

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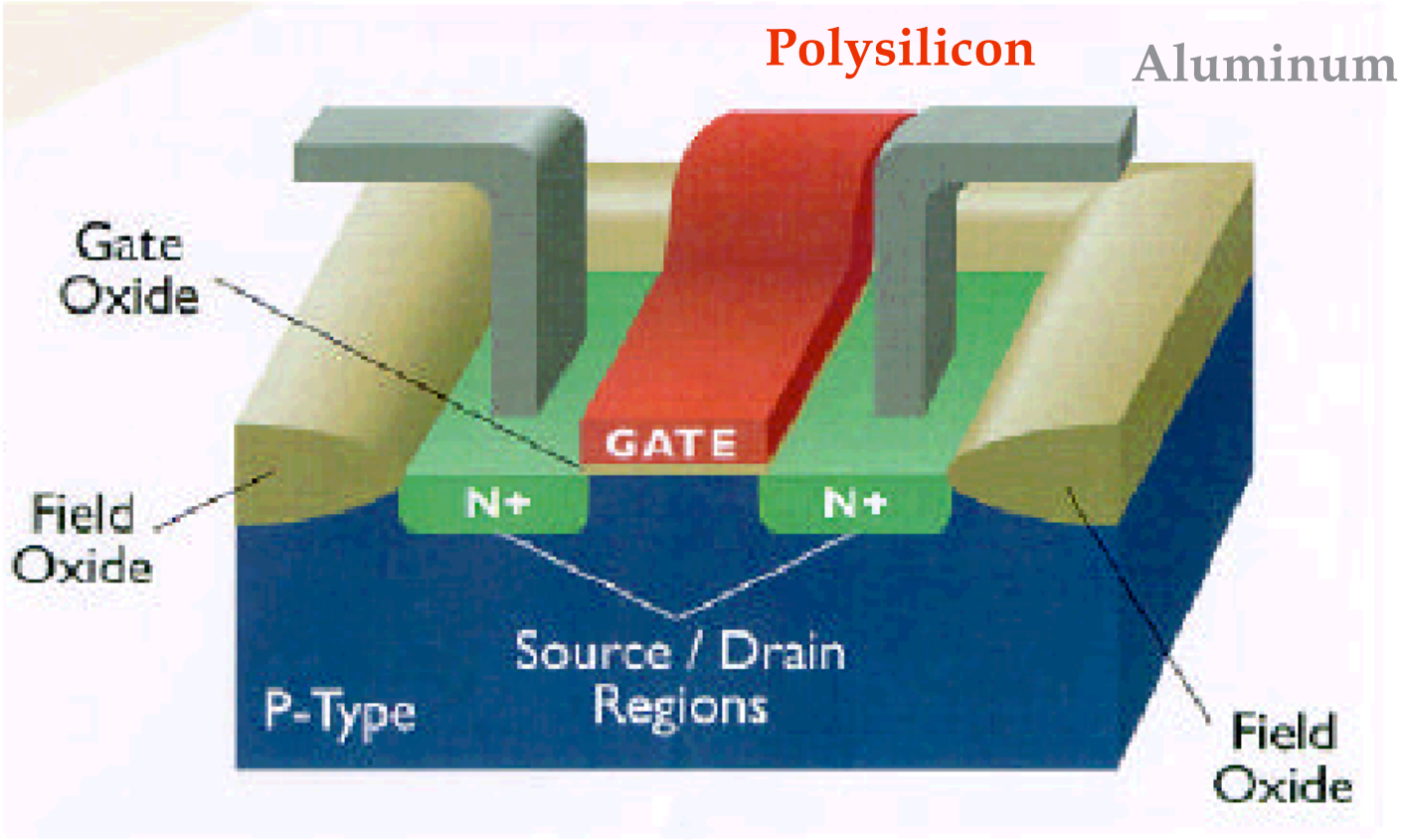
3D Perspective



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Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

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CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

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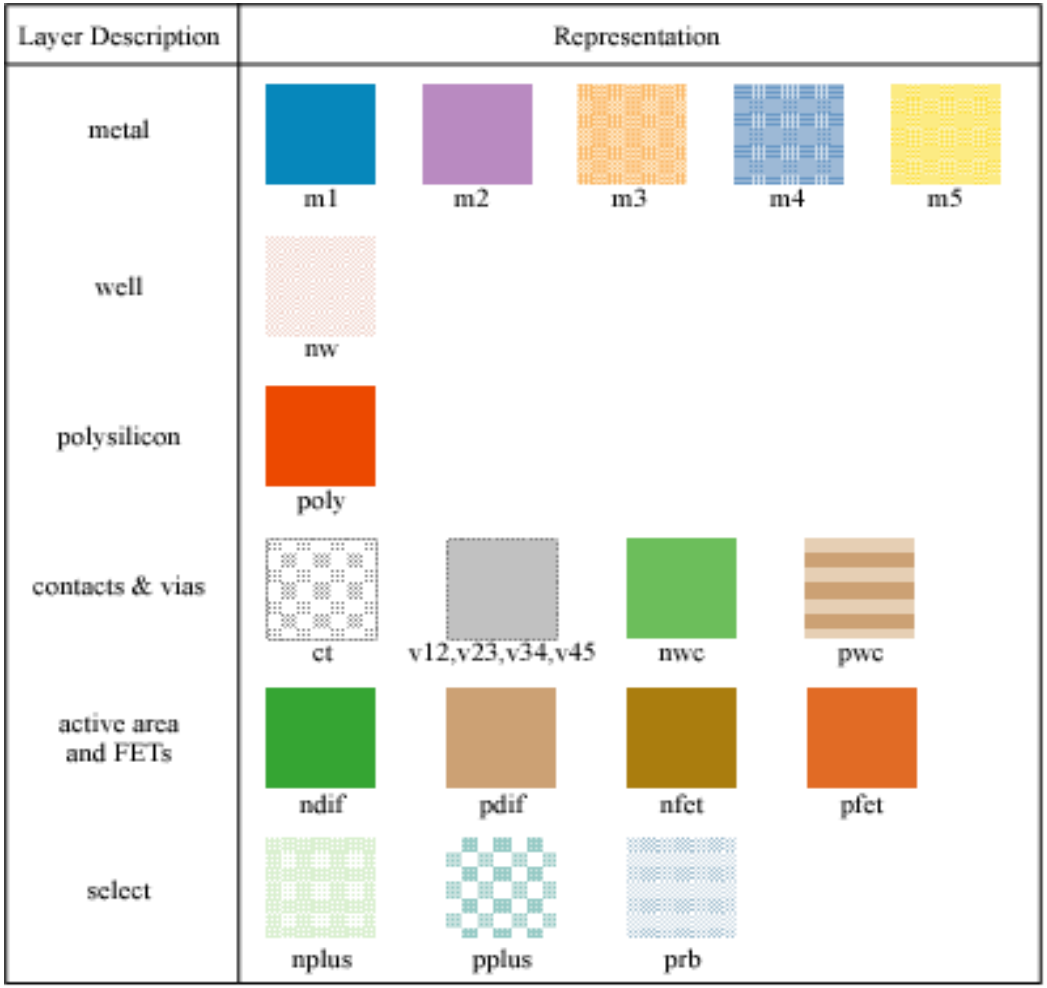
Layers in 0.25 μm CMOS process



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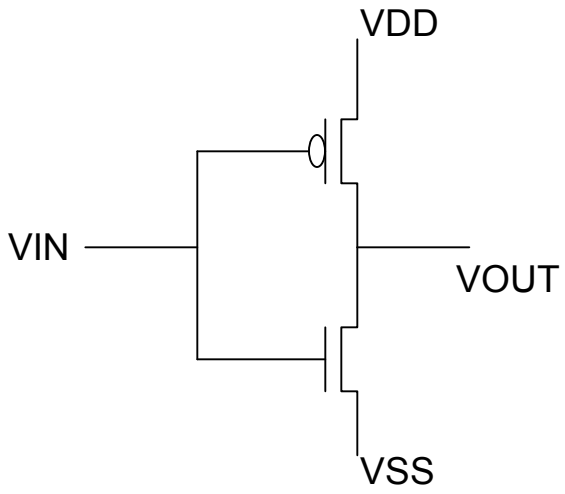
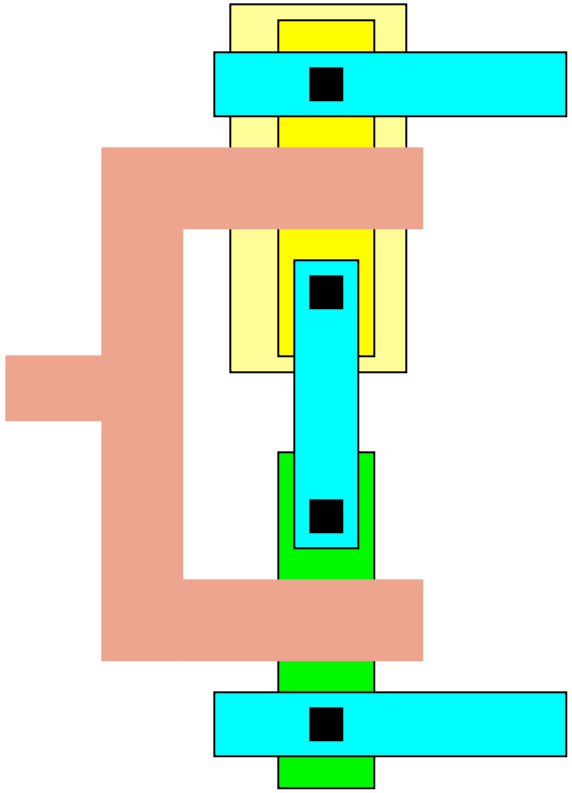
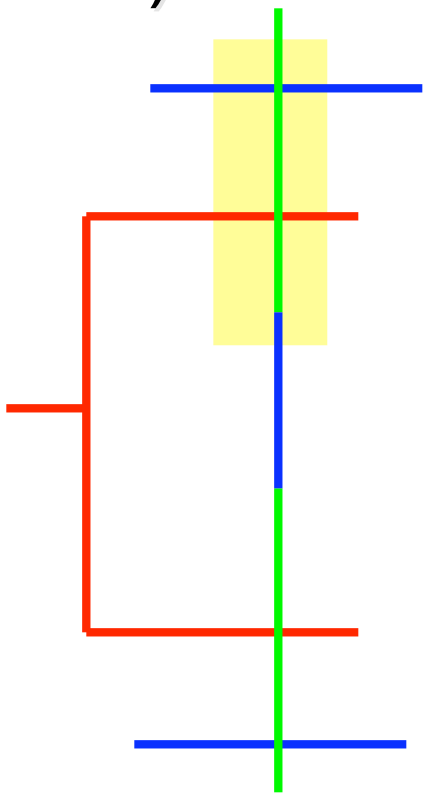
Layout Styles

- Horizontal flow (vertical transistors)

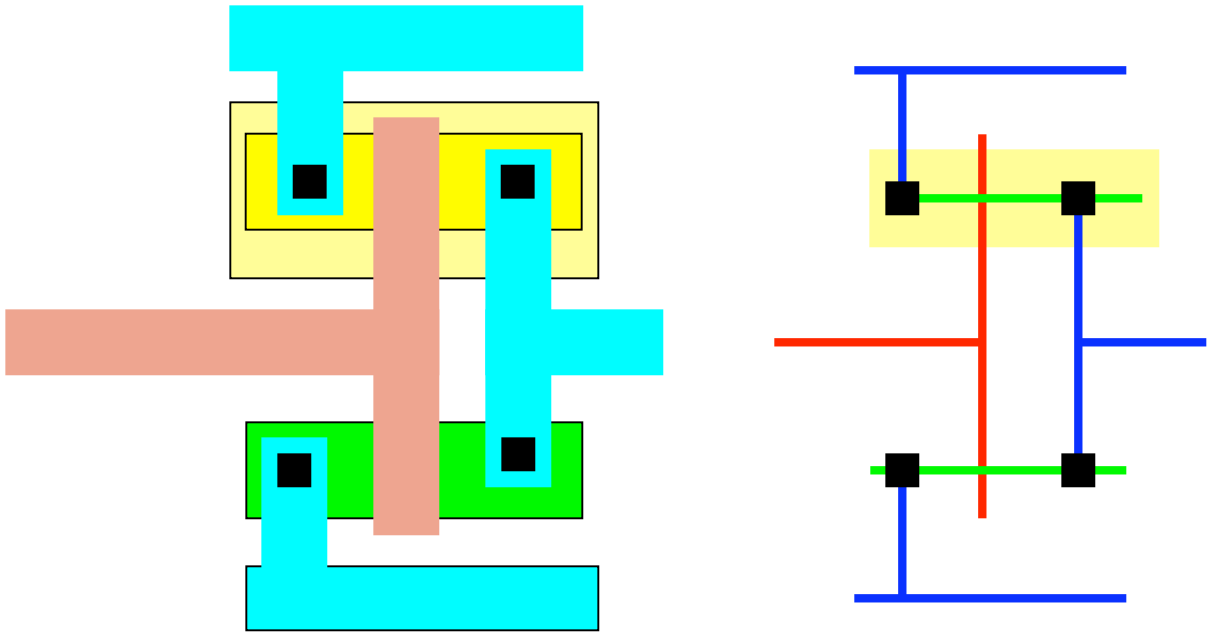






Layout Styles

- Horizontal flow (horizontal transistors)



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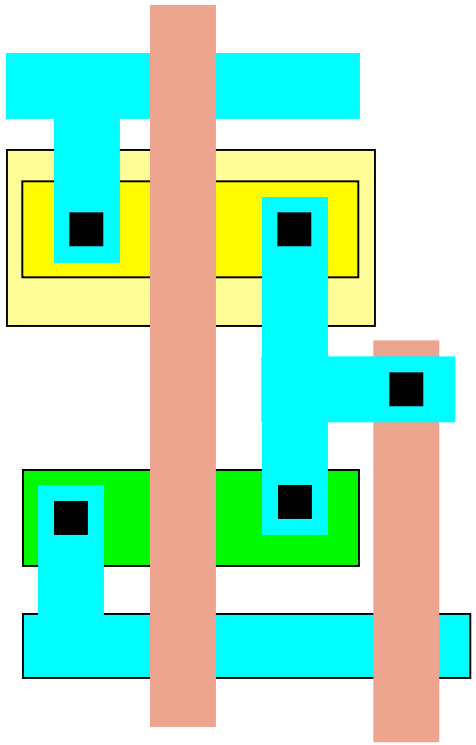
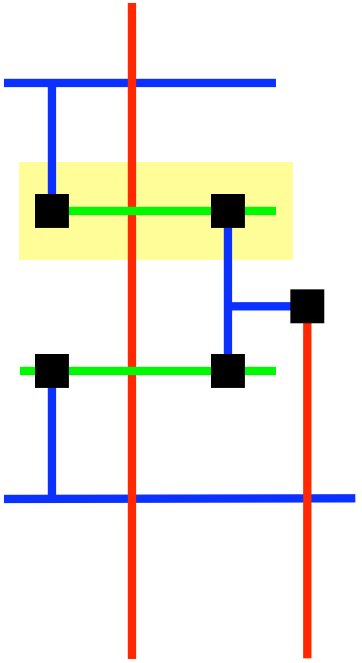
Layout Styles

- Vertical flow (horizontal transistors)
- Standard cell design





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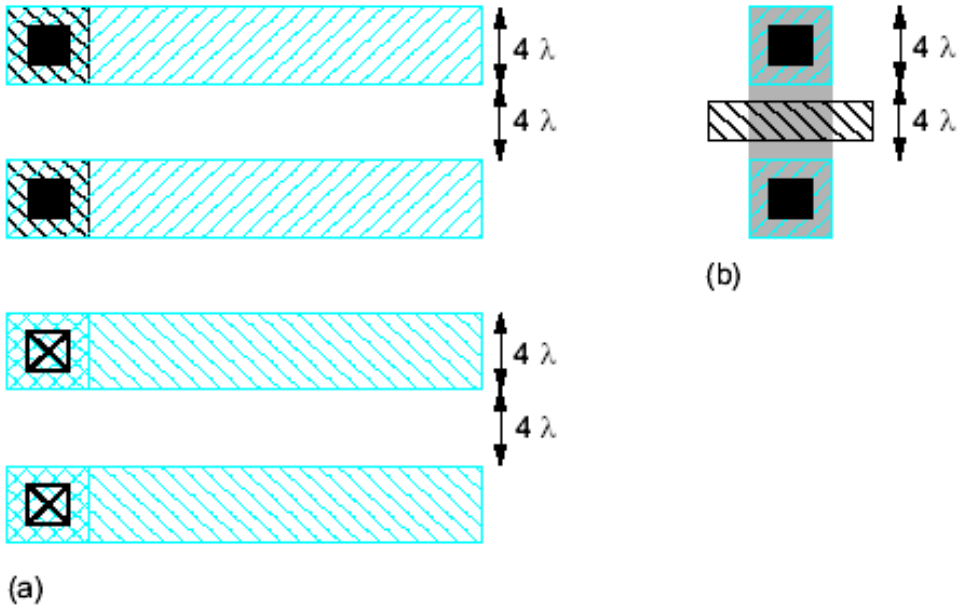
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



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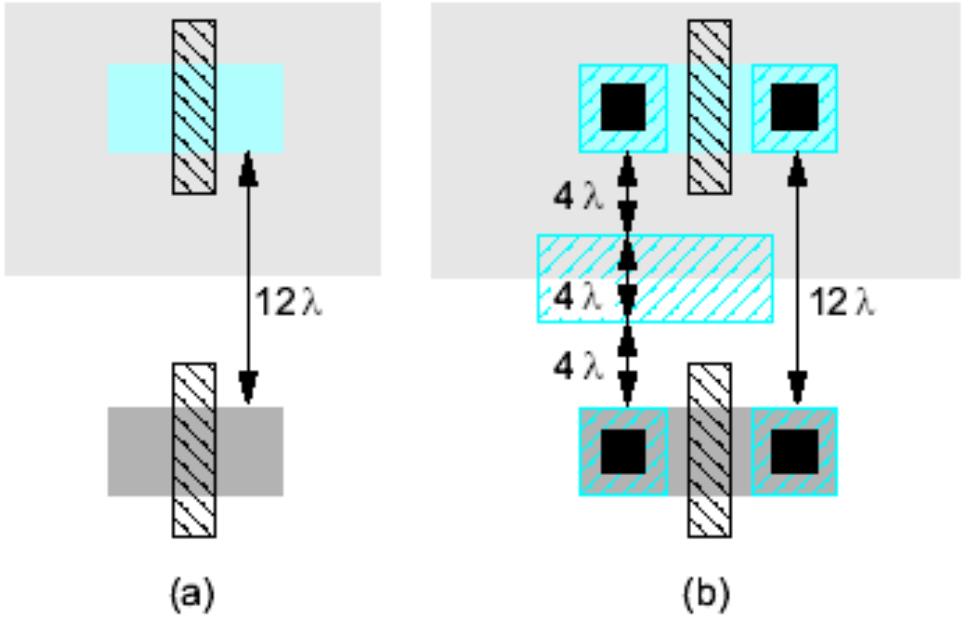
Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



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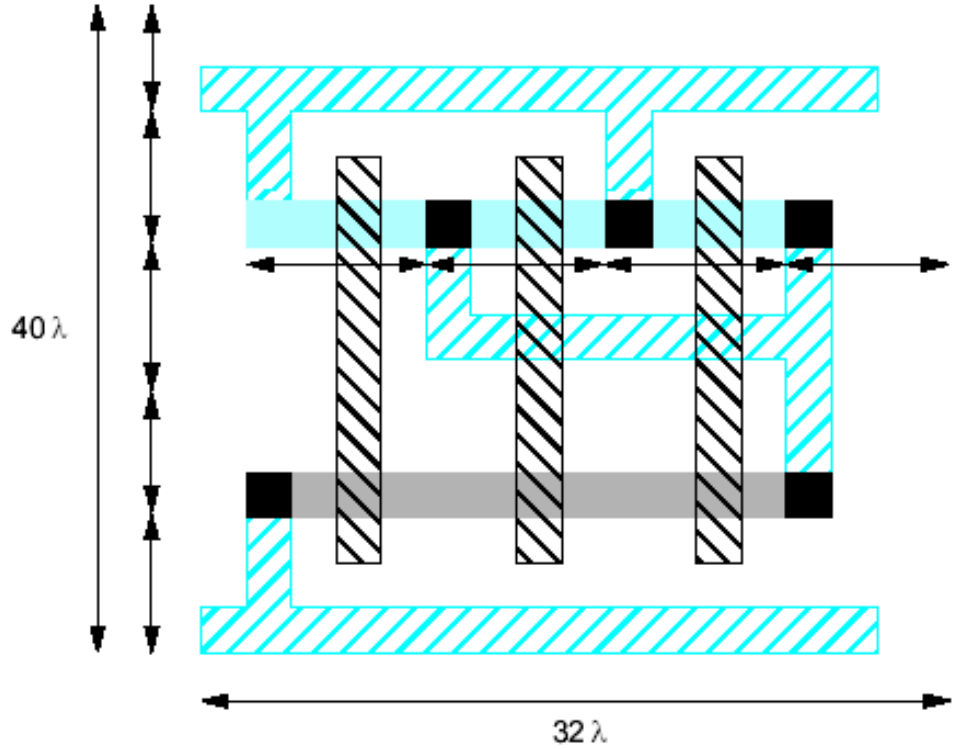
Area Estimation

- Estimate area by counting wiring tracks
  -



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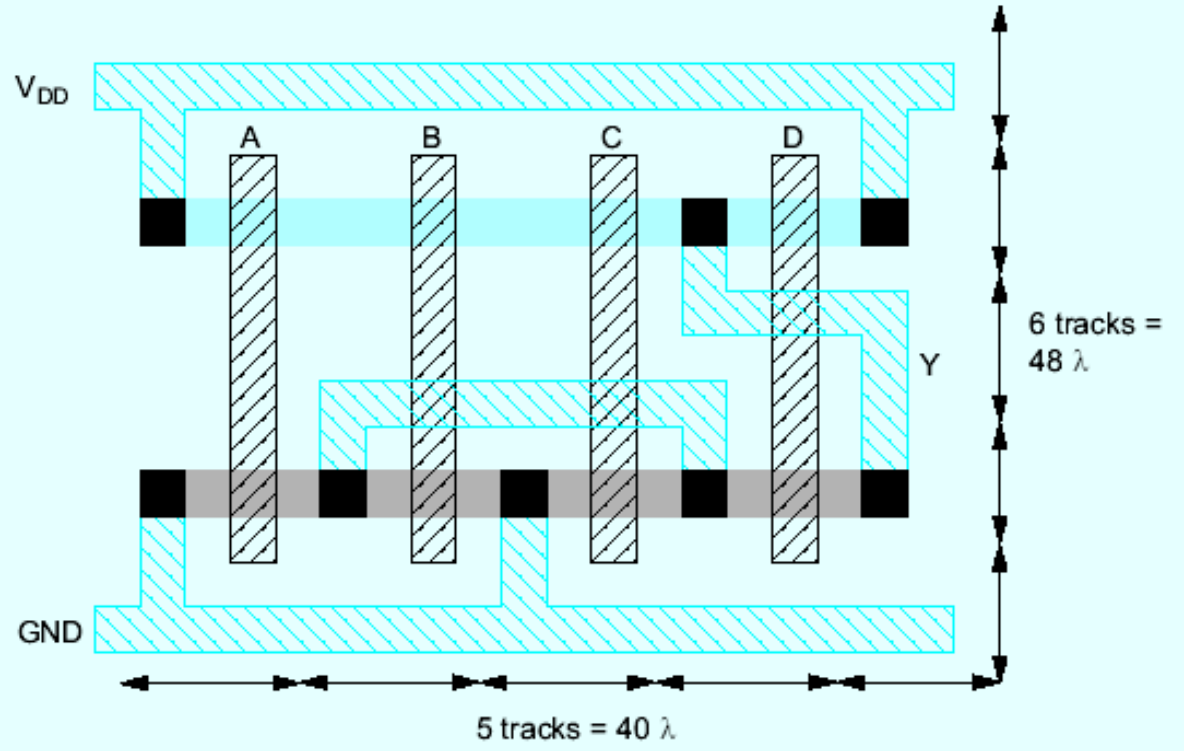
Example: O3AI



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Layout strategies

- How do you decide on a layout?
  - Area constraints
  - Requirements of inputs and outputs
  - Metal layer interconnect
  - Difficult for multi-input gates
    - How do you decide on order of inputs?

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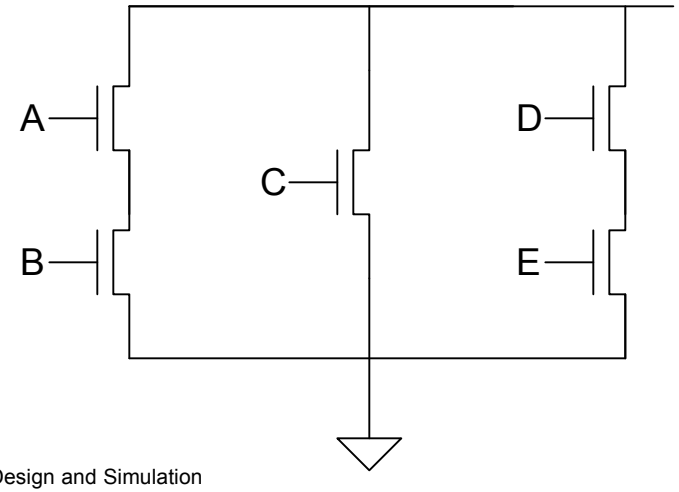
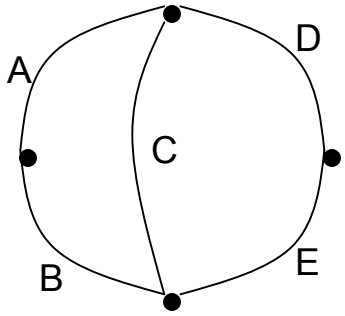
Layout strategies

- Euler path method
- Convert schematic into a graph
- Eg. $F=\overline{AB+C+DE}$





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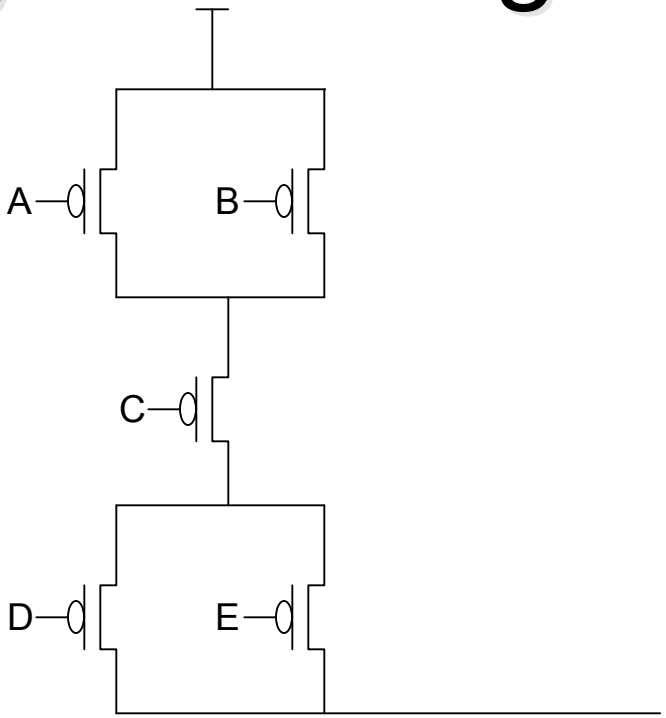
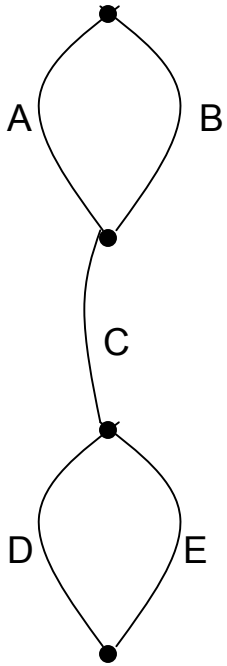
Layout strategies





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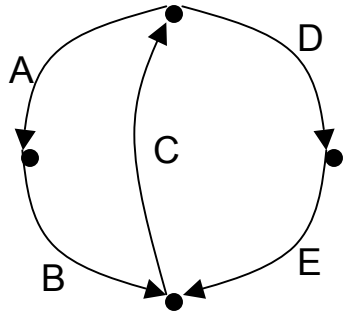
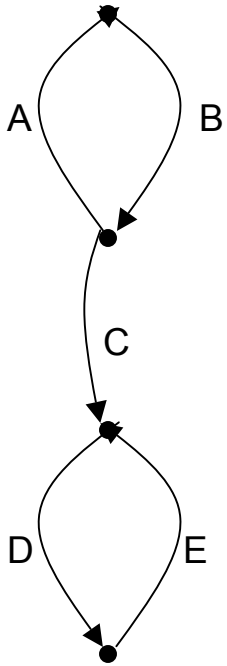
Layout strategies

•Find common path in both graphs (Euler path)





•A to B to C to D to E

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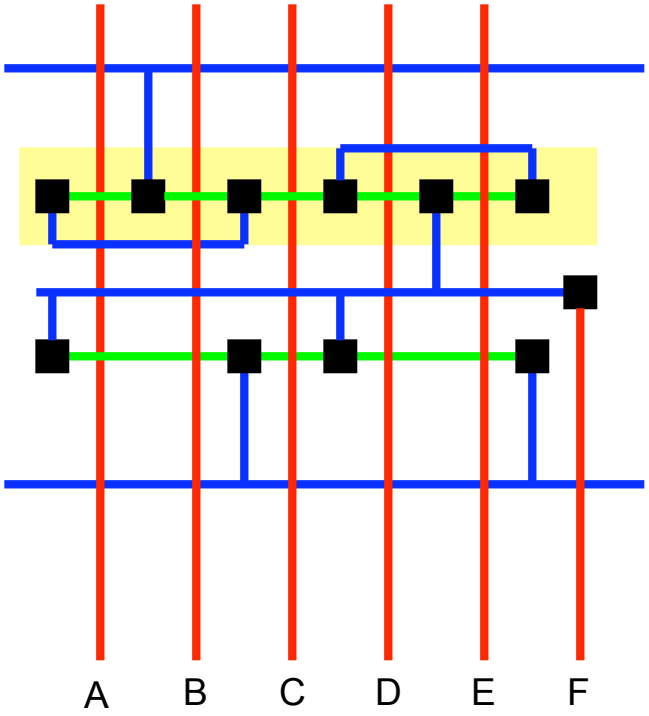
Layout strategies



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Layout strategies

- Euler path method
  - Not always guaranteed to find a Euler path
  - For example, if the function was $F=\overline{C+AB+DE}$
  - If no Euler path found, you will need to break the gate, or rearrange the inputs

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Layout strategies

- How do you decide on a layout?
  - Area constraints
  - Requirements of inputs and outputs
  - Metal layer interconnect
  - Performance considerations

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Layout strategies

- Very wide transistors
  - Multiple contacts to reduce diffusion resistance
  - Folding to reduce diffusion capacitance

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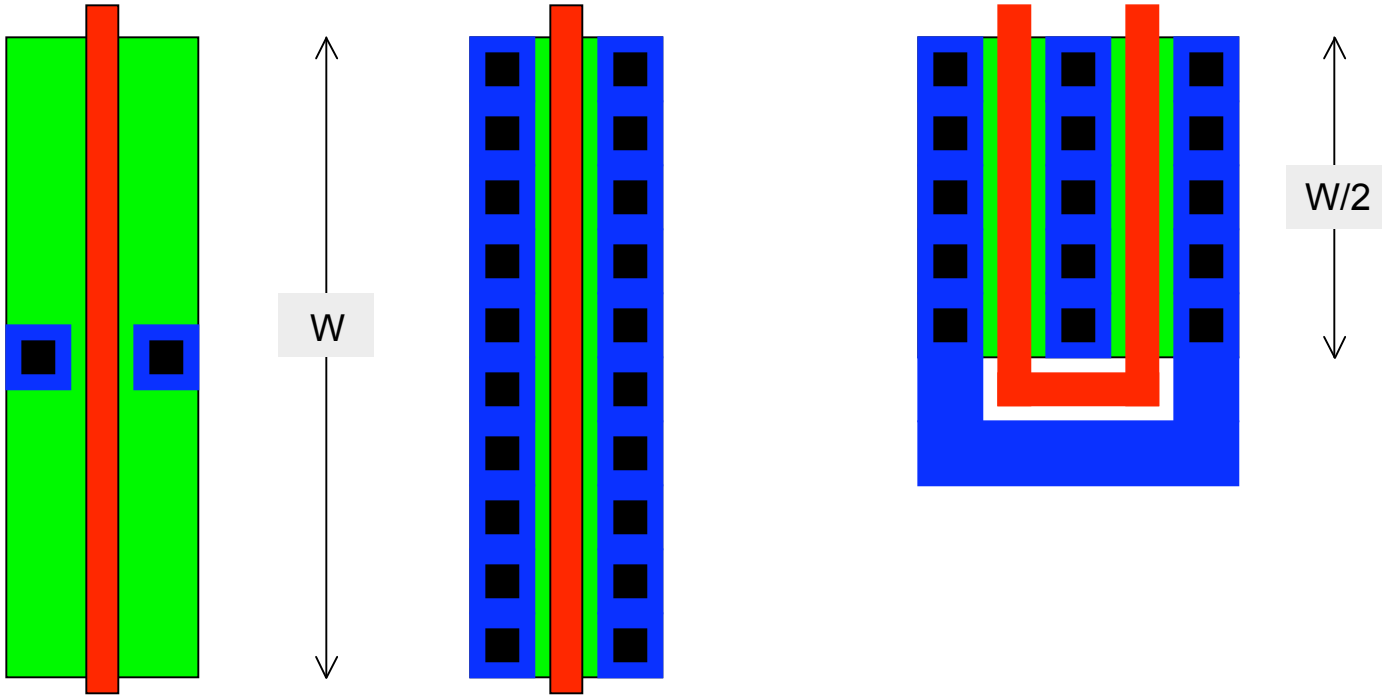
Layout strategies



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Layout strategies

- Performance implications
  - Number of transistors at output
  - Order of transistors

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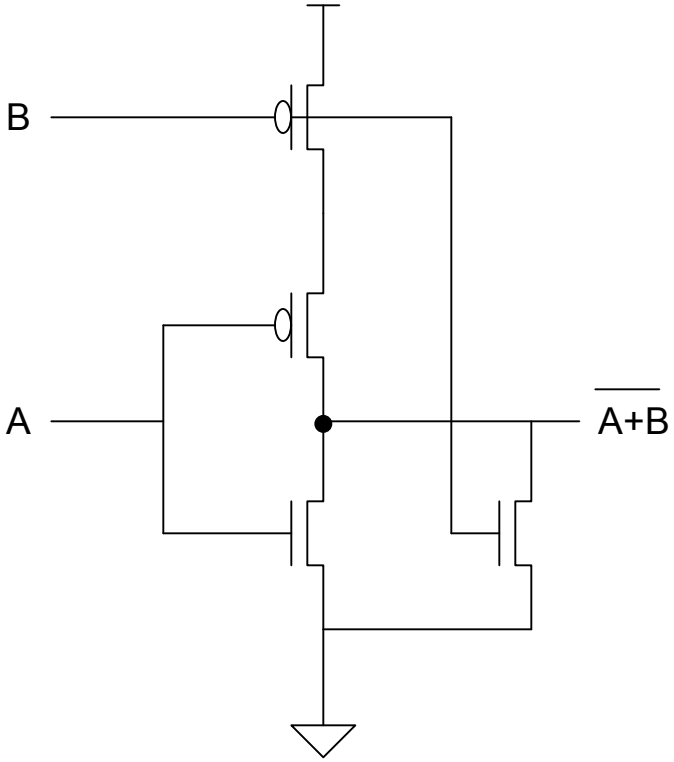
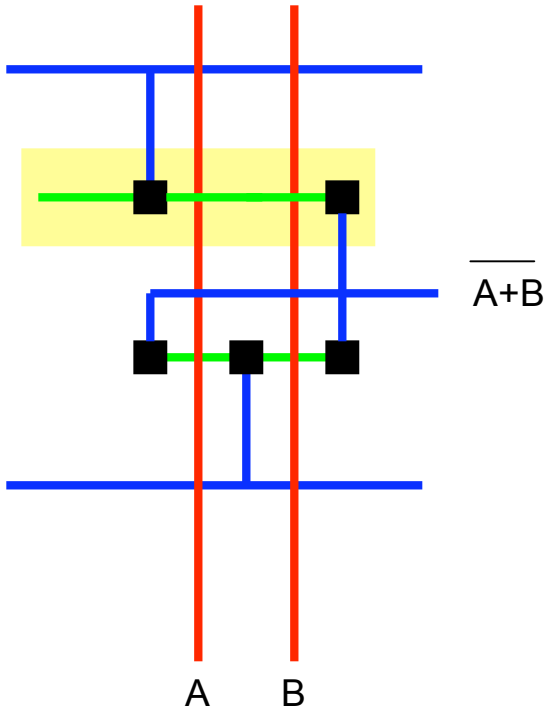
Layout strategies





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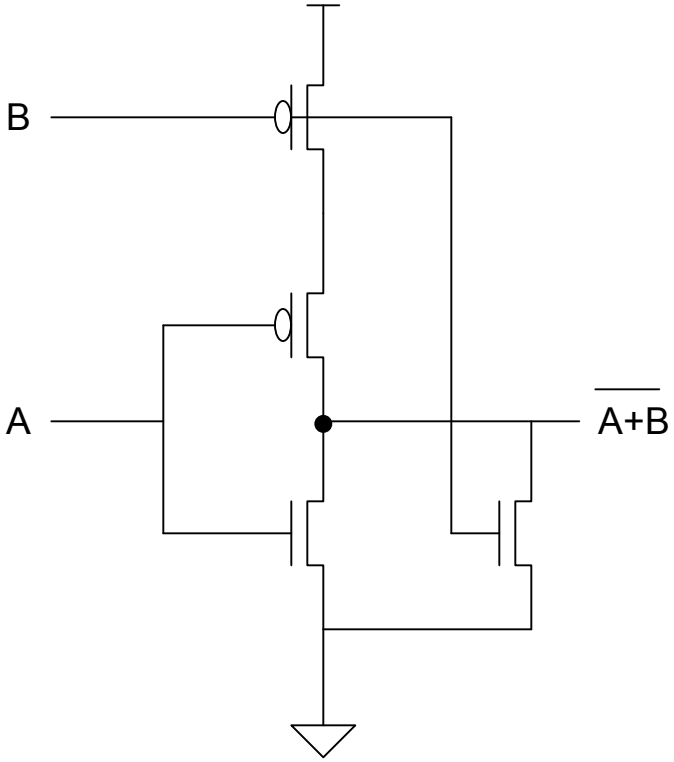
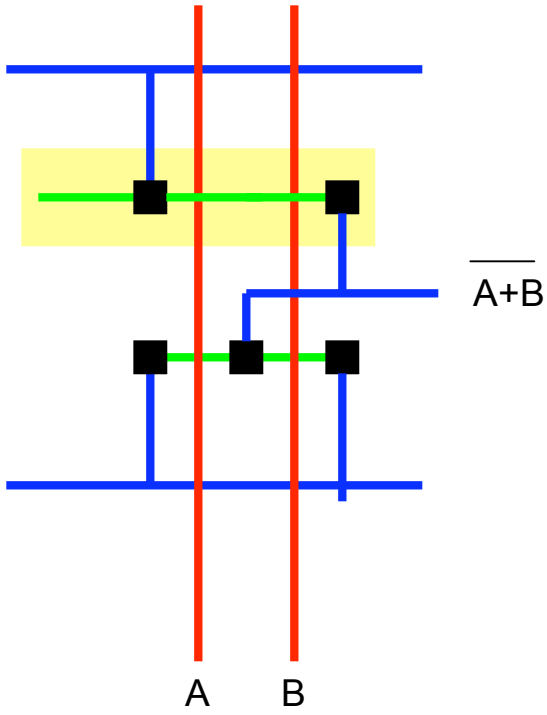
Layout strategies





Merged drain reduces output capacitance which will decrease switching time

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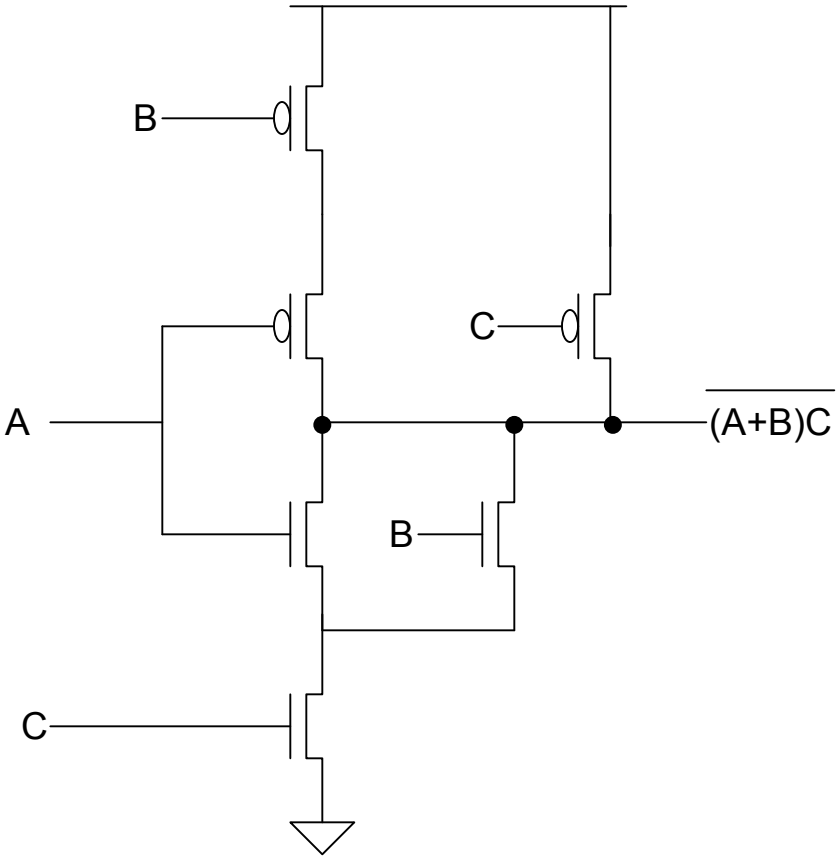
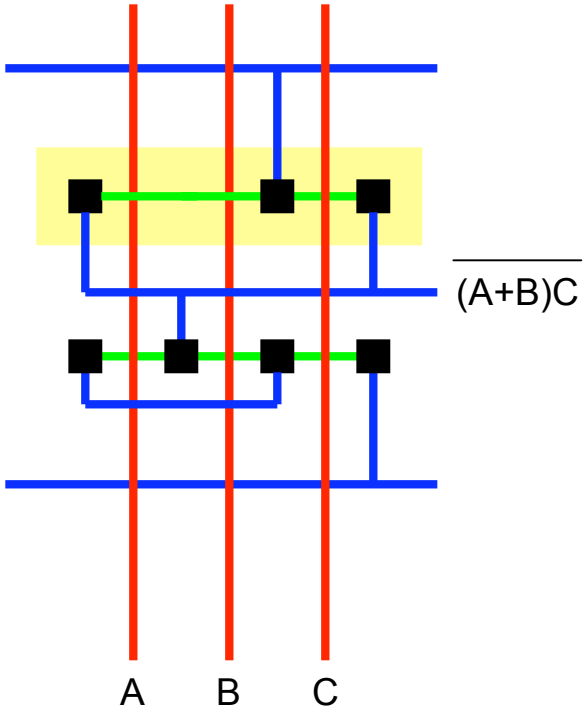
Layout strategies





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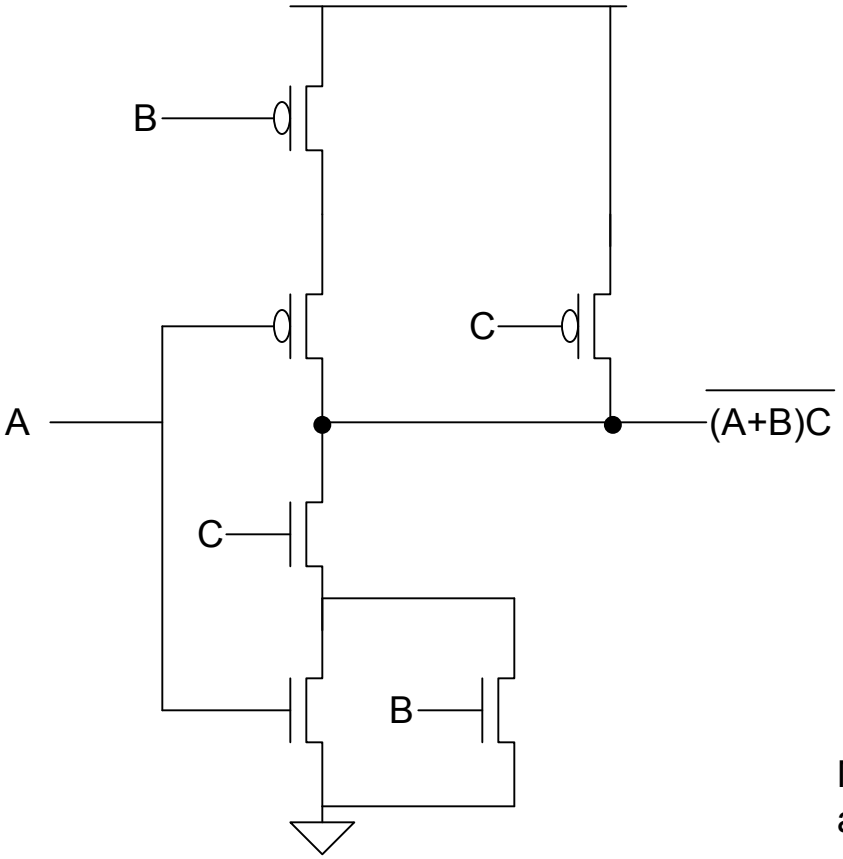
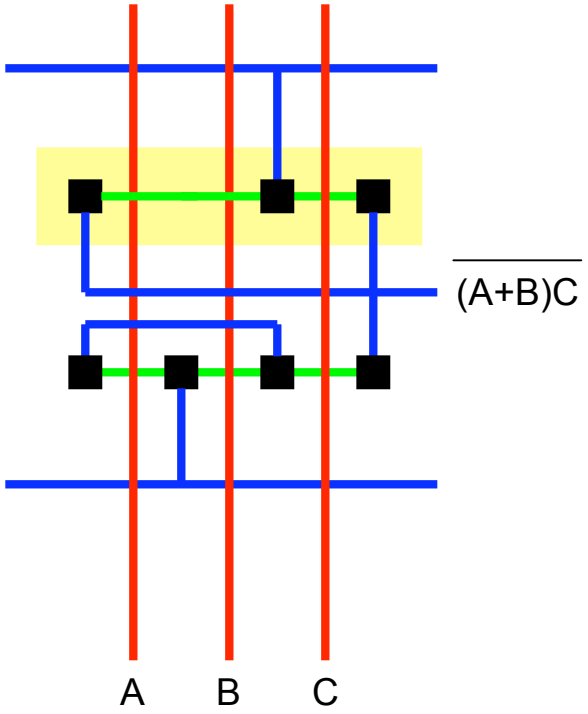
Layout strategies





Move higher capacitances closer to ground and away from output

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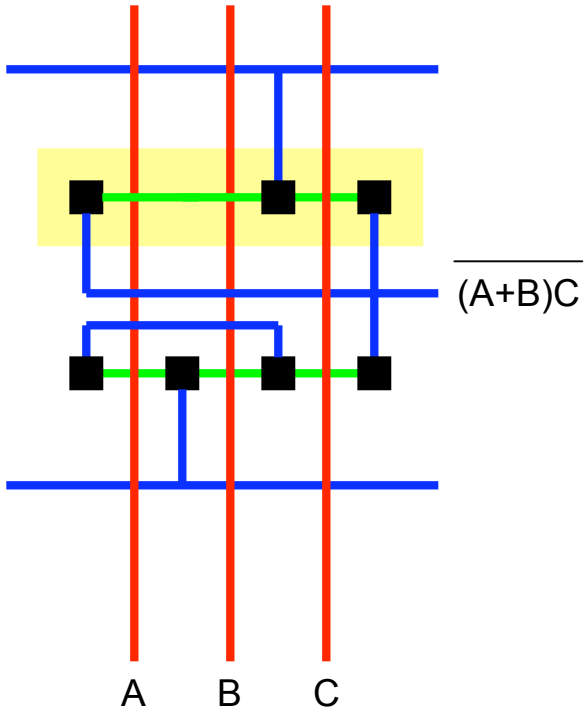
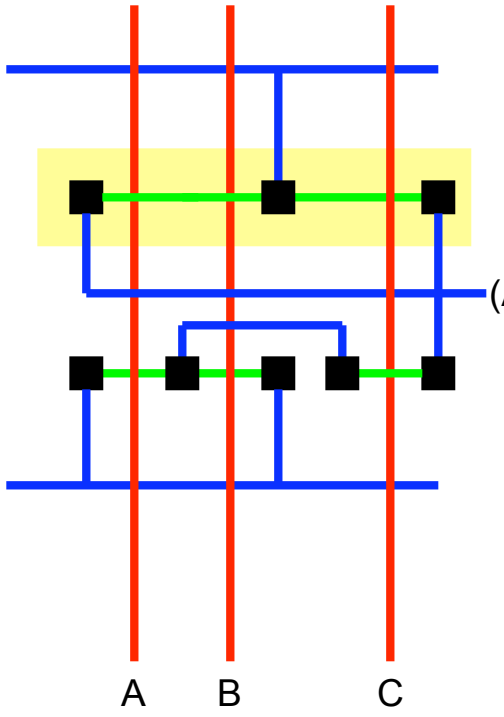
Layout strategies



$\overline{(A+B)C}$



$\overline{(A+B)C}$

Merged drain at A&B may cause the gate to become wider

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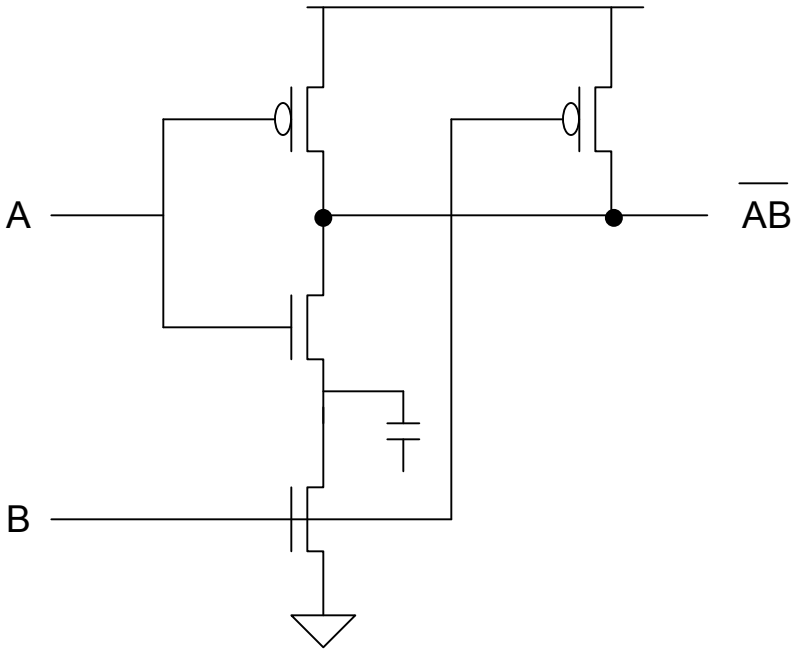
Layout strategies

•Ordering of inputs



- If A arrives before B, it will charge up the capacitance to VDD. When B arrives, it needs to discharge the capacitor.
- If B arrives before A, the capacitor will be discharged before A arrives.
- Try and put the early arriving signal close to ground - can speed NAND up to 20%

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Layout Choices

- Horizontal transistors
  - When FET sizes are similar
  - When data is in a vertical flow
- Vertical transistors
  - Different size FETs
  - Horizontal data flow
  - More complex functions

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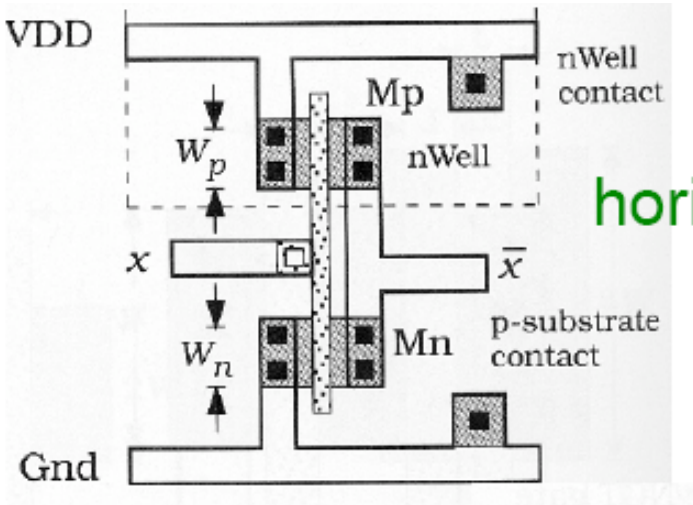
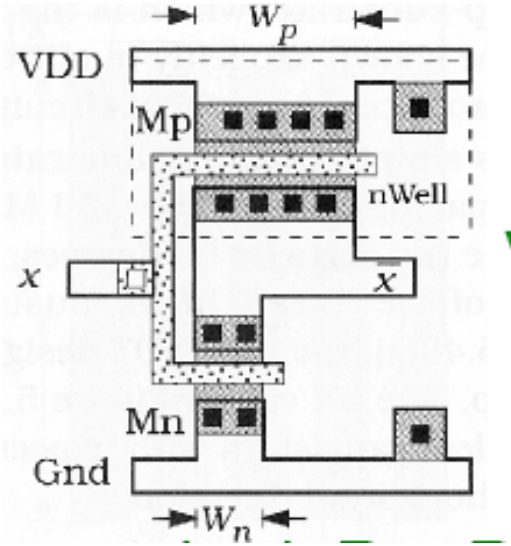
Layout choices



horizontal



vertical

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Layout choices

- Interconnect
  - Keep VDD and VSS in the highest level metal
  - Within a single cell, use a single layer of metal so you can route other metal layers above the cell
  - Limit the use of vias - can be up to 50Ω per via
  - Don't have long runs of poly

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Layout choices

- Consider how low level cells will interconnect with each other
- Minimize locally and compact globally
- Find critical areas first and then optimize

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Layout Process

- Design Rule Check (DRC)
  - Check if all design rules are met
- Layout vs. Schematic (LVS)
  - Make sure that the layout matches your schematic

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Next class

- Exam 1
- Power Dissipation
- Final Project

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