Topics

- Exam 1
- Arithmetic Operators

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Exam 1

- Average: 62.6
- Median: 72

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Power dissipation

$$P = \frac{1}{T}\left[\int_0^{\frac{T}{2}} i_n(t) V_{out}\, dt + \int_{\frac{T}{2}}^{T} i_p(t)\left(V_{DD} - V_{out}\right)\right]$$

$$= \frac{1}{T}\left[-C_L \int_{V_{DD}}^{0} V_{out}\, dV_{out} + C_L \int_0^{V_{DD}} \left(V_{DD} - V_{out}\right) dV_{out}\right]$$

$$= \frac{C_L}{T}\left[\frac{{V_{DD}}^2}{2} + \frac{{V_{DD}}^2}{2}\right]$$

$$= C_L {V_{DD}}^2 f_{0\to 1}$$

$$P = C_L {V_{DD}}^2 \alpha_{0\to 1} f$$

- α is the activity factor - I.e. the probability that a clock event results in a 0→1 transition

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Power dissipation

- Example - NAND gate with independent and uniformly distributed inputs.
  - Probability of NAND gate outputs: P_0=0.25 and P_1=0.75.
  - Therefore, probability of 0→1 transition is $\alpha_{0\to1} = P_0P_1 = 0.1875$

$$
\begin{aligned}
V_{DD} &= 5V \\
f &= 1GHz \\
C_L &= 1pF \\
P &= C_L V_{DD}^2 \alpha_{0\to1} f \\
&= 1pf \cdot 5^2 \cdot 0.1875 \cdot 1GHz \\
&= 4.7mW
\end{aligned}
$$

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Building Blocks for Digital Architectures

Arithmetic unit

- Bit-sliced datapath (adder, multiplier, shifter, comparator, etc.)

Memory

- RAM, ROM, Buffers, Shift registers

Control

- Finite state machine (PLA, random logic.)
- Counters

Interconnect

- Switches
- Arbiters
- Bus

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Datapath operators

- Operate on multiple bits at once
- Allows tight design of several elements
  - Arithmetic/logic functions, shifters
  - Registers, Register Files
  - Wires, buses

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Control

- Control signals determine the flow of data along the datapath
- Fuctional control of data
  - Whether to add or subtract
  - When to store to what register
  - Which wires to transmit data on

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Datapath and Control

- Separation of datapath and control simplifies design
- Layout strategy
  - Datapath horizontal in metal2
  - Control vertical in metal1

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Datapath design

- Components
  - Storage elements (registers, latches, etc.)
  - Operators (adders, shifters, comparators, etc.)
  - Interconnect (buses, wires)
- Characteristics
  - Wide data transfers for regularity and modularity
  - Large capacitances on buses - cross-coupling
  - Large fanout on buses
  - Critical path on carry signals

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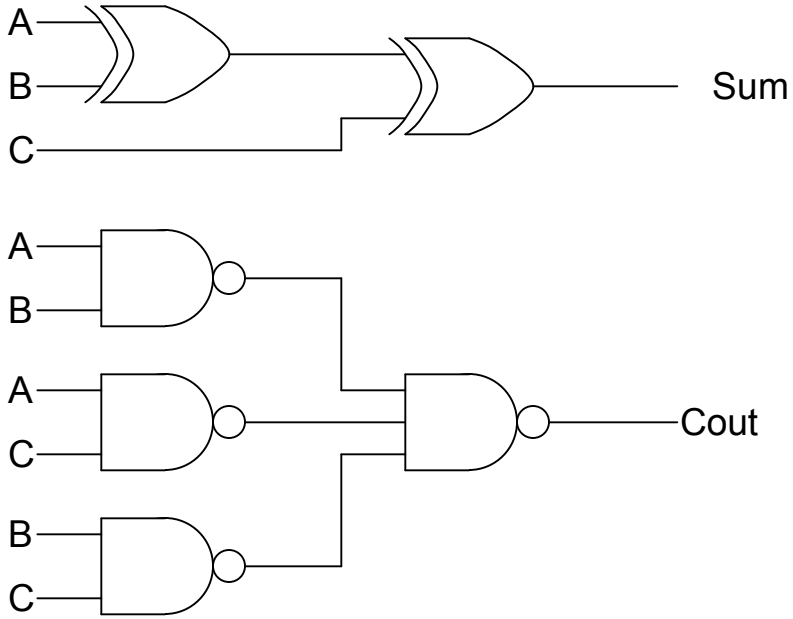
Datapath operators

- Full Adder

$$Sum = A \oplus B \oplus C$$

$$Cout = AB + BC + AC$$



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Datapath operators

- Full Adder

$$
\begin{aligned}
Sum &= A \oplus B \oplus C \\
&= ABC + A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}C \\
&= ABC + (A + B + C)\left(\overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}\right) \\
&= ABC + (A + B + C)\left(\overline{(A + B)(B + C)(A + C)}\right) \\
&= ABC + (A + B + C)\left(\overline{AB + BC + AC}\right) \\
&= ABC + (A + B + C)\left(\overline{Cout}\right)
\end{aligned}
$$

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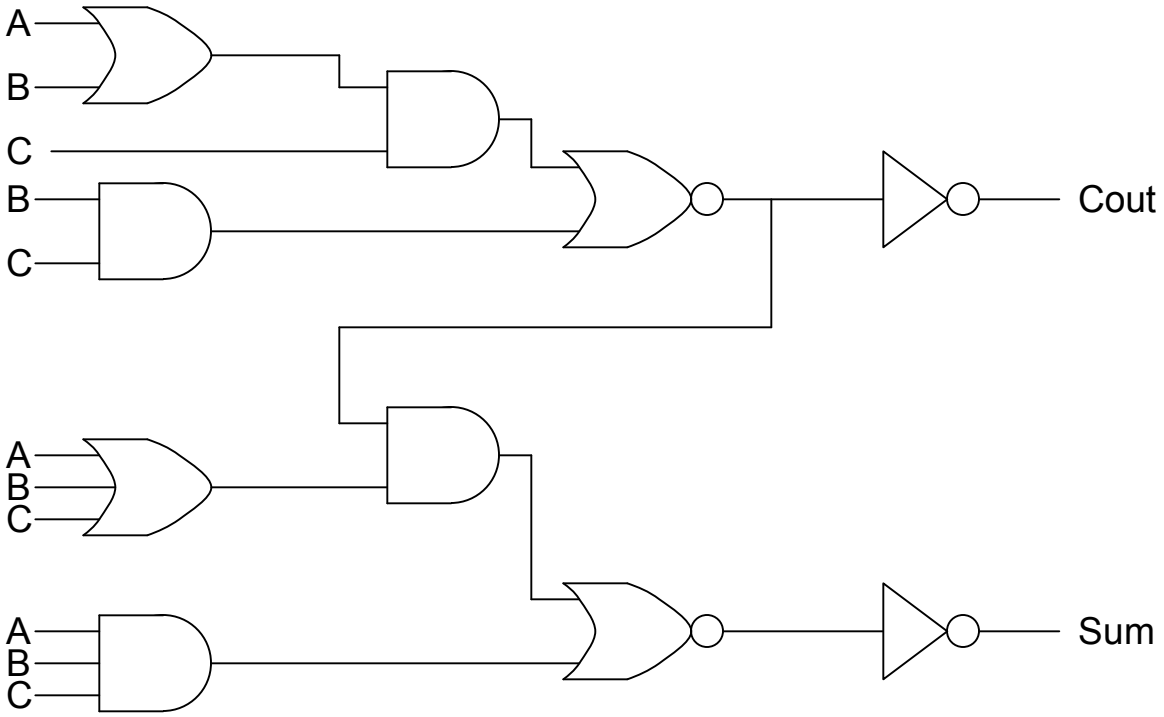
Datapath operators

- Full Adder



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Datapath operators

- Full adder

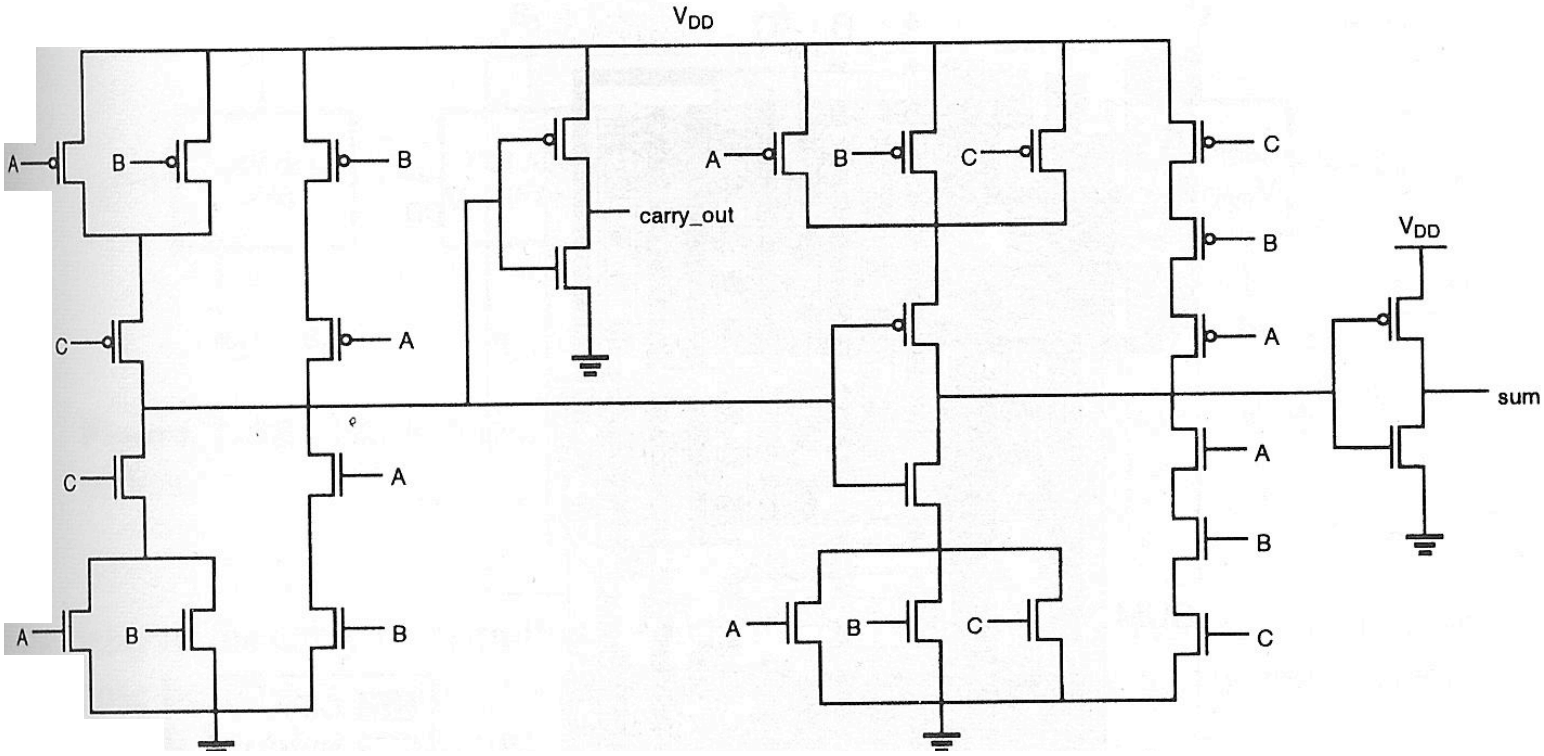

Fig. 7.28, “CMOS Digital Integrated Circuits”, Kang and Leblebici

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Datapath operators

$$\overline{AB + BC + AC} = \overline{AB} \cdot \overline{BC} \cdot \overline{AC}$$
$$= \left(\overline{A} + \overline{B}\right)\left(\overline{B} + \overline{C}\right)\left(\overline{A} + \overline{C}\right)$$
$$= \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}$$

- Equivalent duals
  - Possible when $\overline{F} = F\left(\overline{A}, \overline{B}, \overline{C}, \ldots\right)$
  - Allows much simpler layout because the pulldown and pullup networks are the same

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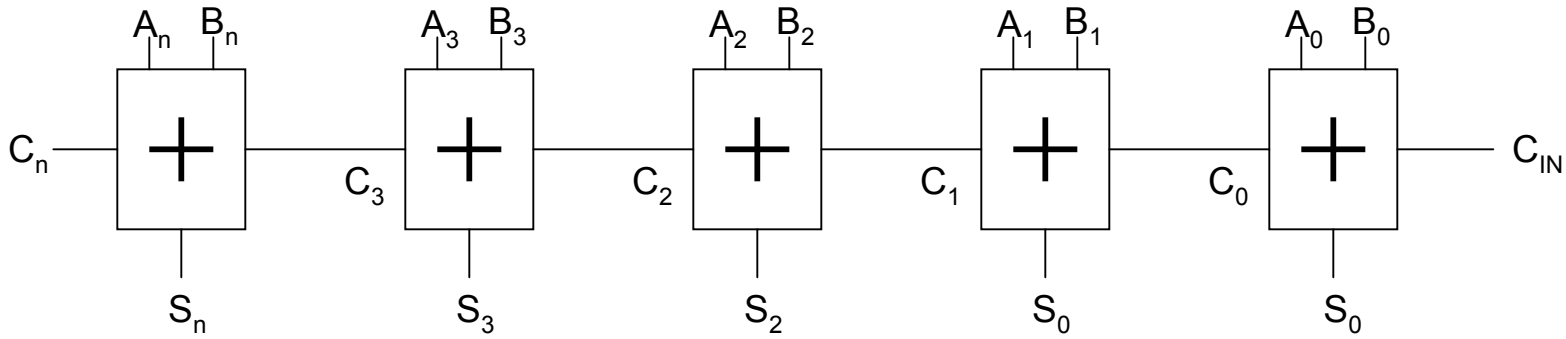
Datapath operators

- Ripple carry adder



- Carry delay increases with number of bits

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Datapath operators

- Carry lookahead adders
  - Calculate carry in parallel with sum
  - Each carry bit is dependent on inputs only - not previous carry

$$C_i = A_i B_i + A_i C_{i-1} + B_i C_{i-1}$$

$$C_0 = A_0 B_0 + (A_0 + B_0) C_{in}$$

$$C_1 = A_1 B_1 + (A_1 + B_1) A_0 B_0 + (A_1 + B_1)(A_0 + B_0) C_{in}$$

$$C_2 = A_2 B_2 + (A_2 + B_2) A_1 B_1 + (A_2 + B_2)(A_1 + B_1) A_0 B_0 + (A_2 + B_2)(A_1 + B_1)(A_0 + B_0) C_{in}$$

$$C_i = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + P_i P_{i-1} P_{i-2} G_{i-3} + \ldots + P_i \ldots P_0 C_{in}$$

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Datapath operators

- Carry lookahead adders
  - For more than 4 bits, the effect of fanout can be significant - the delay through the carry generate logic could be more than the carry ripple delay
  - Usually divide the data into four bit chunks with a hierarchy of propagate and generate circuitry

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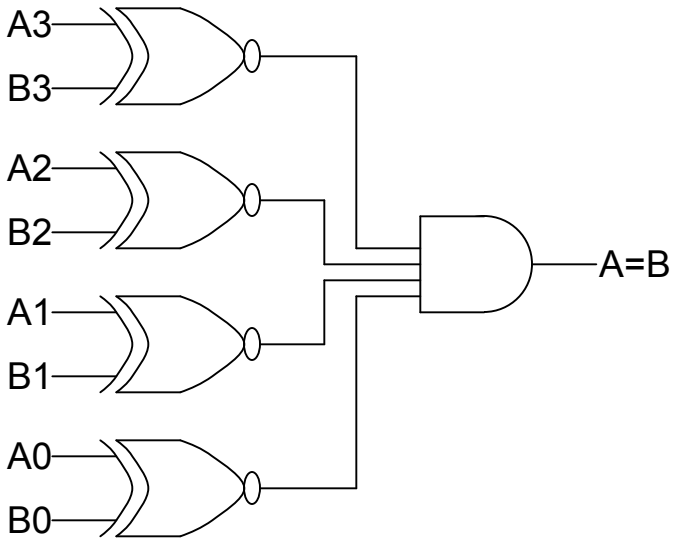
Datapath operators

- Comparators



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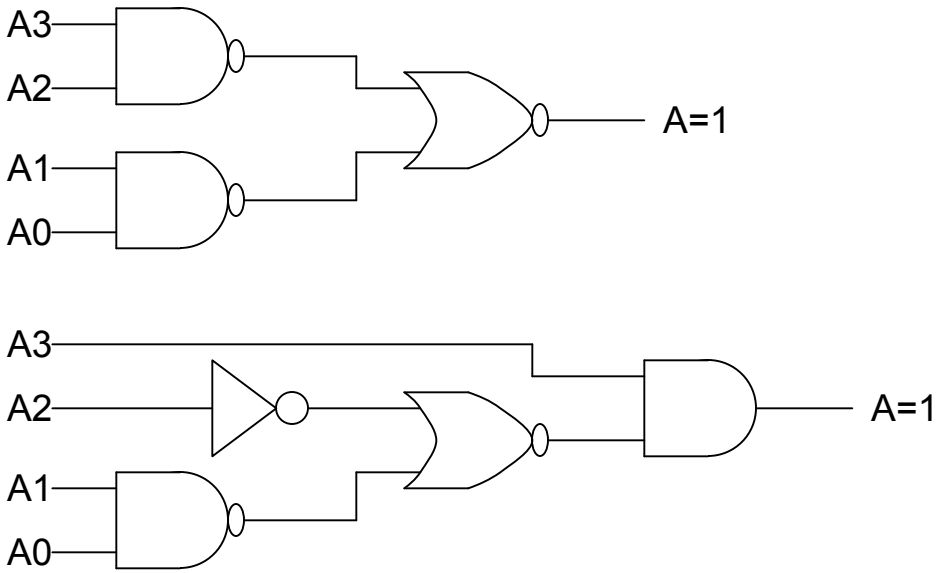
Datapath operators

- Detection



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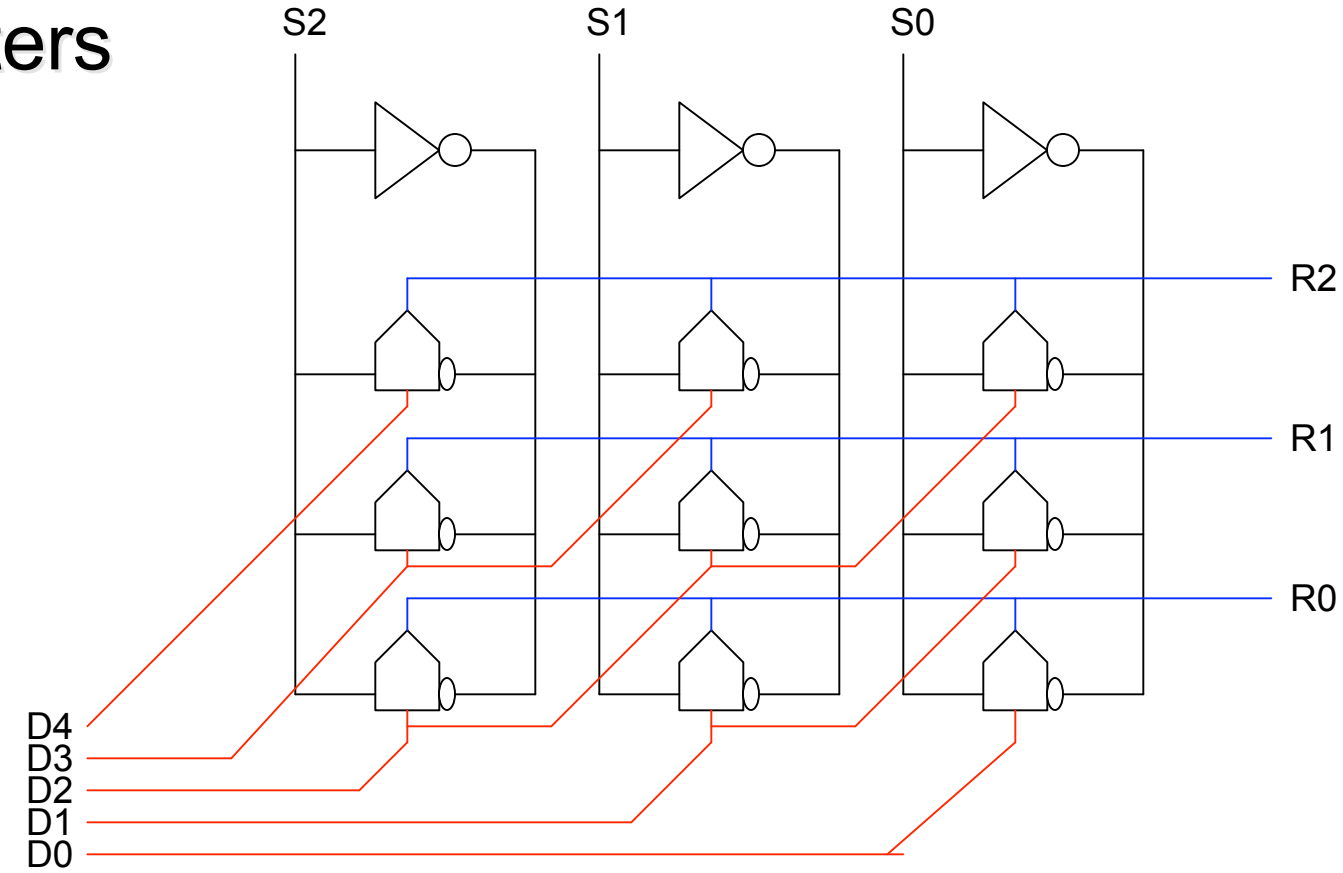
Datapath operators

- Shifters



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Datapath operators

- Wider datapaths means longer delays
- When designing datapath operators, tradeoff between ripple delays and multi-input gates

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Datapath bus design

- Long buses typical in datapaths
- Large capacitances due to bus length and loading of multiple inputs
- Use precharging to speed up buses

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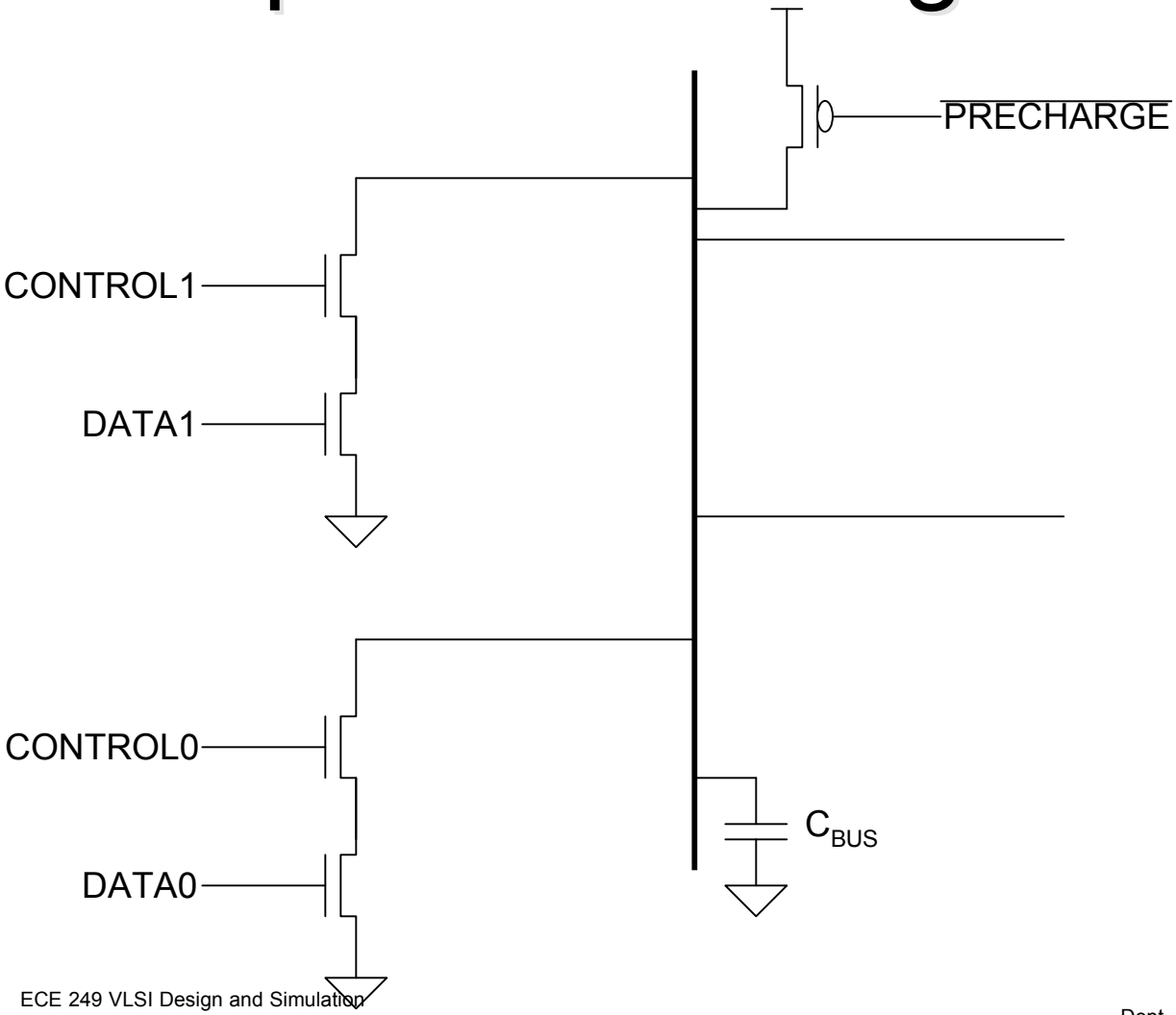
Datapath bus design



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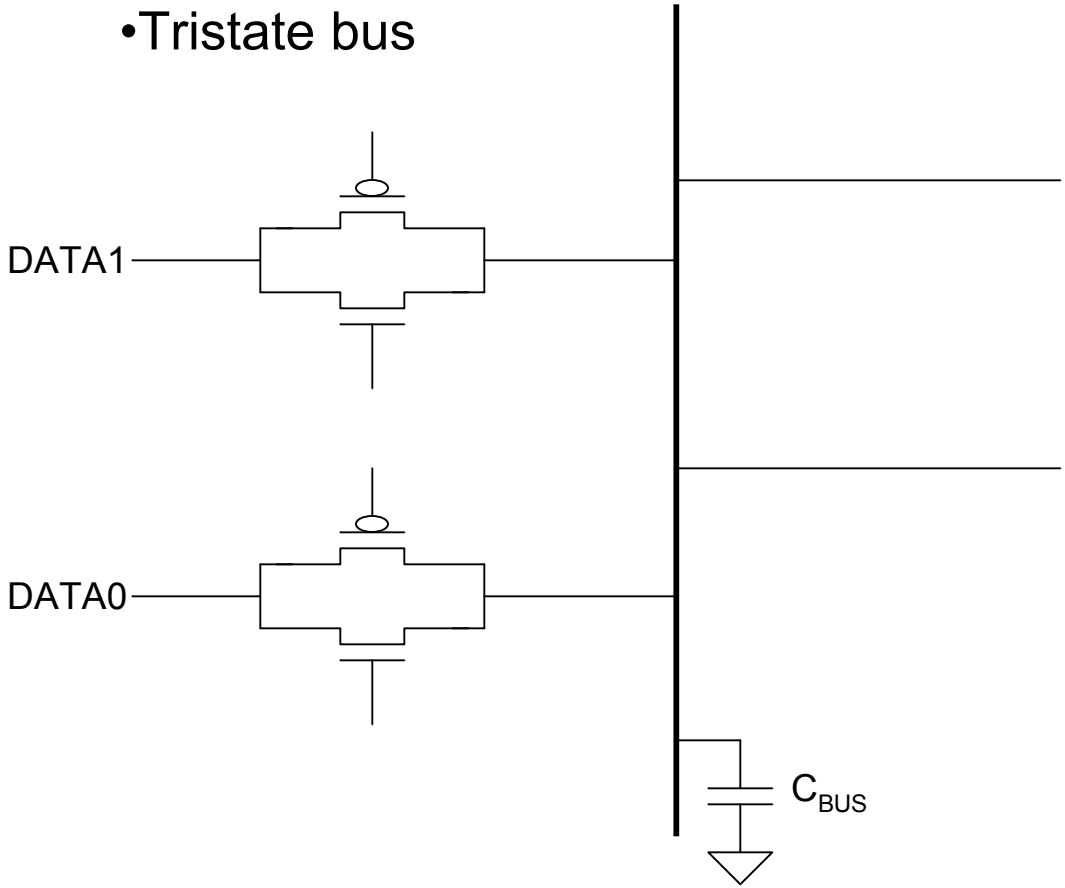
Datapath bus design

- Tristate bus



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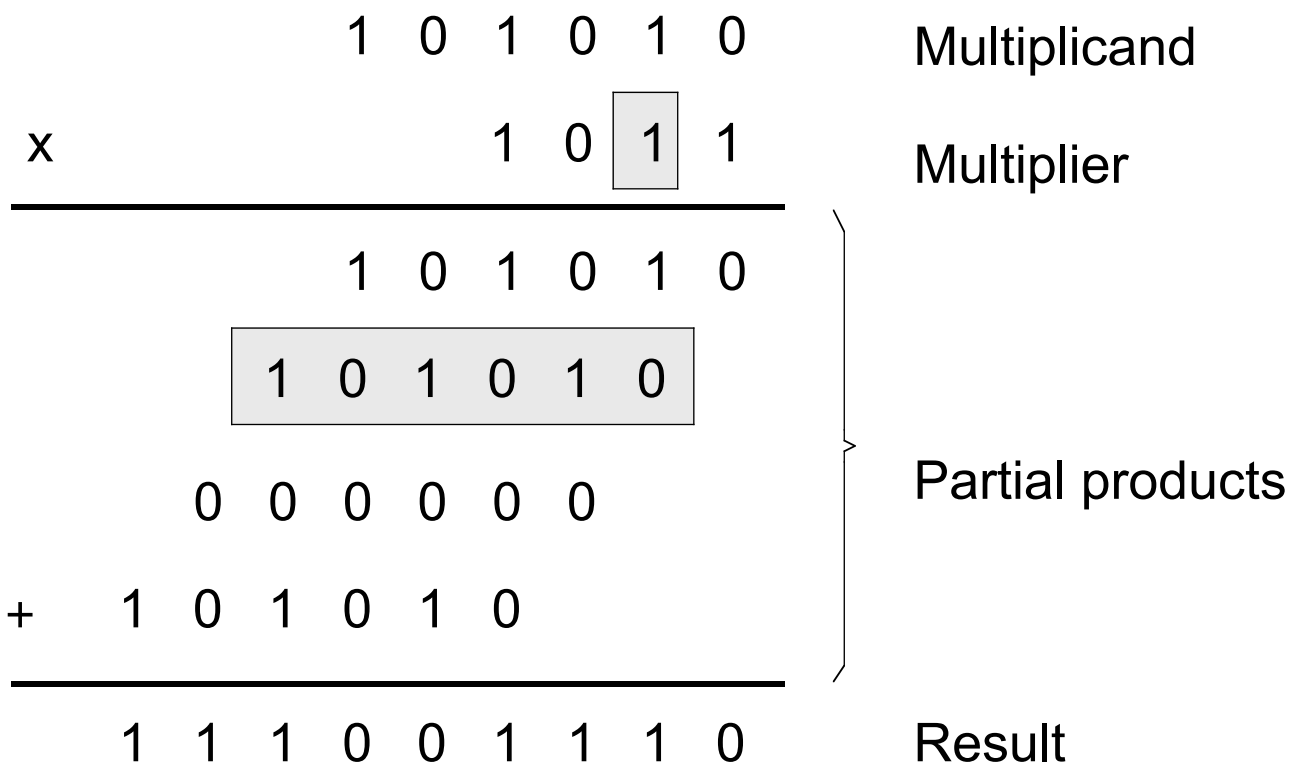
Binary Multiplication



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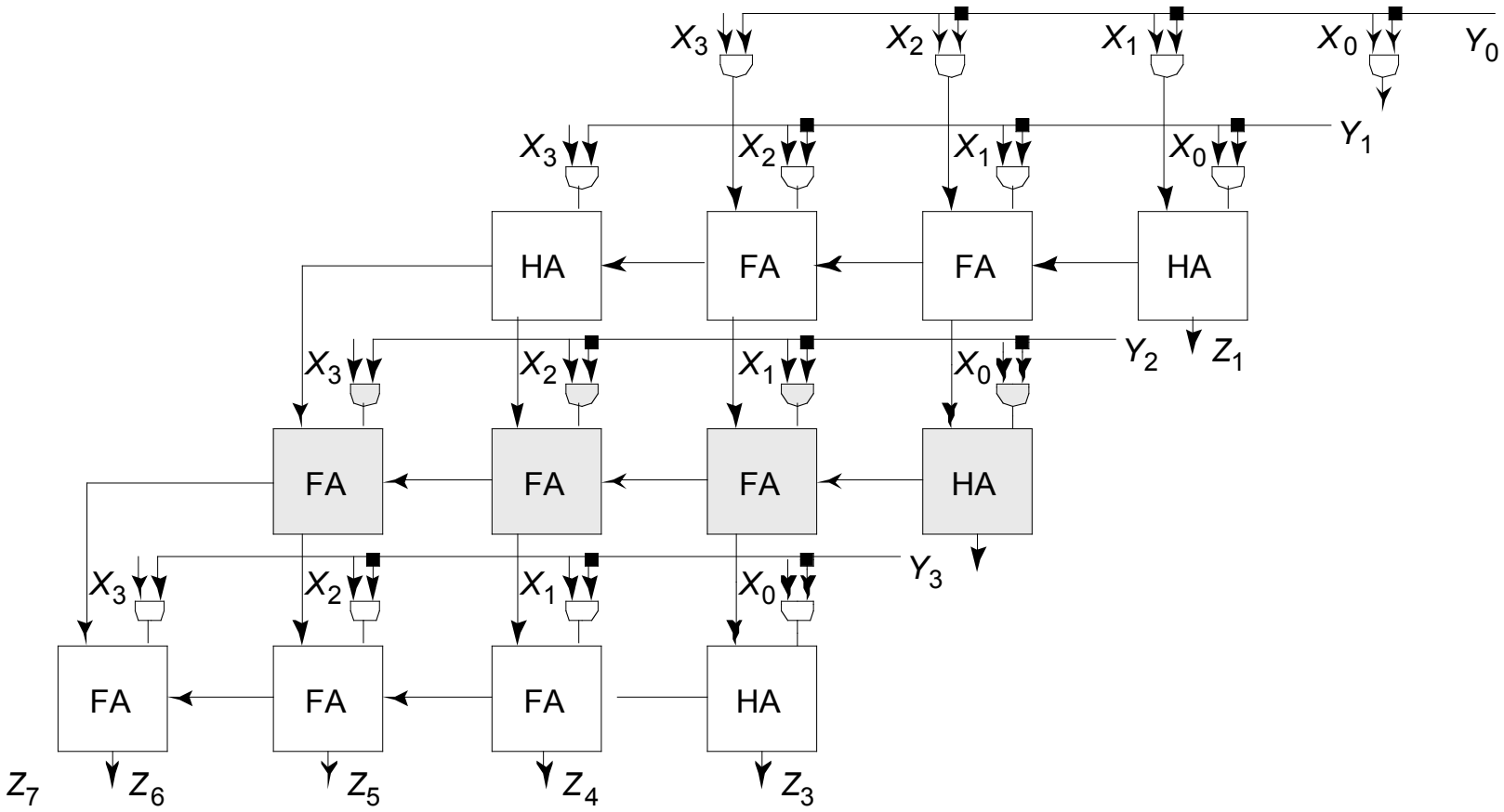
The Array Multiplier



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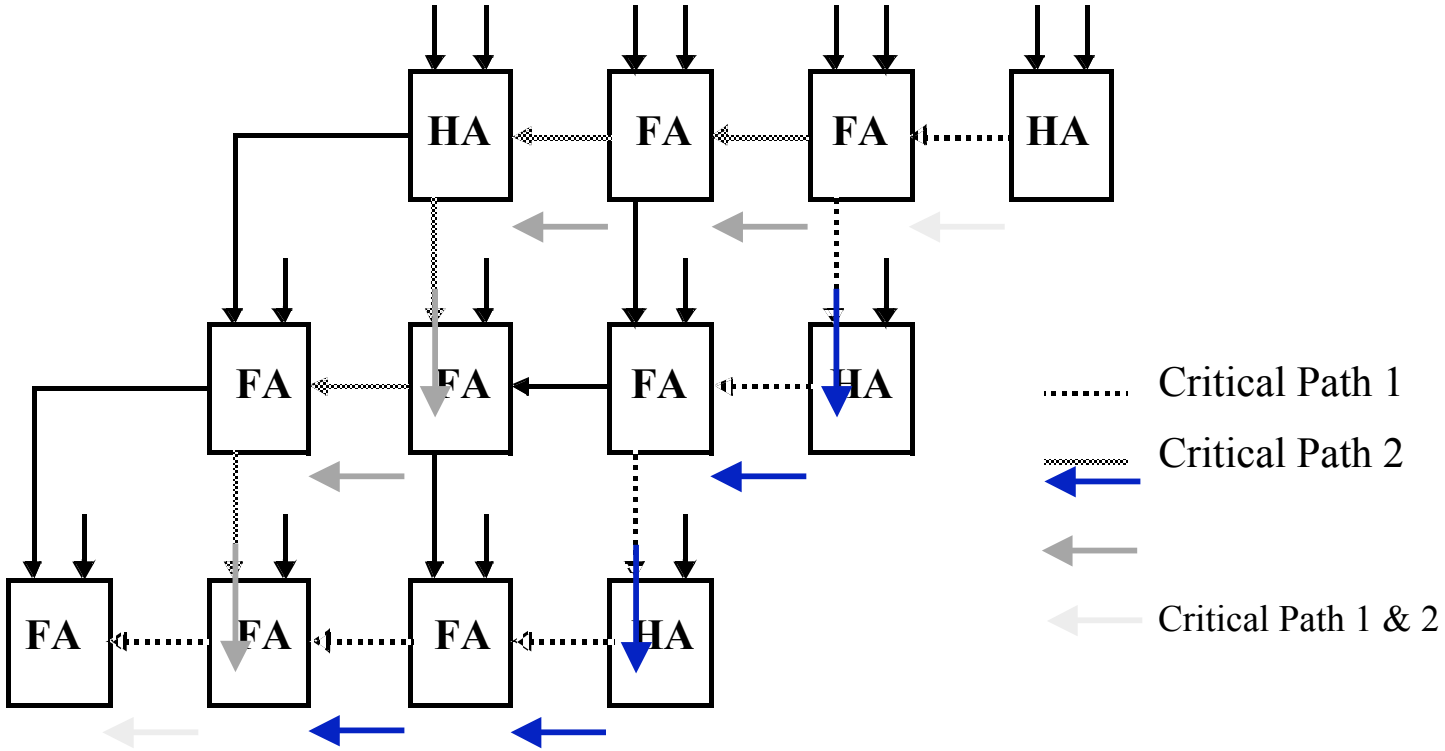
The MxN Array Multiplier — Critical Path



$$t_{mult} \approx [(M-1)+(N-2)]t_{carry}+(N-1)t_{sum}+(N-1)t_{and}$$

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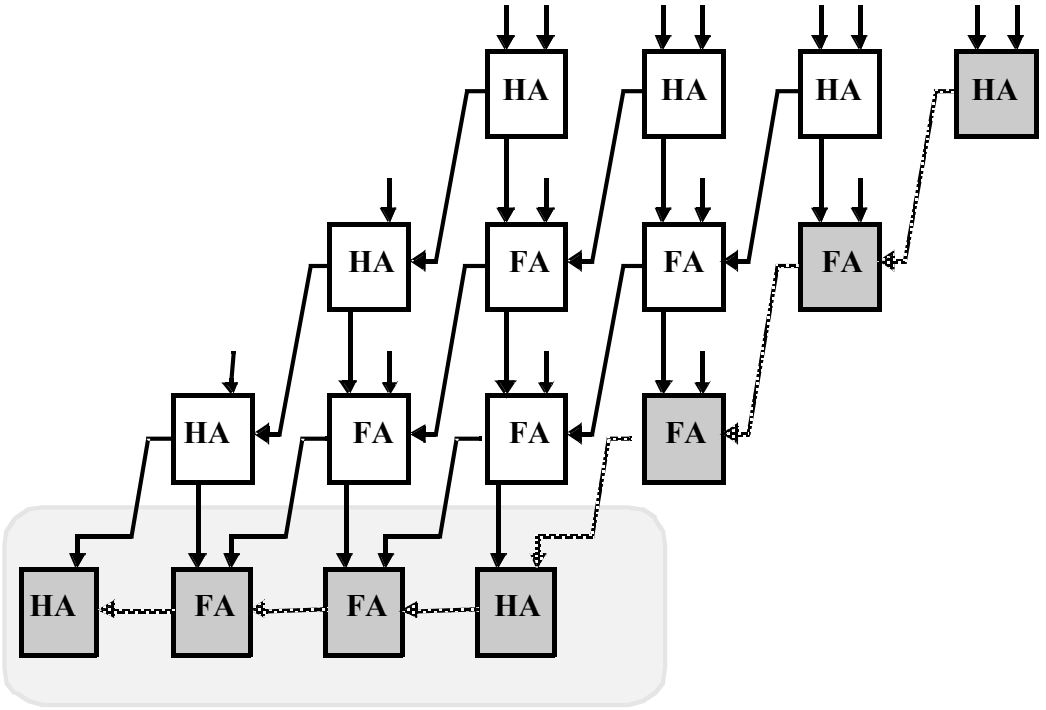
Carry-Save Multiplier



Vector Merging Adder

$$t_{mult} = (N-1)t_{carry} + (N-1)t_{and} + t_{merge}]$$

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Next Class

- VLSI Logic Styles
- Read Chapters 6.2.2, 6.2.3, 6.3, and 6.4
- Lab 4 due tomorrow
- Final Project proposals due Thursday
- Homework 4 due 3/17

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