VLSI Logic Structures

- Ratioed Logic
- Pass-Transistor Logic
- Dynamic CMOS
  - Domino Logic
  - Zipper CMOS

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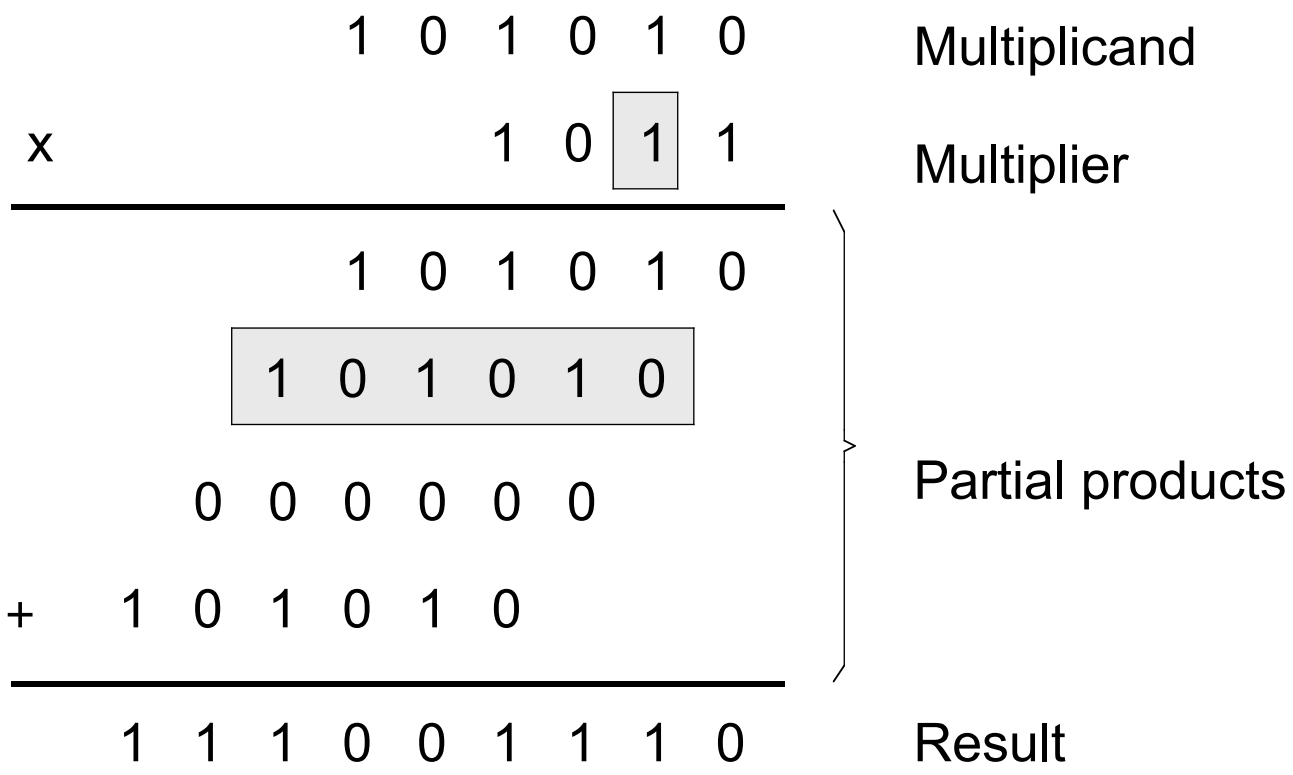
Binary Multiplication



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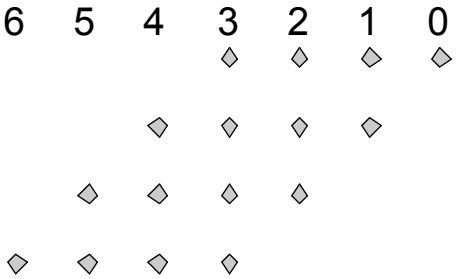
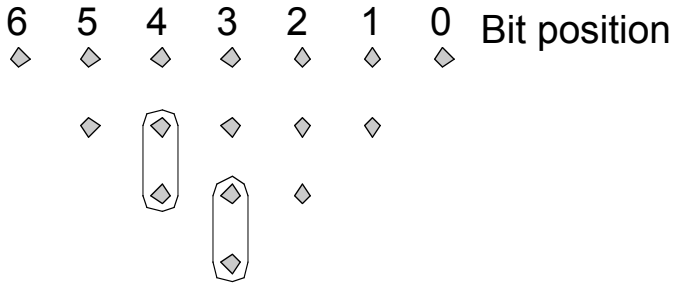
Wallace-Tree Multiplier

Partial products



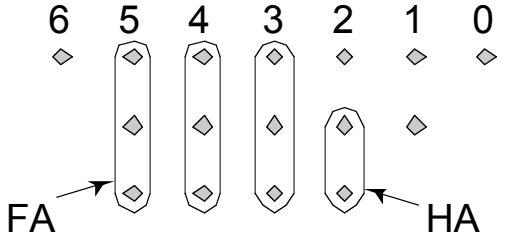
(a)

First stage



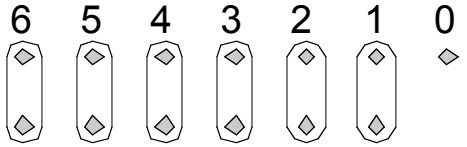
(b)

Second stage



(c)

Final adder



(d)

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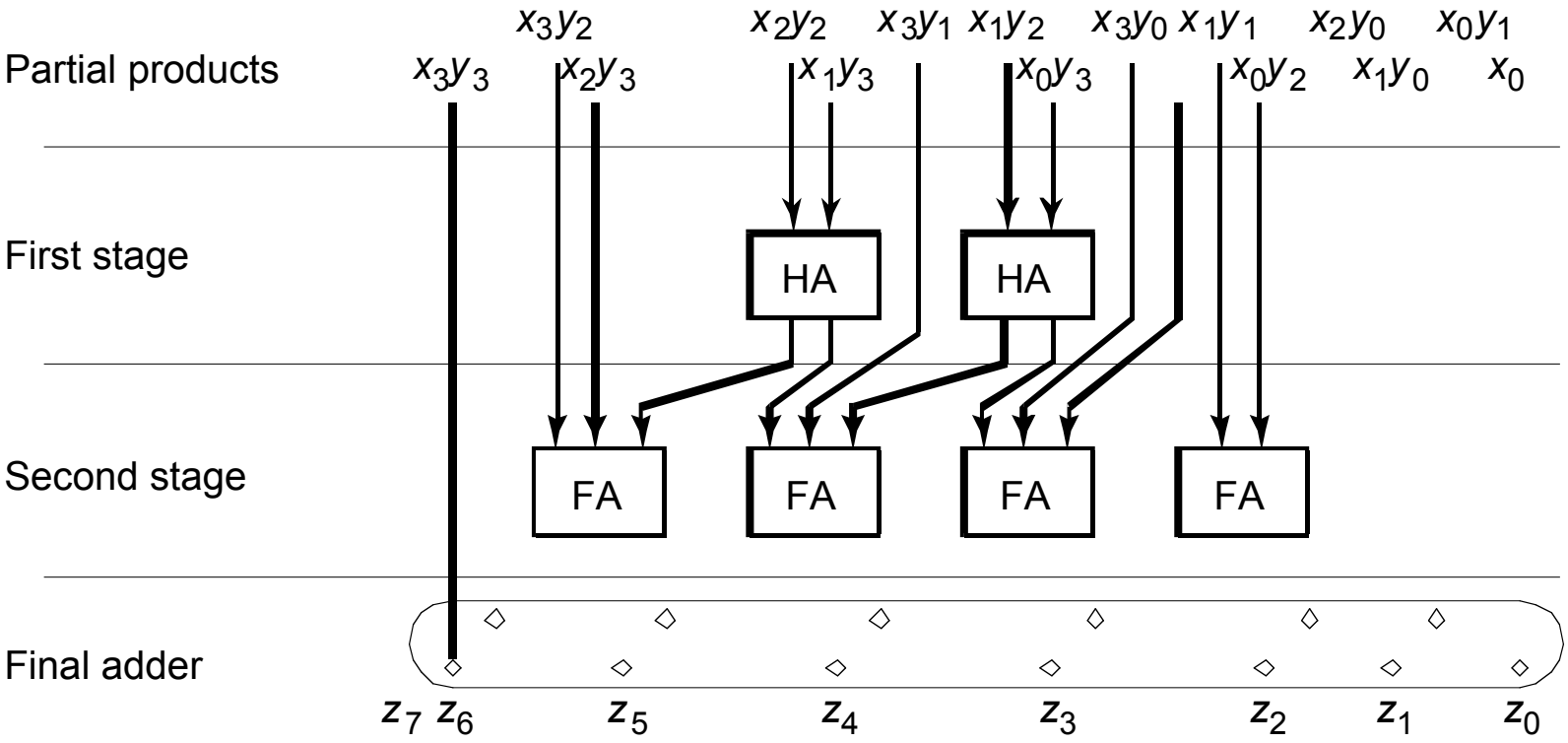
Wallace-Tree Multiplier



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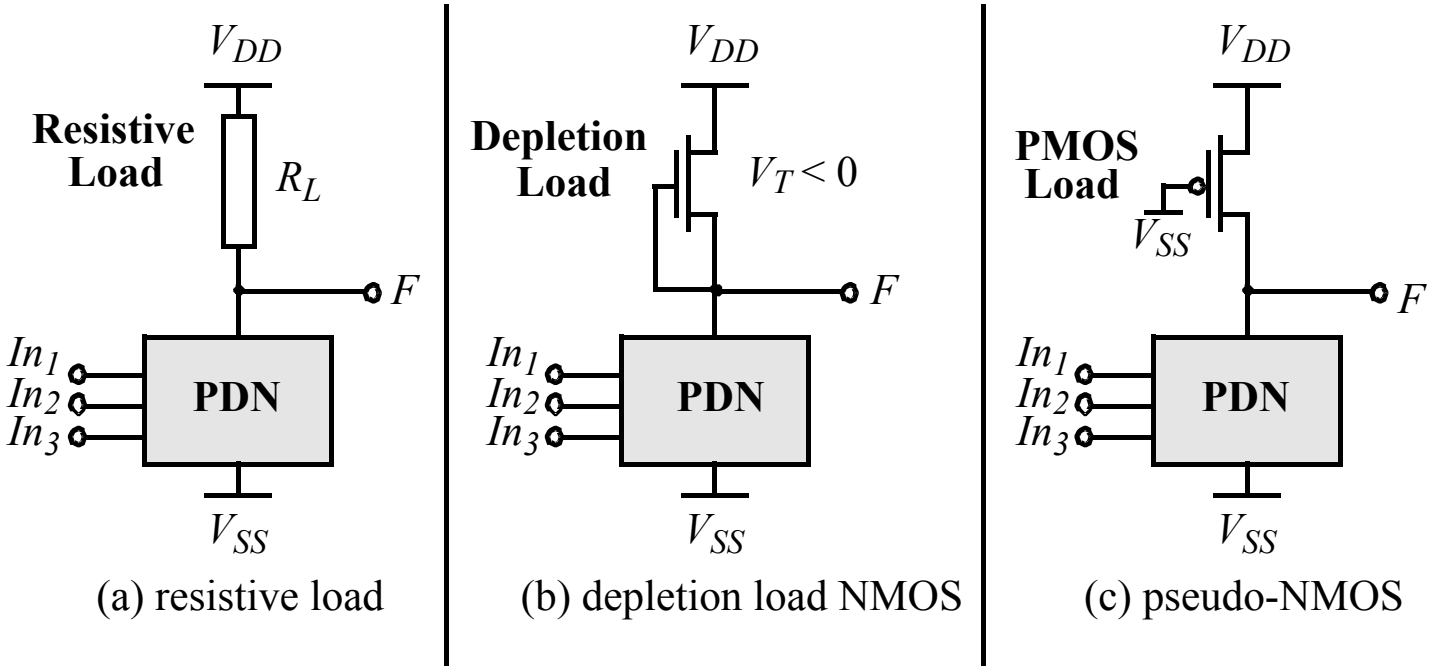
Ratioed Logic



Goal: to reduce the number of devices over complementary CMOS

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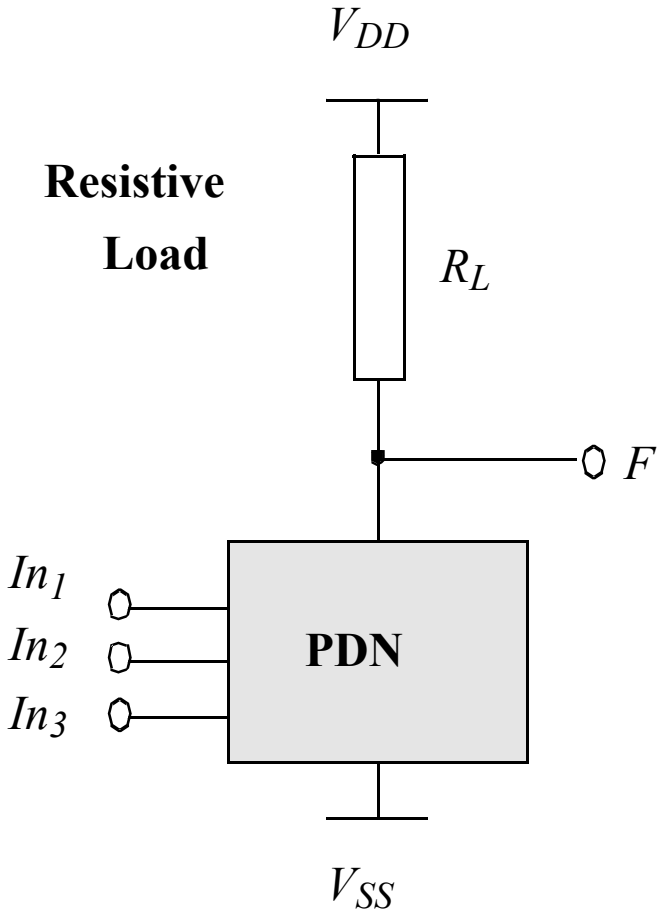
Ratioed Logic



- **N transistors + Load**
- **$V_{OH} = V_{DD}$**
- **$V_{OL} = \dfrac{R_{PN}}{R_{PN} + R_L}$**
- **Assymetrical response**
- **Static power consumption**
- **$t_{pL} = 0.69\, R_L C_L$**

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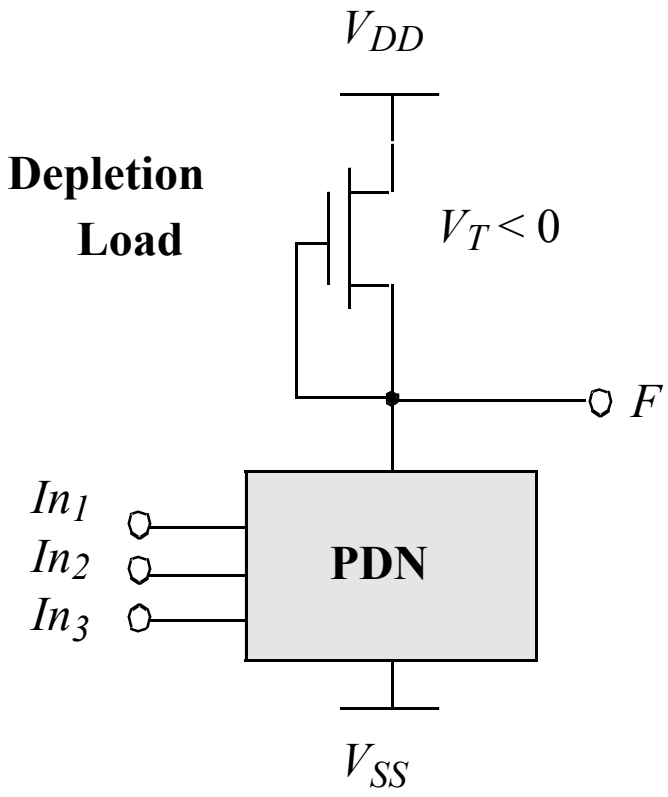
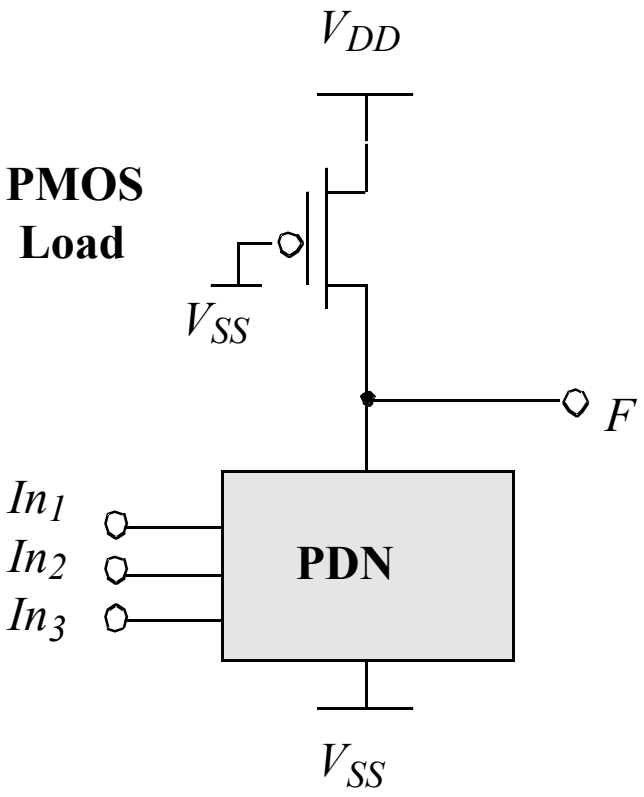
Active Loads



depletion load NMOS



pseudo-NMOS

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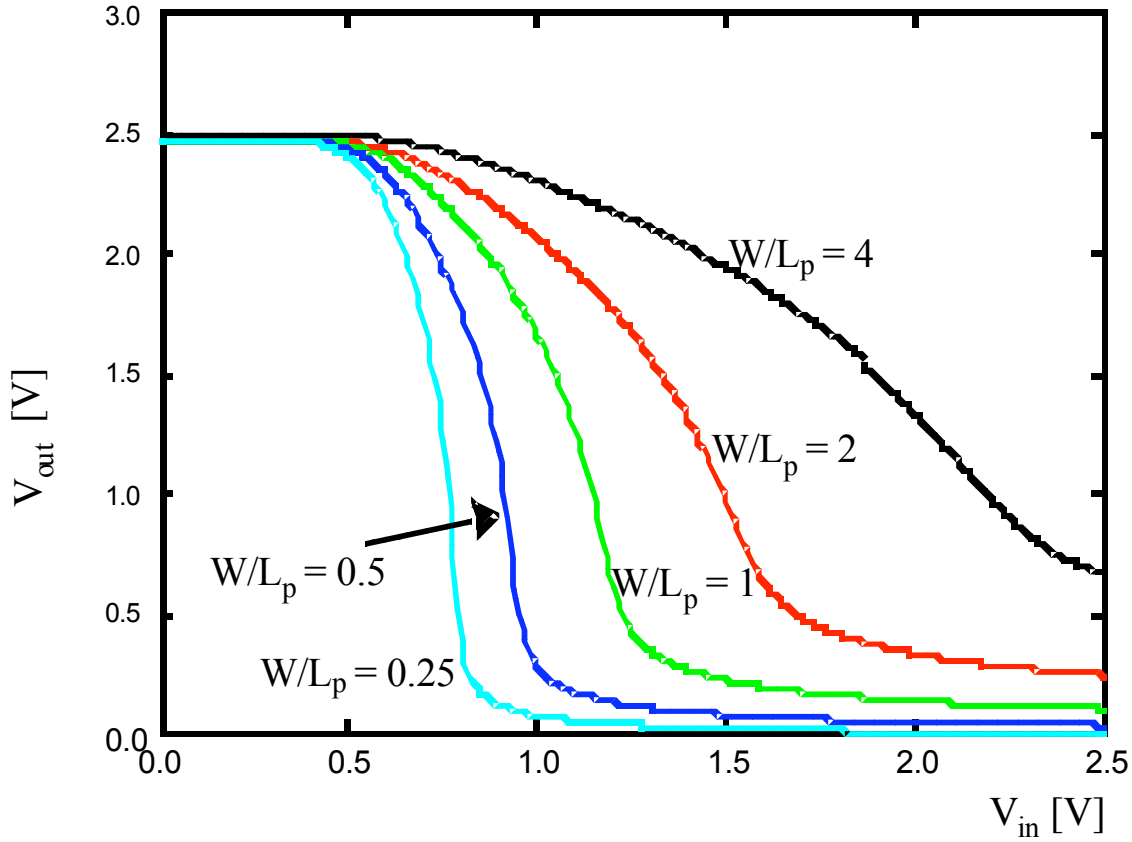
Pseudo-NMOS VTC



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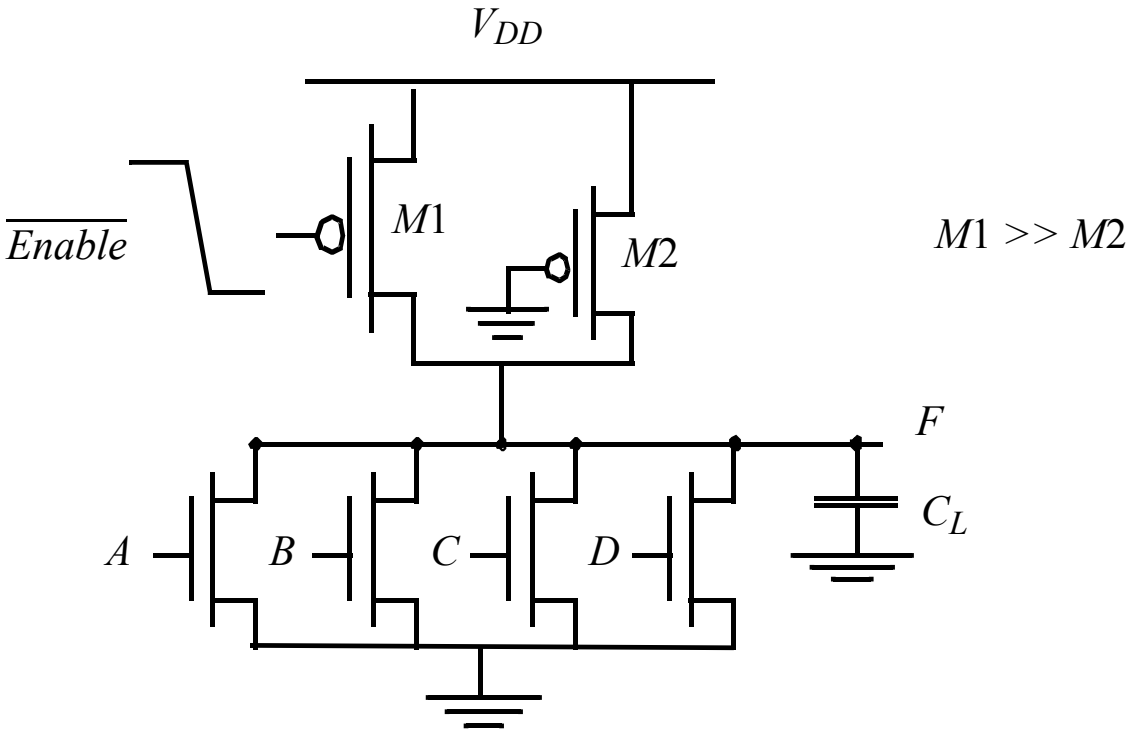
Improved Loads



Adaptive Load

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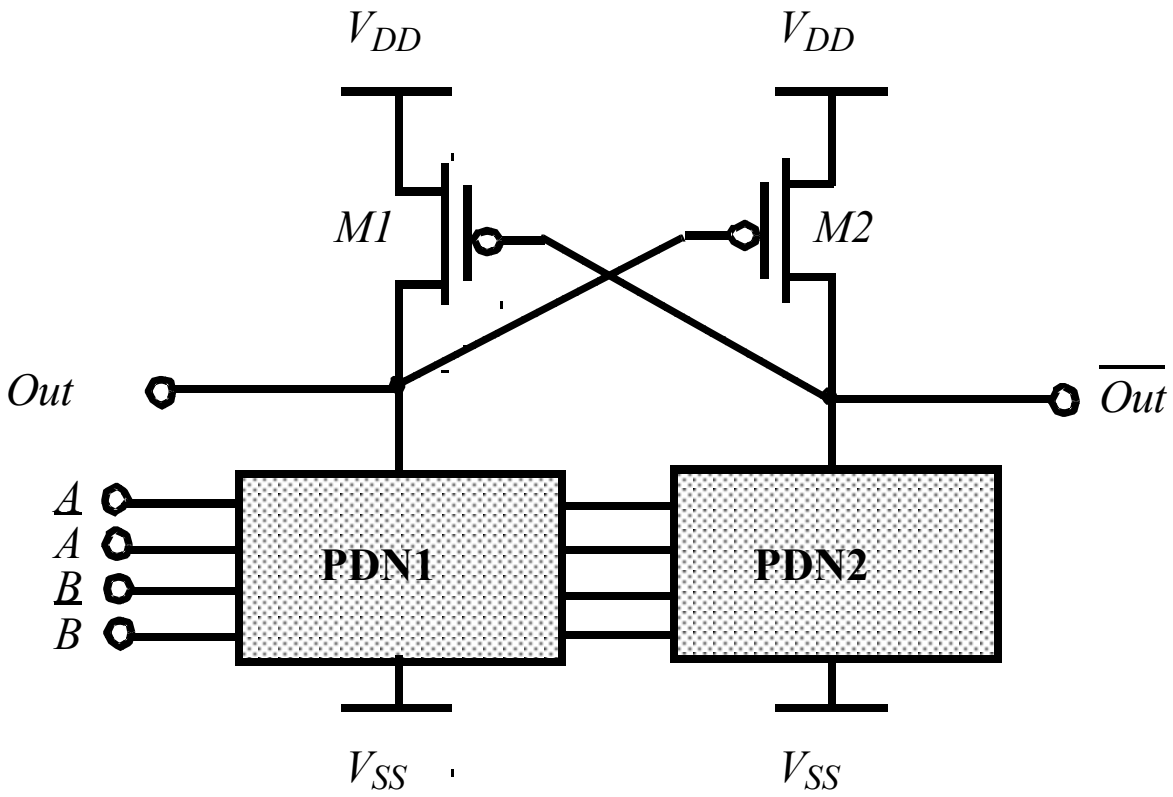
Improved Loads (2)



Differential Cascode Voltage Switch Logic (DCVSL)

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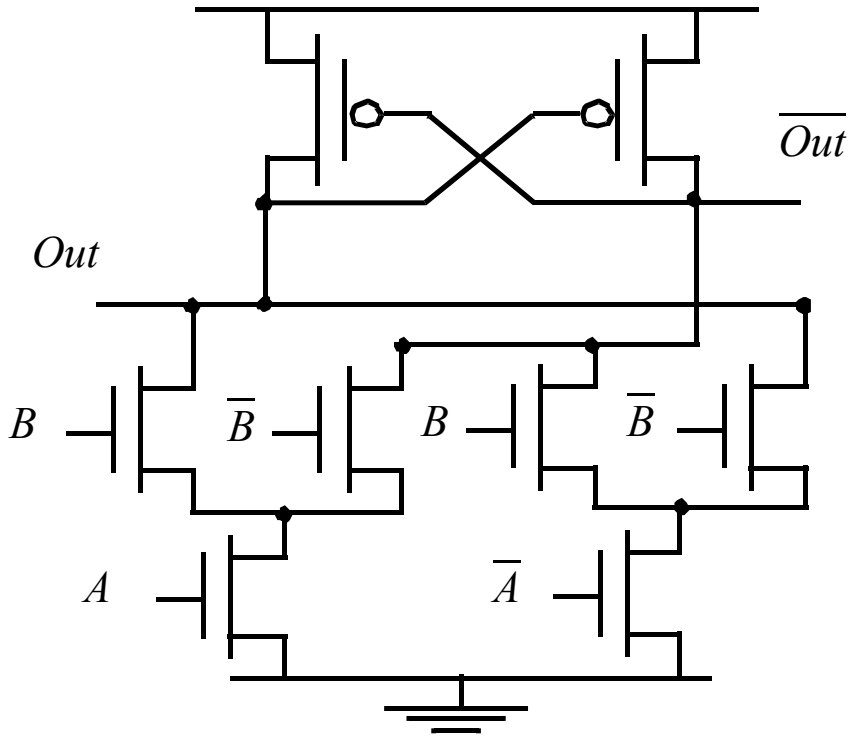
DCVSL Example



XOR-NXOR gate

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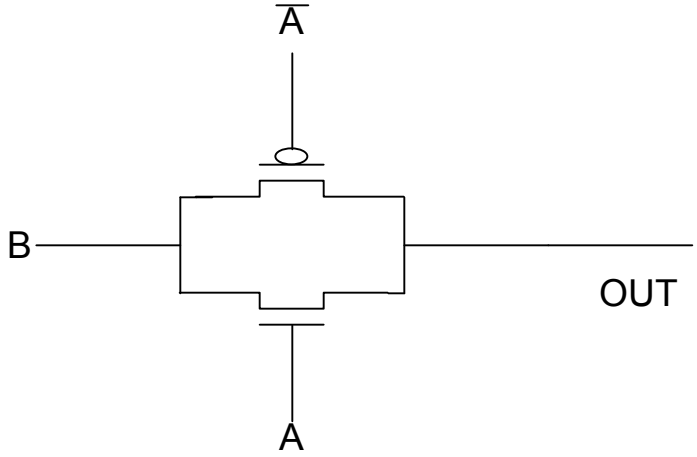
Pass-Transistor Logic

- Transmission Gate Based



A	B	OUT
0	0	Z
0	1	Z
1	0	0
1	1	1

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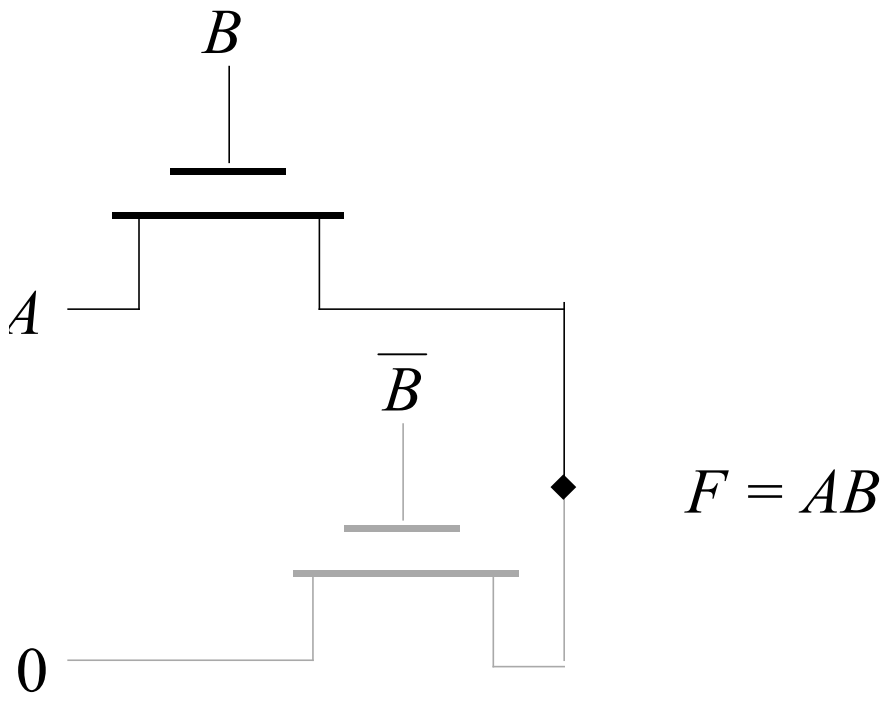
Example: AND Gate



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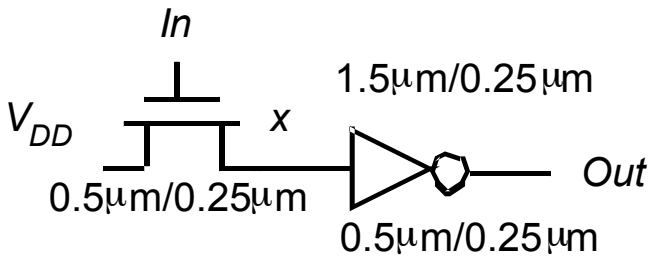
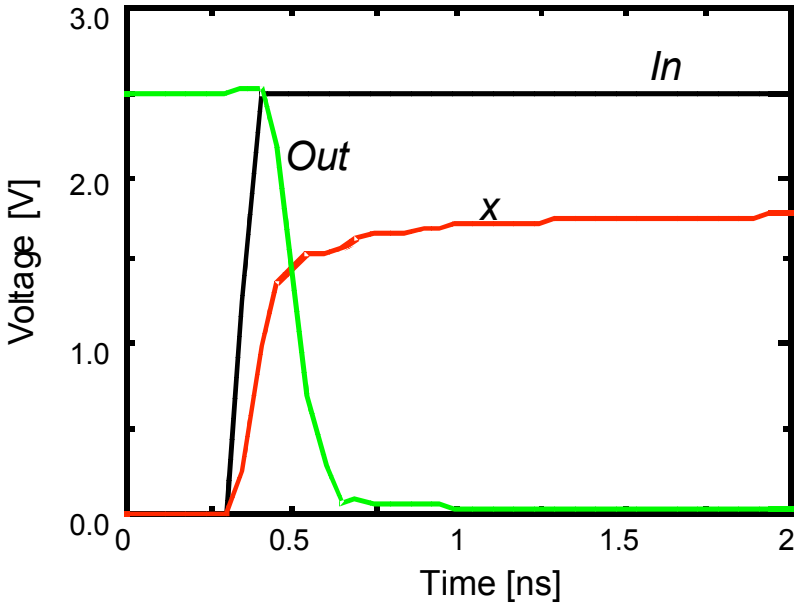
NMOS-Only Logic





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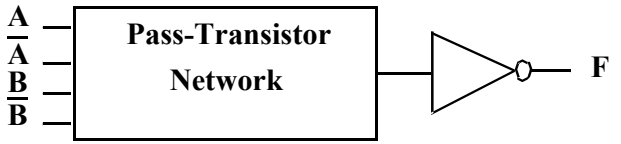
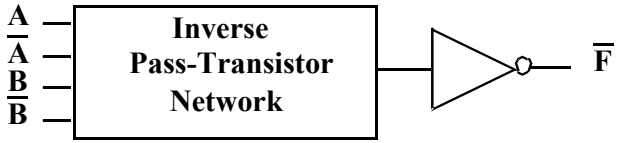
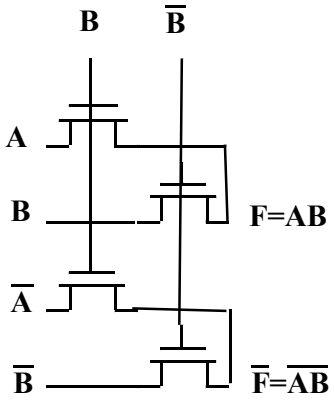
Complementary Pass Transistor Logic

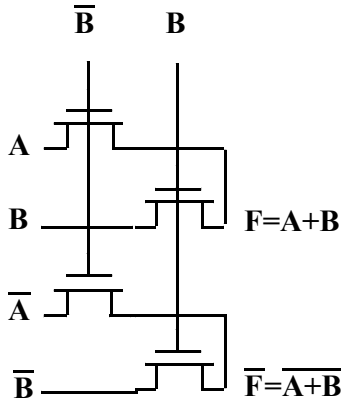


(a)

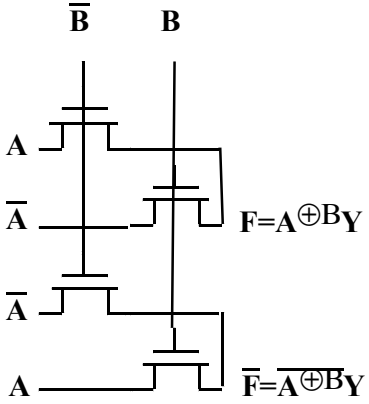




AND/NAND



OR/NOR



EXOR/NEXOR

(b)

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Resistance of Transmission Gate

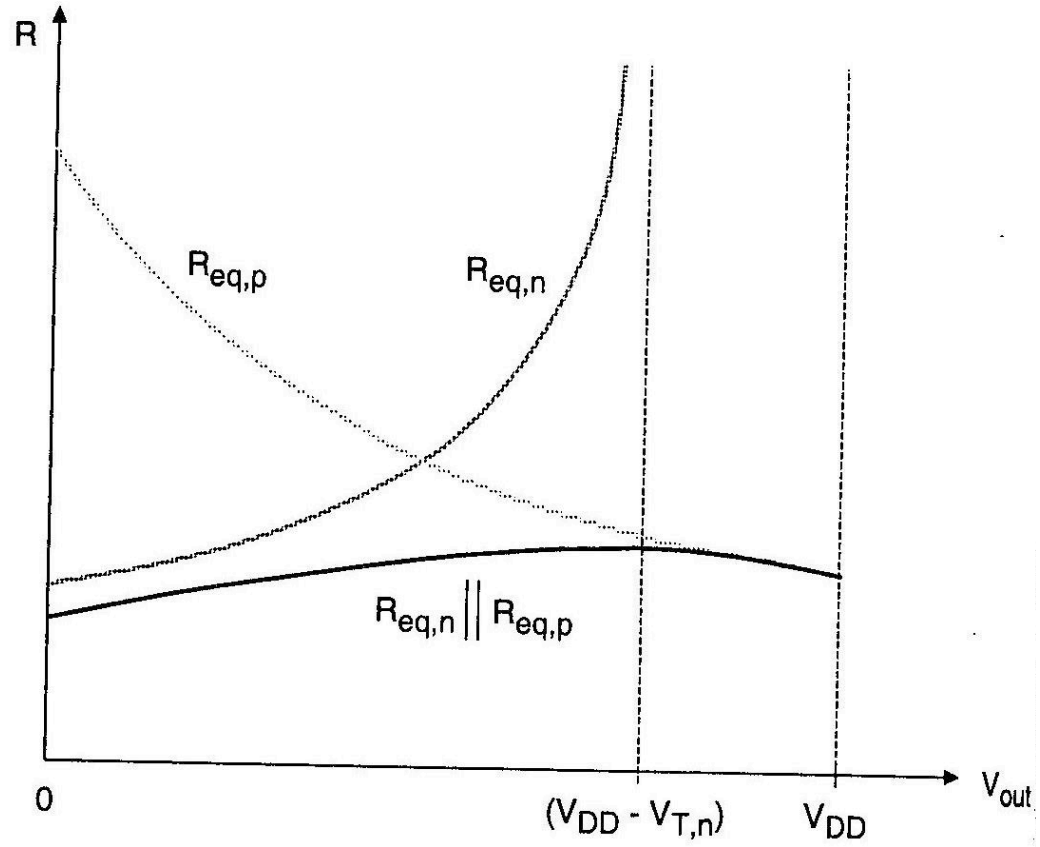

Fig. 7.35, “CMOS Digital Integrated Circuits”, Kang and Leblebici

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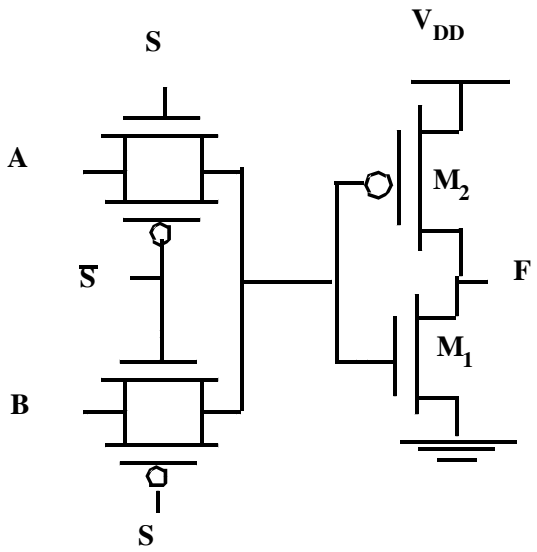
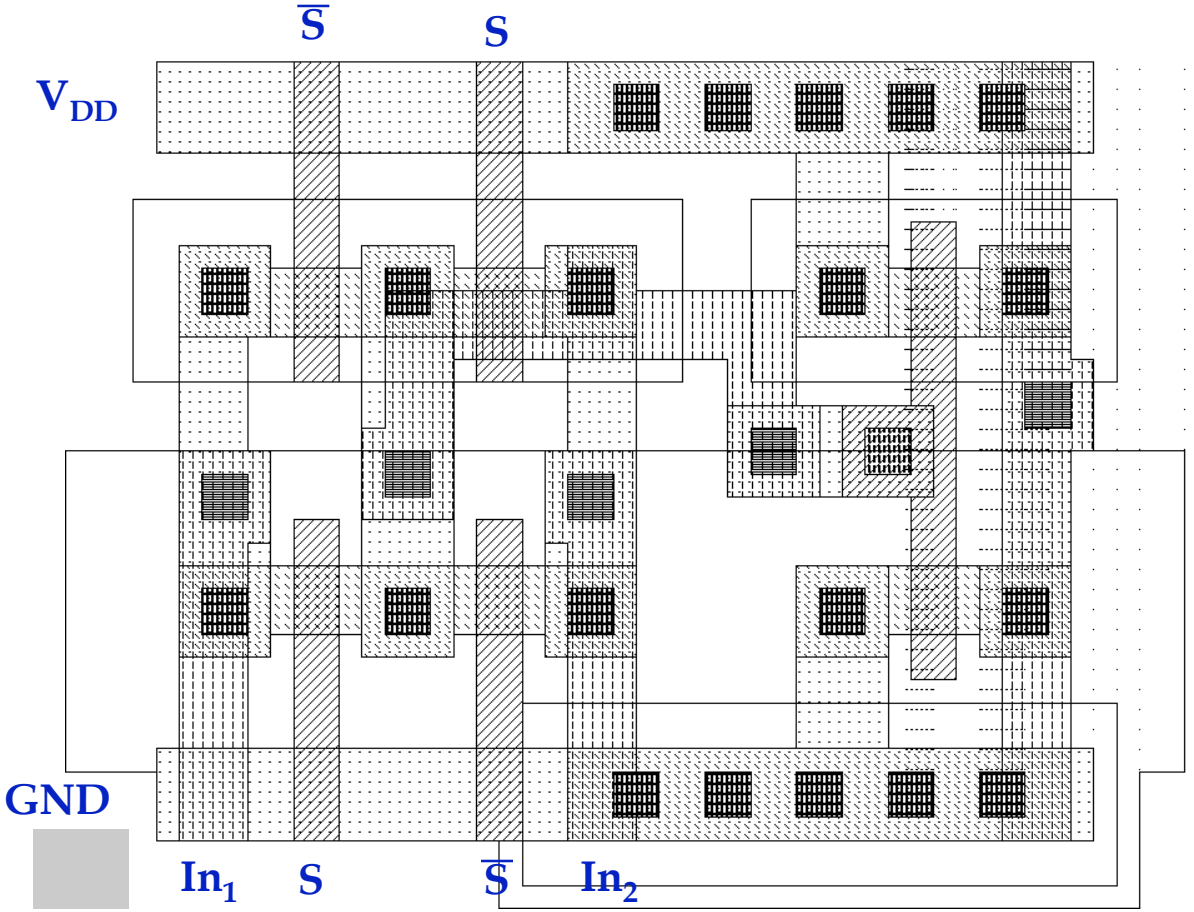
Pass-Transistor Based Multiplexer





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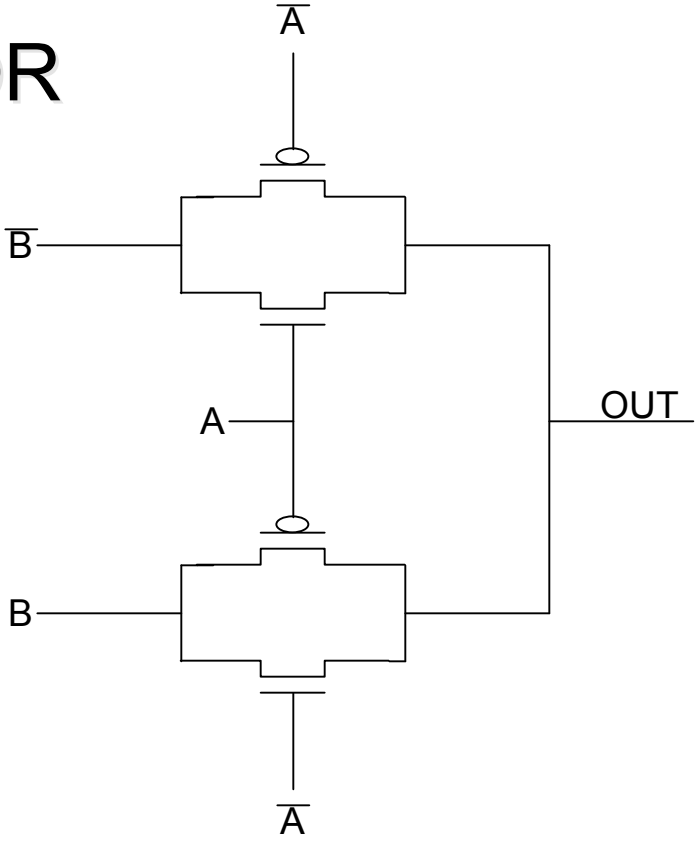
Pass-Transistor Logic

- XOR



A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

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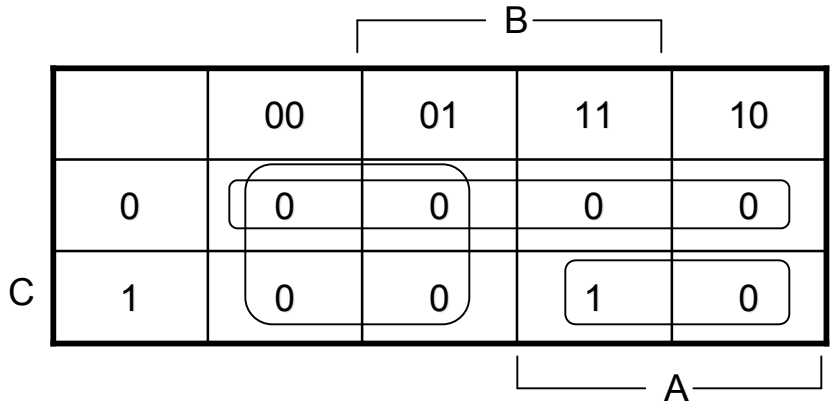
Pass-Transistor Logic

- Use Karnaugh Map



AND

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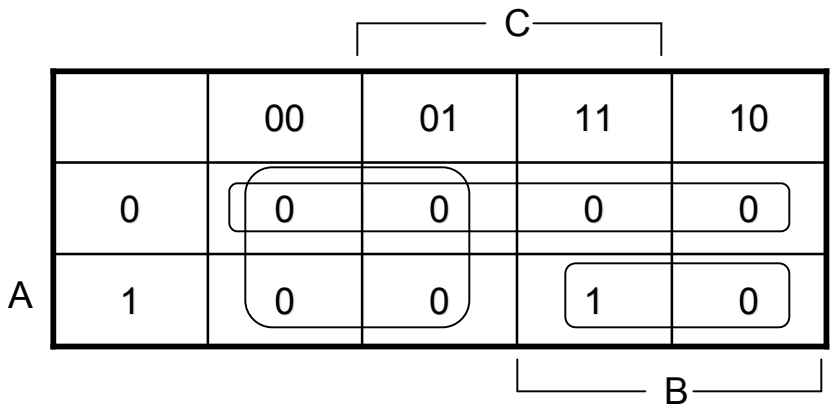
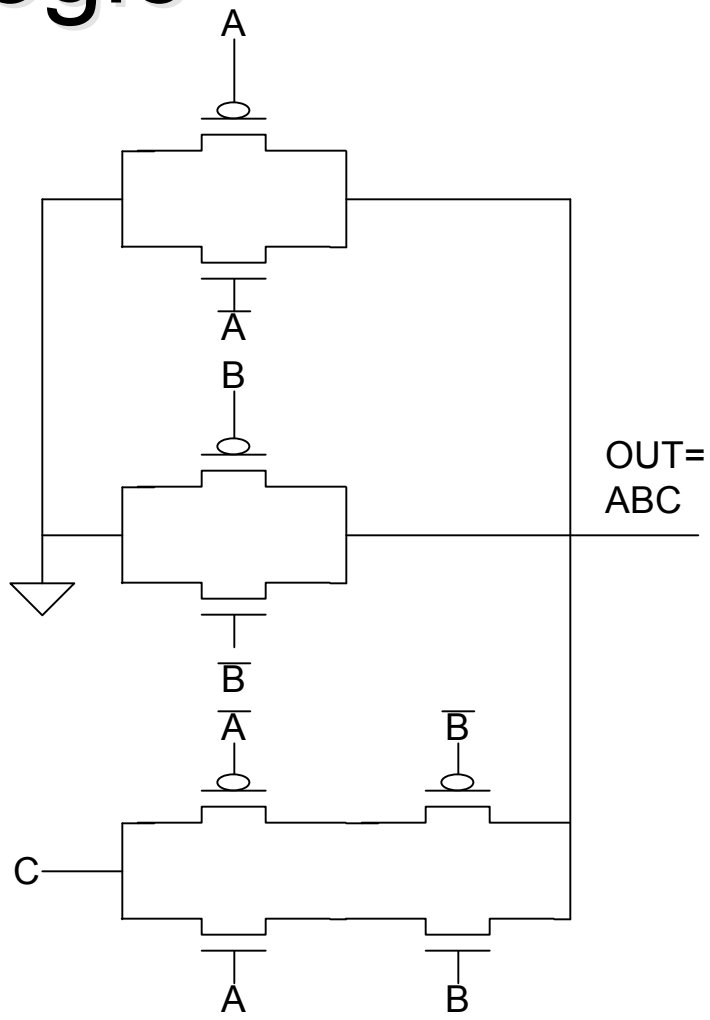
Pass-Transistor Logic





•12 transistors vs. 8 transistors

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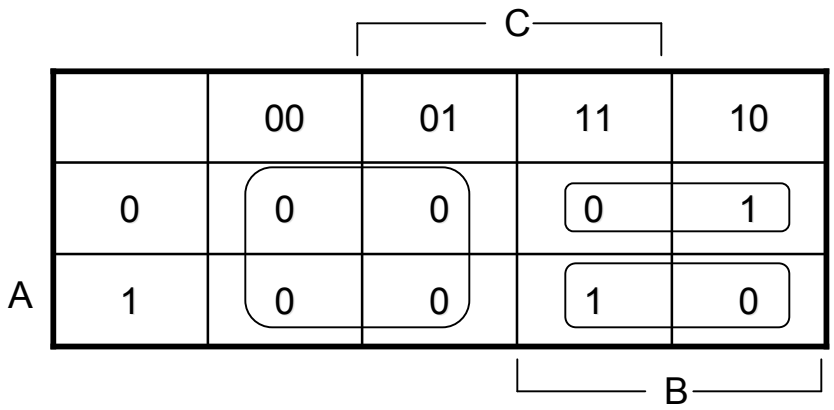
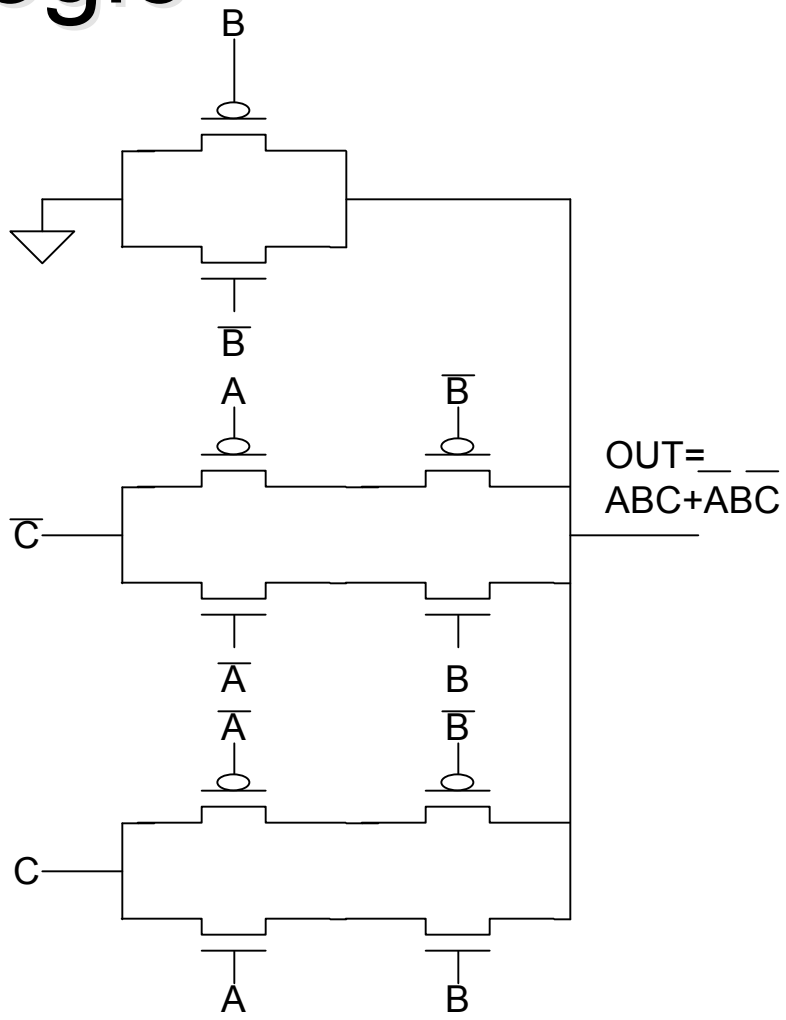
Pass-Transistor Logic





•16 transistors vs. 16 transistors

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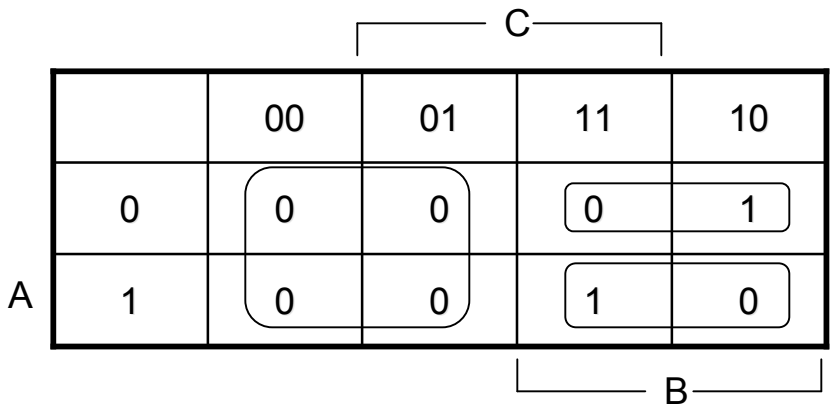
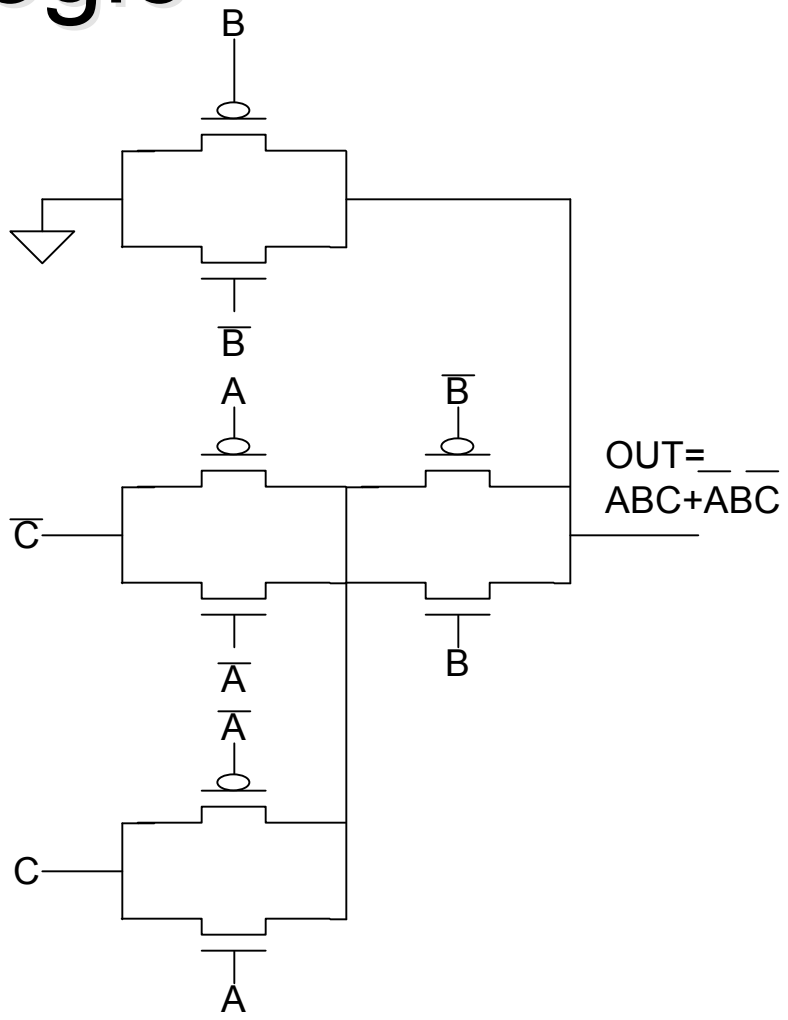
Pass-Transistor Logic





•14 transistors vs. 16 transistors

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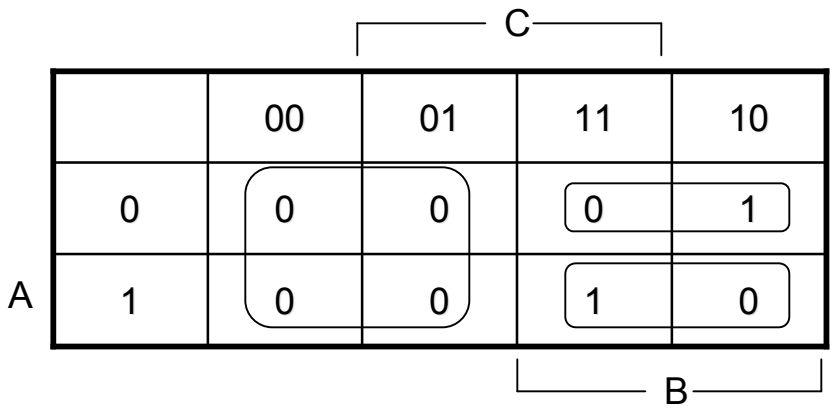
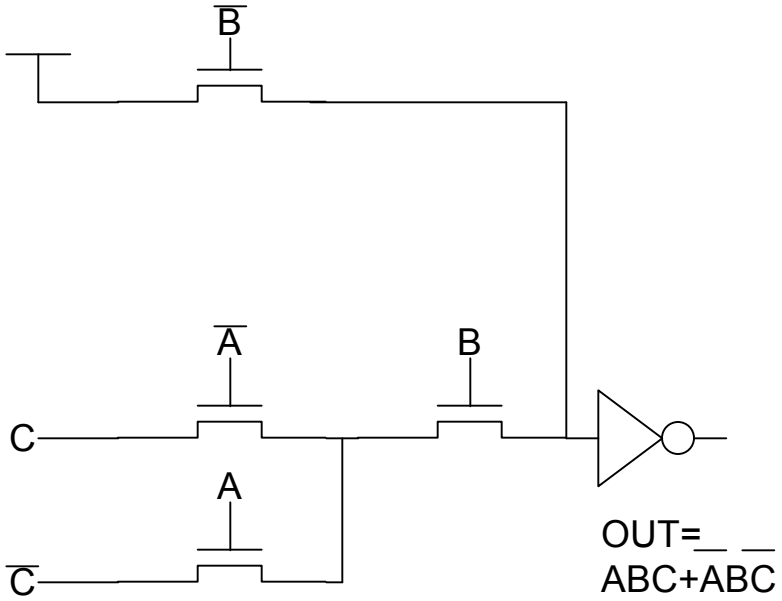
Pass-Transistor Logic





- 12 transistors vs. 16 transistors

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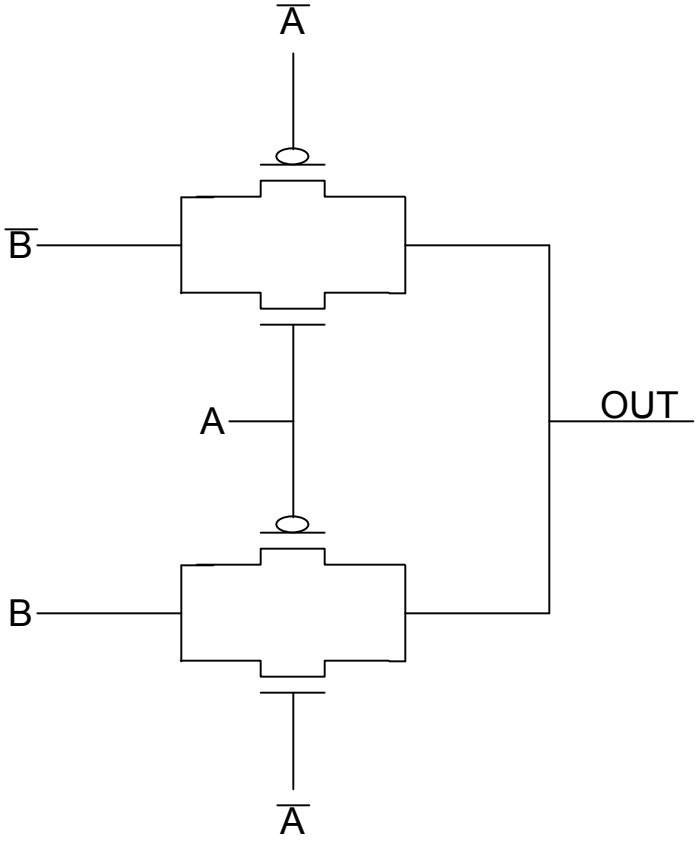
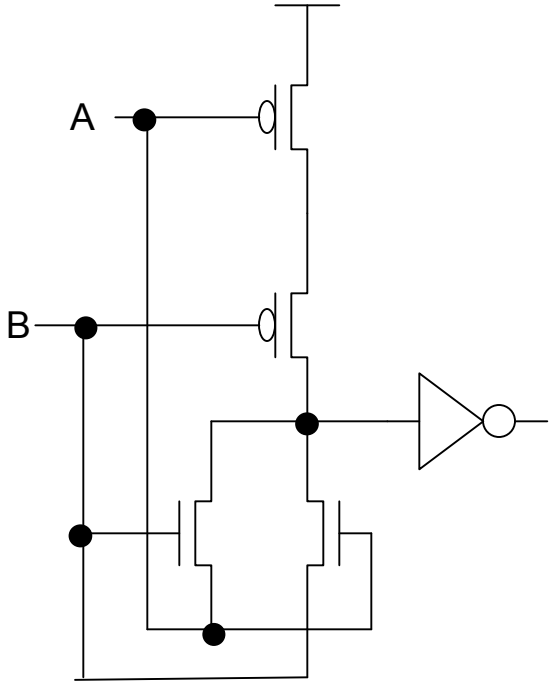
Pass-Transistor Logic





Cross Coupled XOR

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Pass-Transistor Logic

- In many cases, uses fewer transistors
- Can be difficult to design
- Usually requires complemented versions of all signals
- Difficult to layout
- Delay analysis is not as well defined in terms of sizing choices

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Pass-Transistor Logic

- Delay characteristics
  - nMOS-only pass logic has fast fall times
  - Complementary designs have faster rise times, but increasing the pMOS width to decrease the rise time will increase the fall time
  - Transmission gate looks like a RC line

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Next Class

- Sequential Design
- Memory and Control
- Chapter 7
- Have a great Spring Break!

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