Topics

- Dynamic CMOS
- Sequential Design
- Memory and Control

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Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of n requires $2n$ (n N-type + n P-type) devices

- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires only $n+2$ ($n+1$ N-type + 1 P-type) transistors

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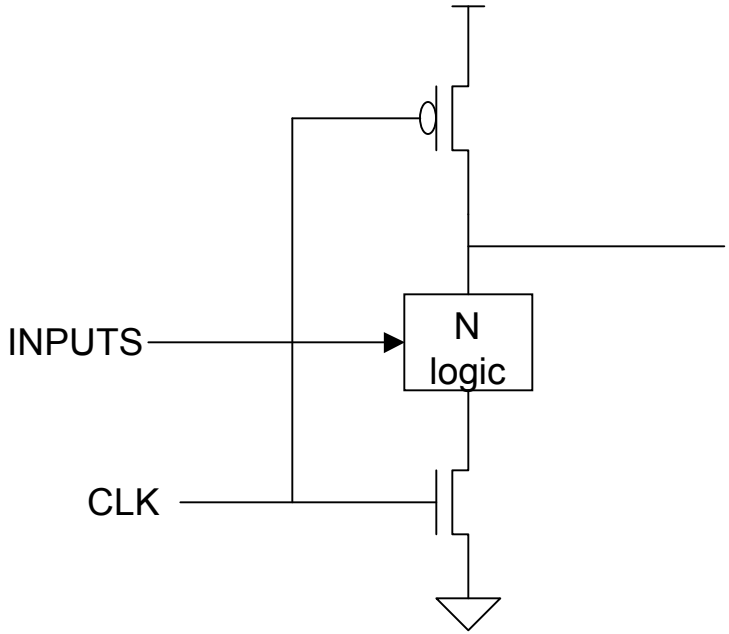
Dynamic CMOS

- nMOS logic structure with precharged pullup



- Precharge to VDD when clock is low
- Evaluate when clock is high

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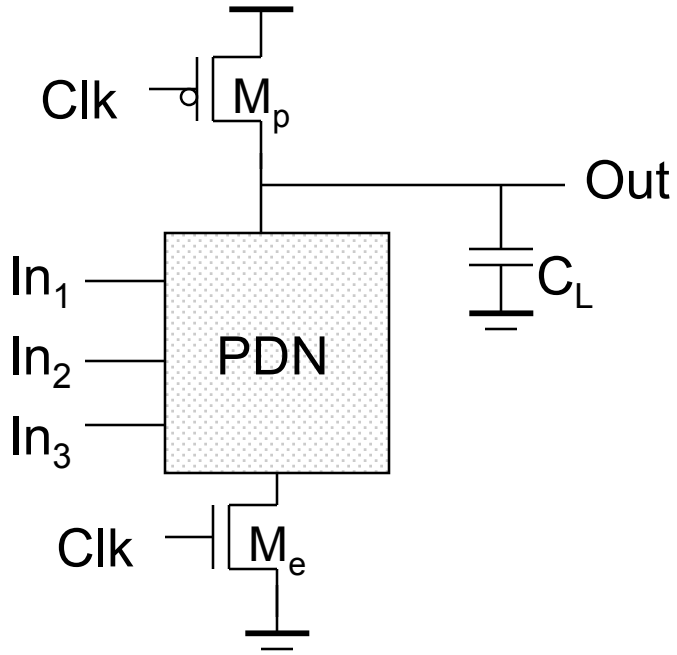
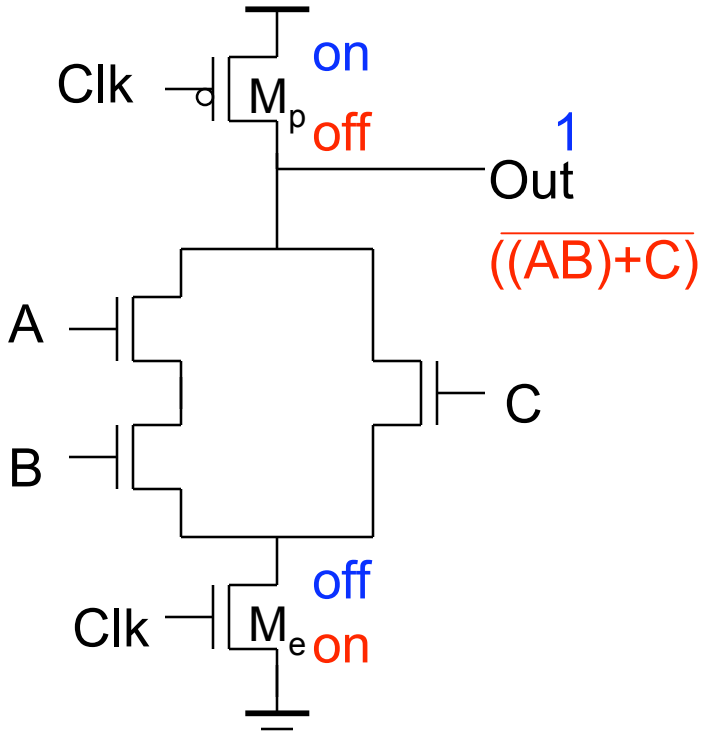
Dynamic Gate





Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

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Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

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Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (Cout)
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

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Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
- Needs a precharge/evaluate clock

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Dynamic CMOS

- Advantages
  - Fewer transistors than CMOS - on the same order as pseudo-nMOS
  - Smaller load capacitances - faster speed
- Disadvantages
  - Inputs must be stable during evaluate phase
  - Can not be cascaded
  - Charge sharing

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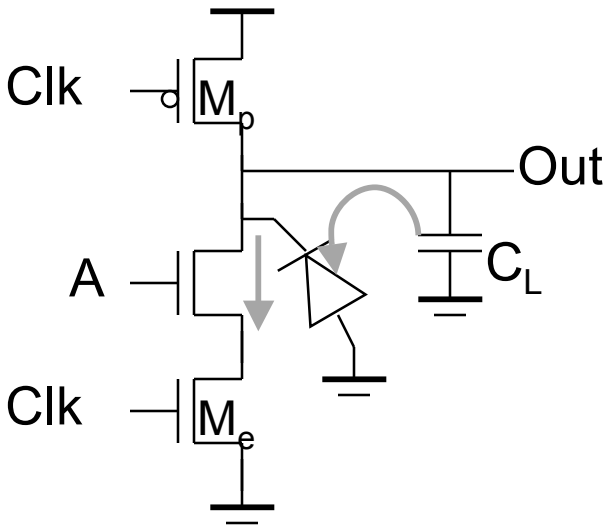
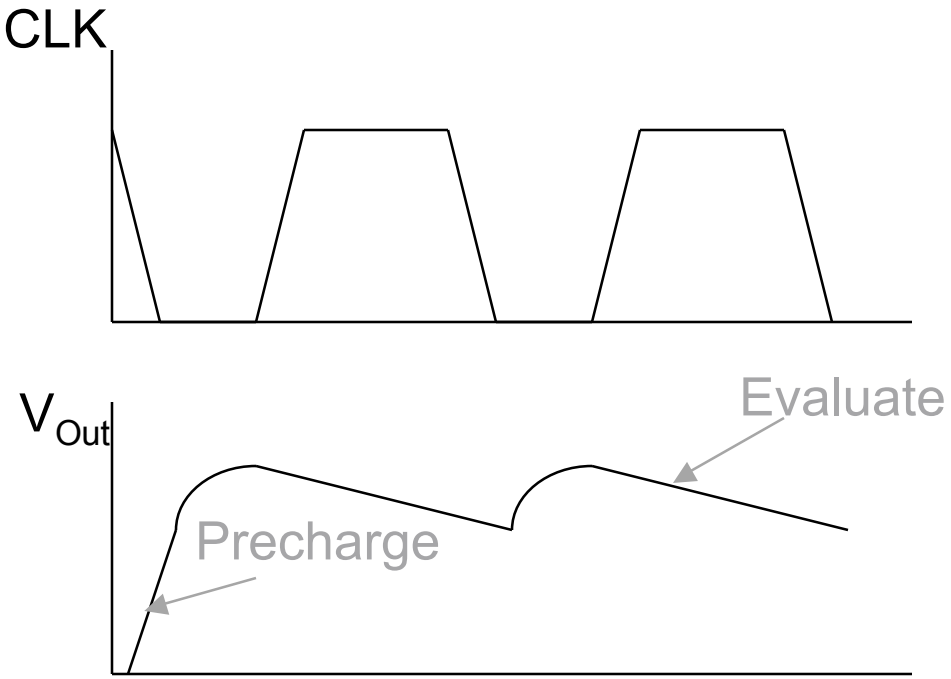
Issues in Dynamic Design 1: Charge Leakage



Leakage sources



Dominant component is subthreshold current

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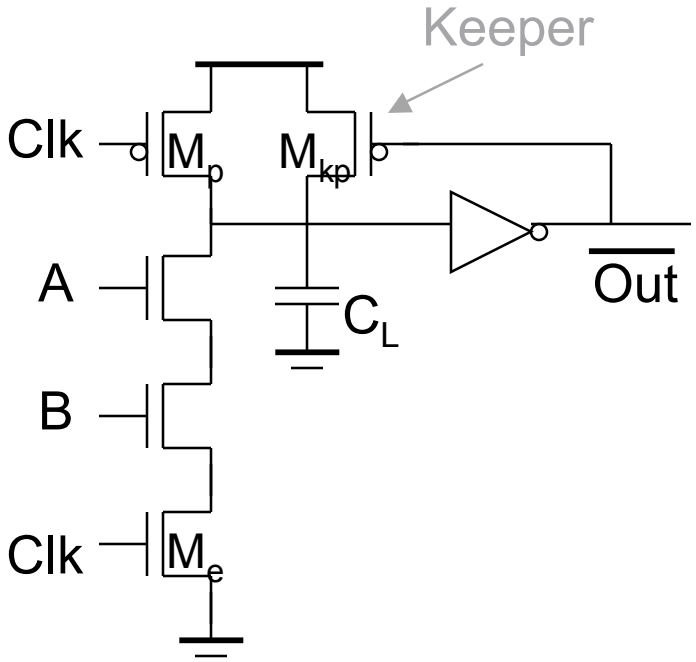
Solution to Charge Leakage



- Same approach as level restorer for pass-transistor logic
- Increase size of inverter to increase capacitance

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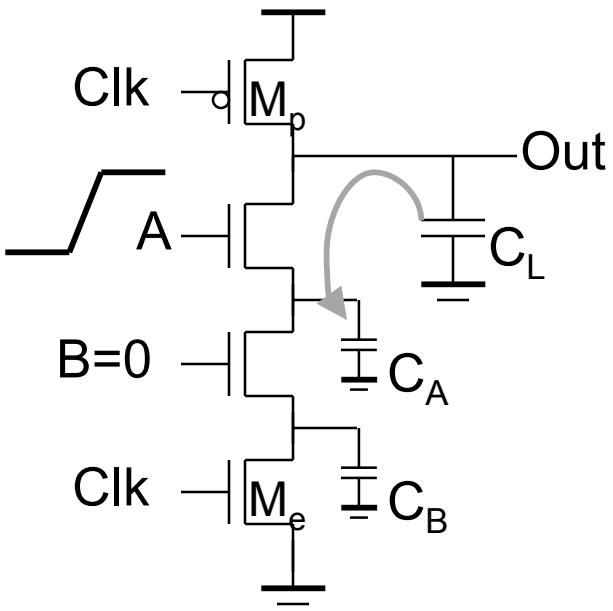
Issues in Dynamic Design 2: Charge Sharing



Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

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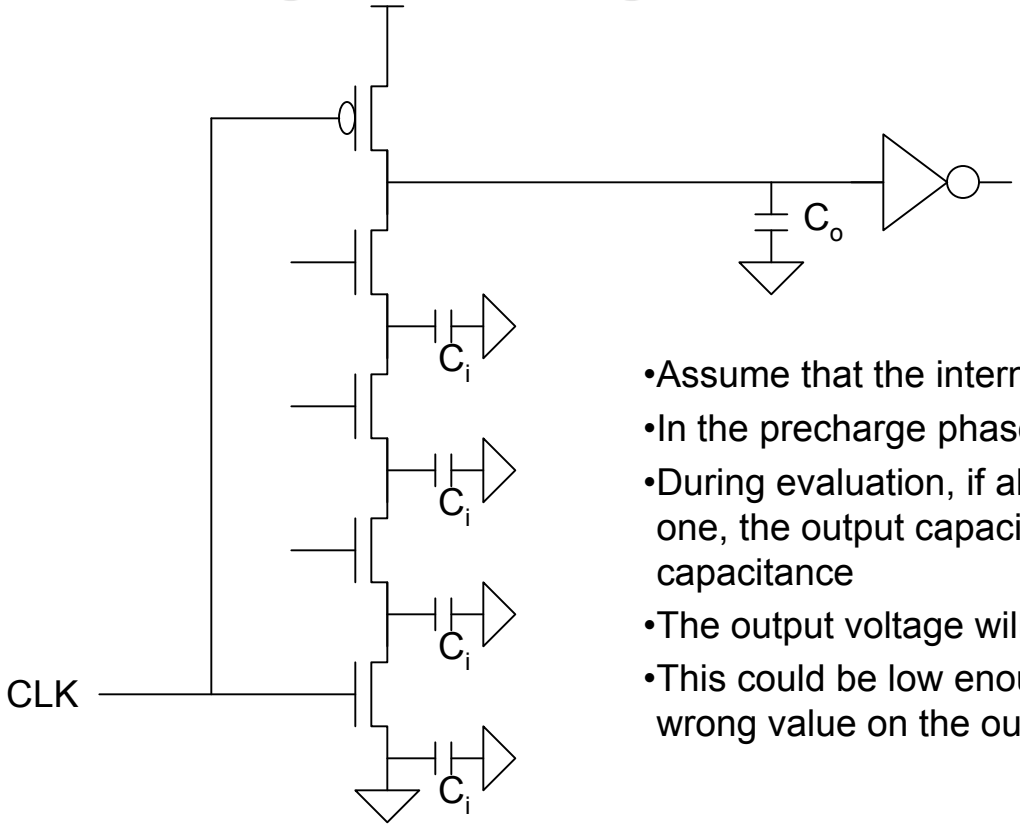
Dynamic CMOS

- Charge Sharing



- Assume that the internal capacitances have been discharged
- In the precharge phase, the output capacitance gets charged
- During evaluation, if all the inputs are high except the bottom one, the output capacitance gets distributed to the internal capacitance
- The output voltage will drop to $V_{DD}\frac{C_o}{C_o + 2C_i}$
- This could be low enough to trigger the inverter, causing a wrong value on the output

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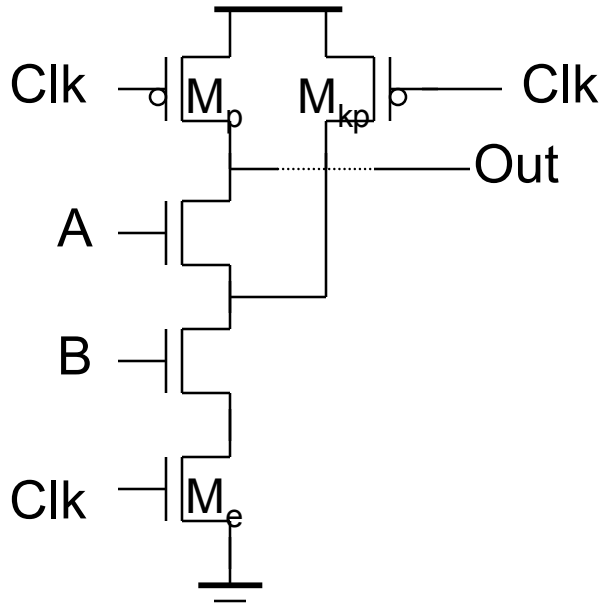
Solution to Charge Redistribution



Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

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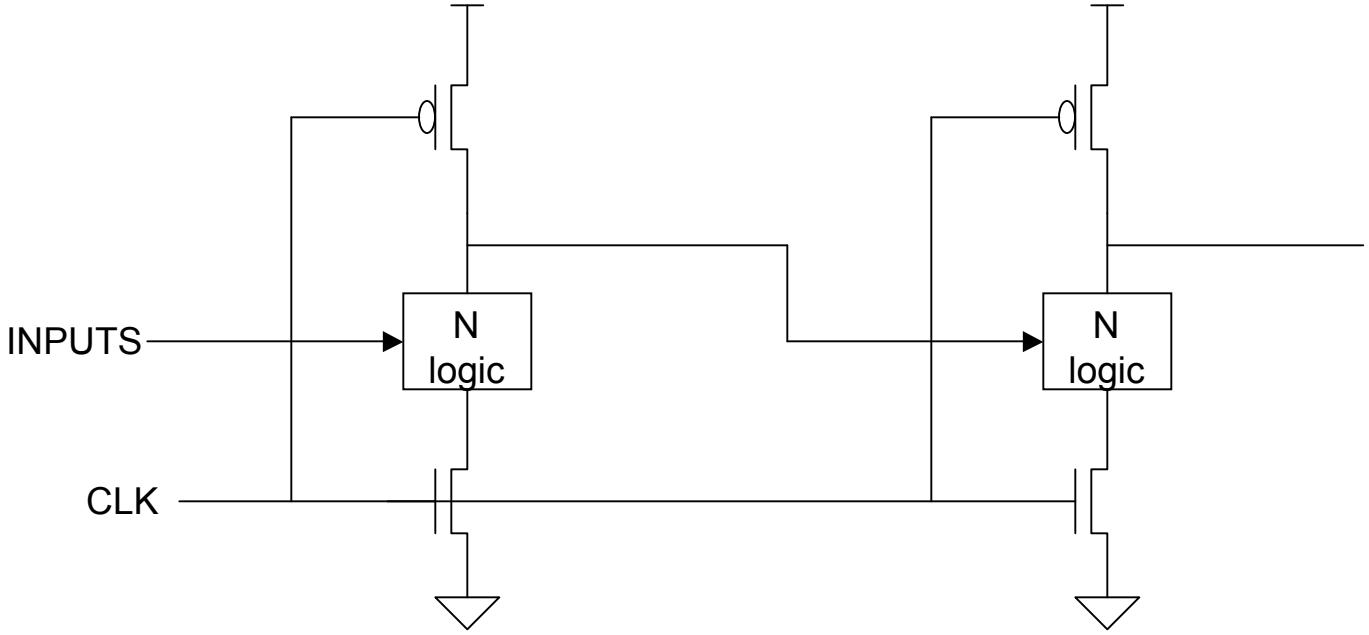
Dynamic CMOS

- Cascade problem



Since the evaluation from the first stage takes some time, the second stage will start evaluating with the precharged input rather than the evaluated input

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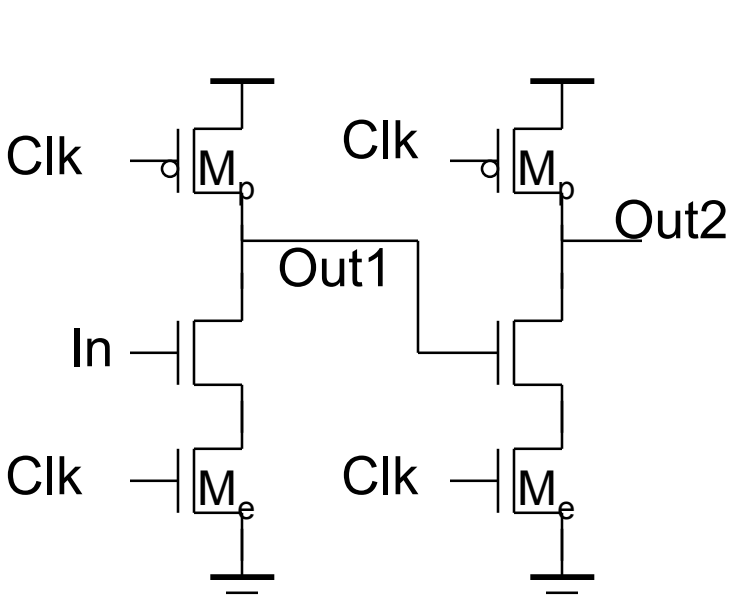
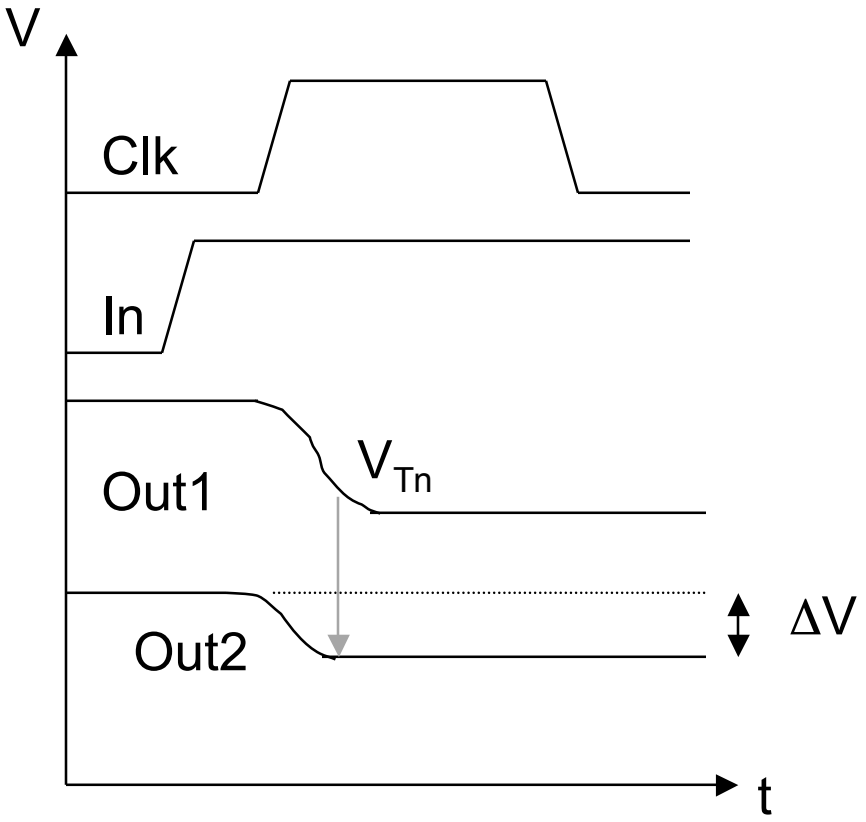
Cascading Dynamic Gates





Only 0 → 1 transitions allowed at inputs!

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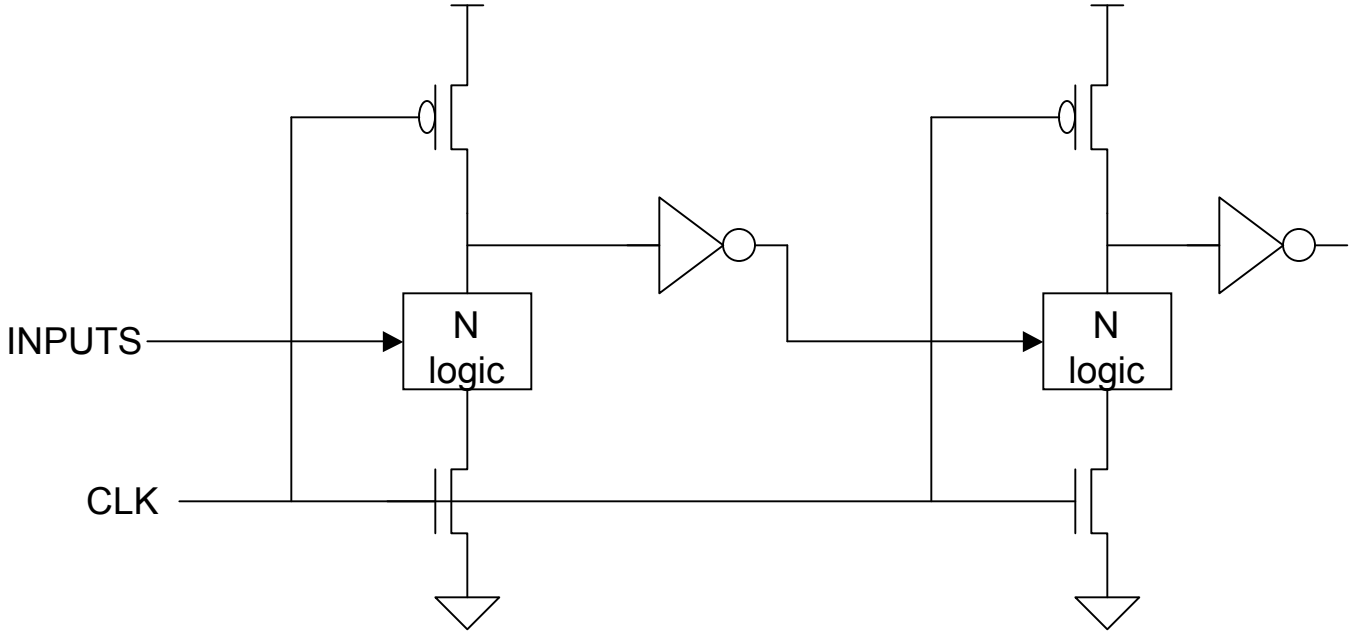
Domino Logic

- Solves cascade problem



Since the precharged output from the first stage is 0, it will never activate the pulldown network in the second stage until the first stage evaluation has completed.

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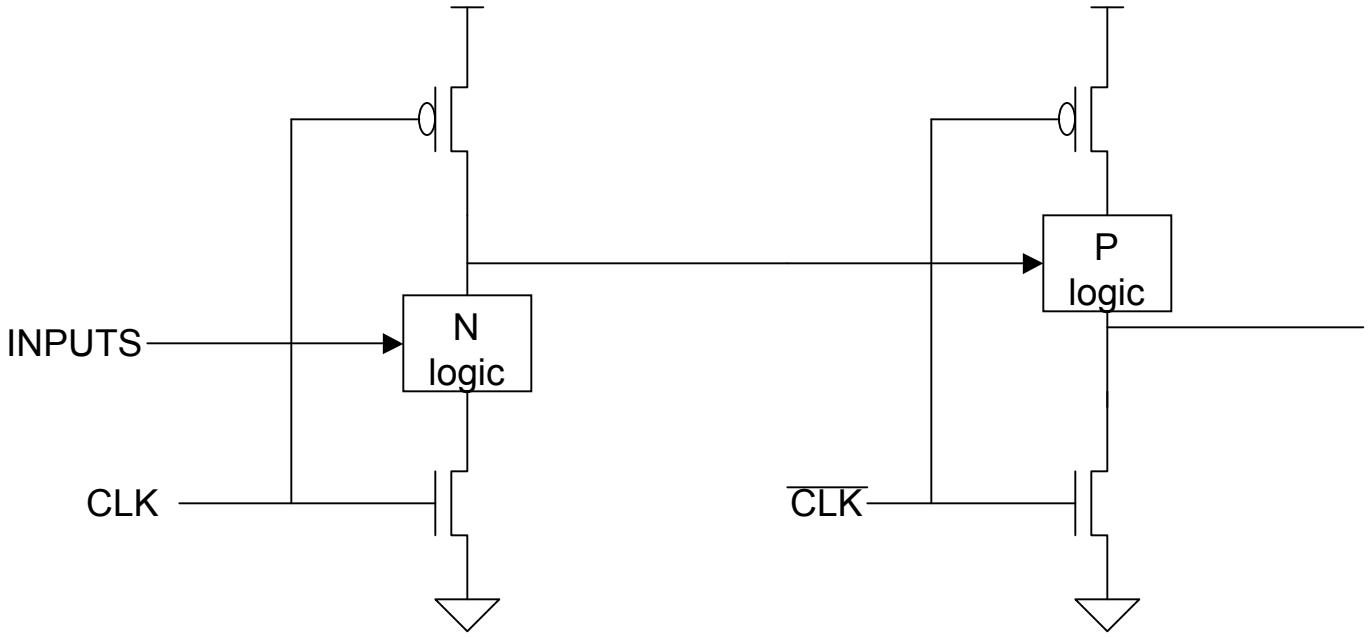
NP Domino (Zipper) CMOS



Since the second stage is build from p-logic, the precharged output from the first stage will not activate the inputs of the second stage

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Sequential Logic

- In our text:
  - a latch is level sensitive
  - a register is edge-triggered
  - a flip-flop is bistable
- There are many different naming conventions
  - For instance, many books call edge-triggered registers flip-flops as well

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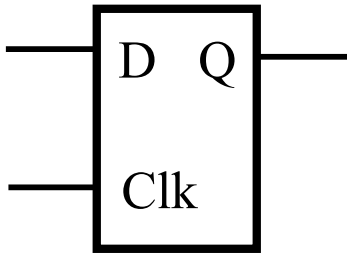
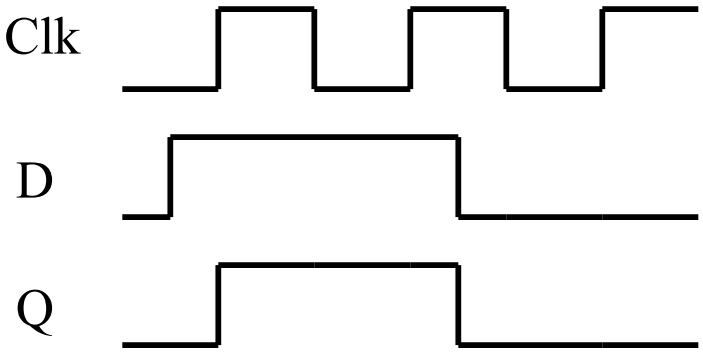
Latch versus Register

- Latch

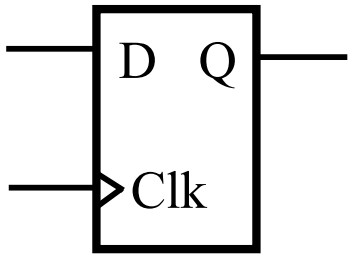
  stores data when clock is low

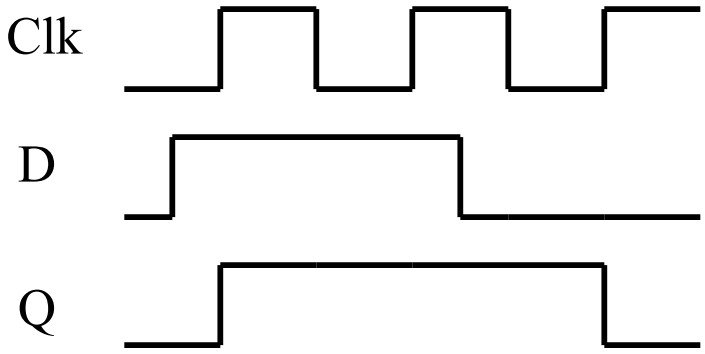




- Register

  stores data when clock rises





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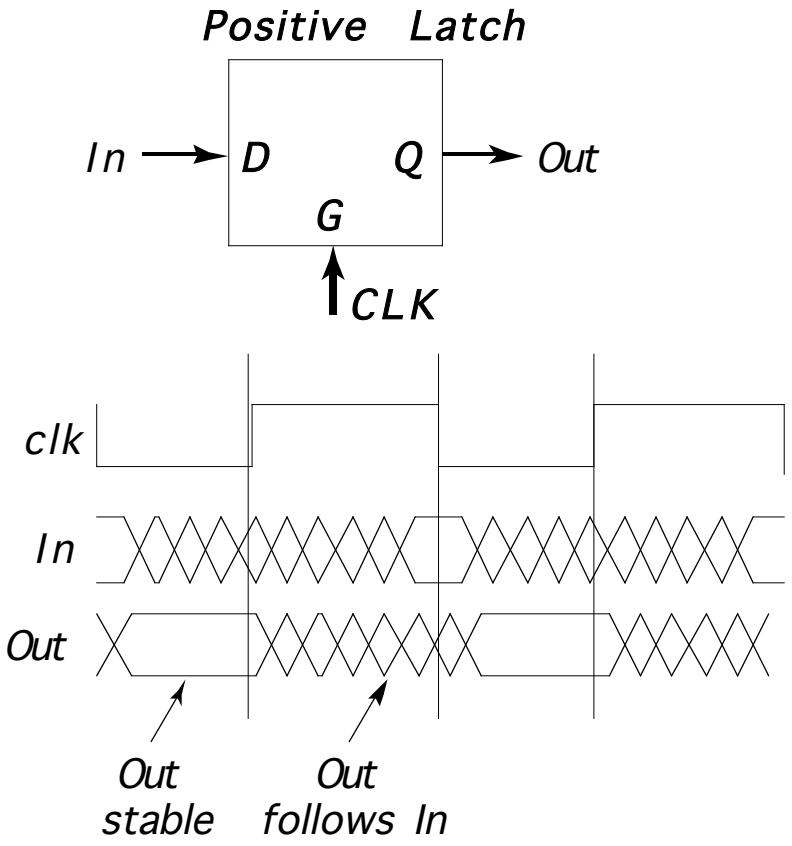
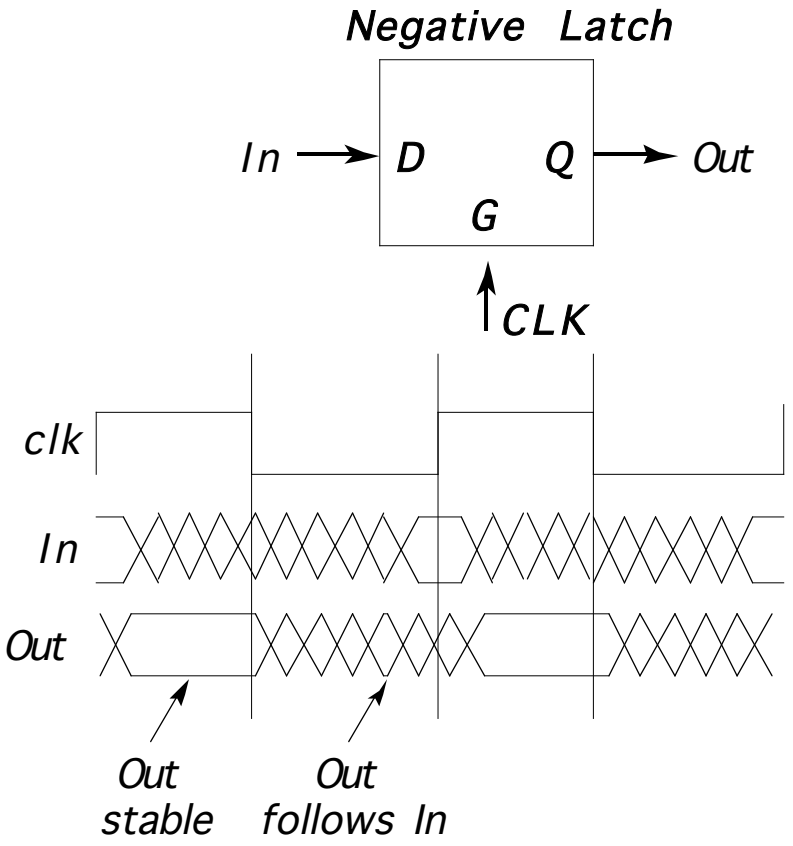
Latches





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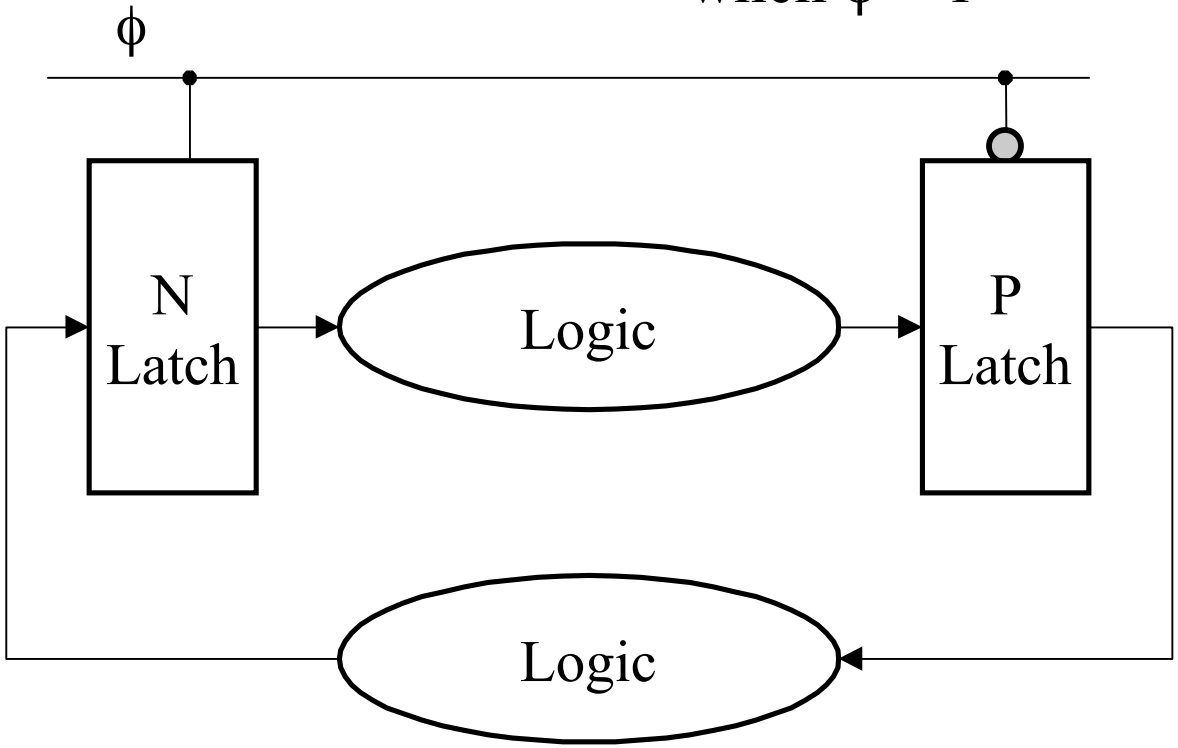
Latch-Based Design

• N latch is transparent when $\phi = 0$

• P latch is transparent when $\phi = 1$



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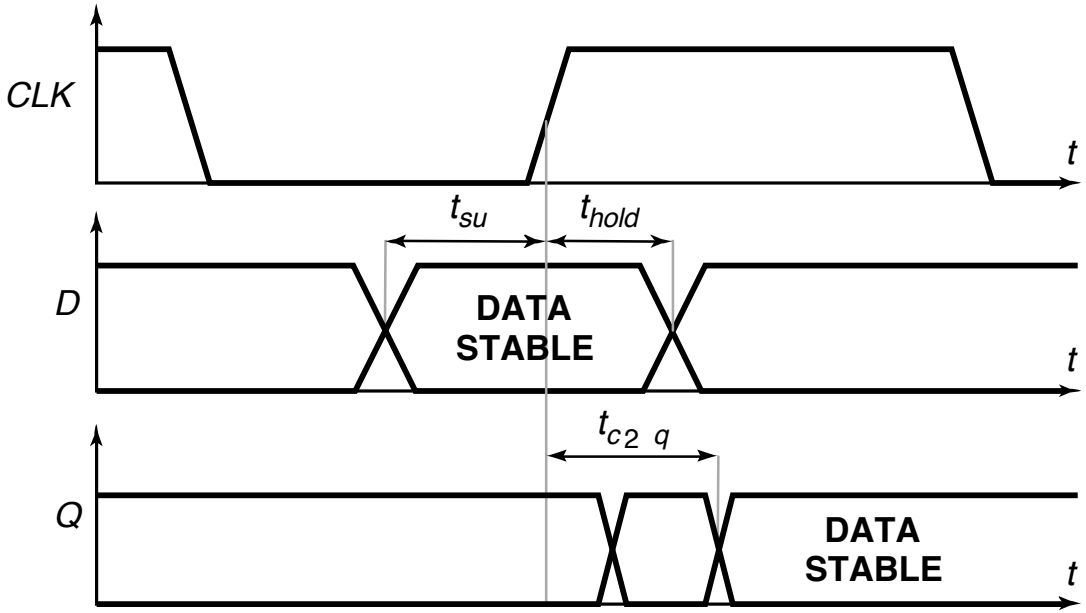
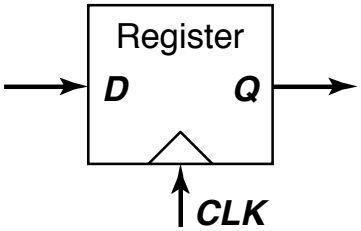
Timing Definitions





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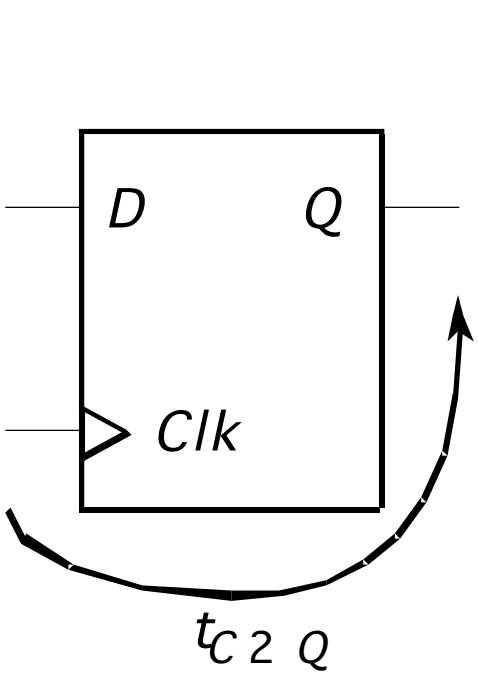
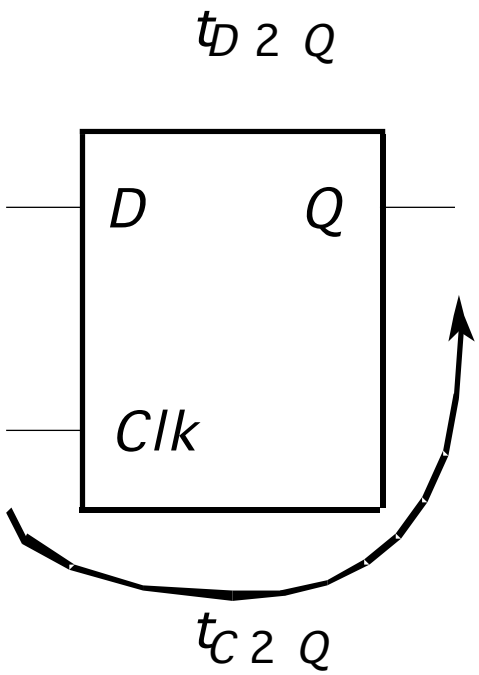
Characterizing Timing



Register



Latch

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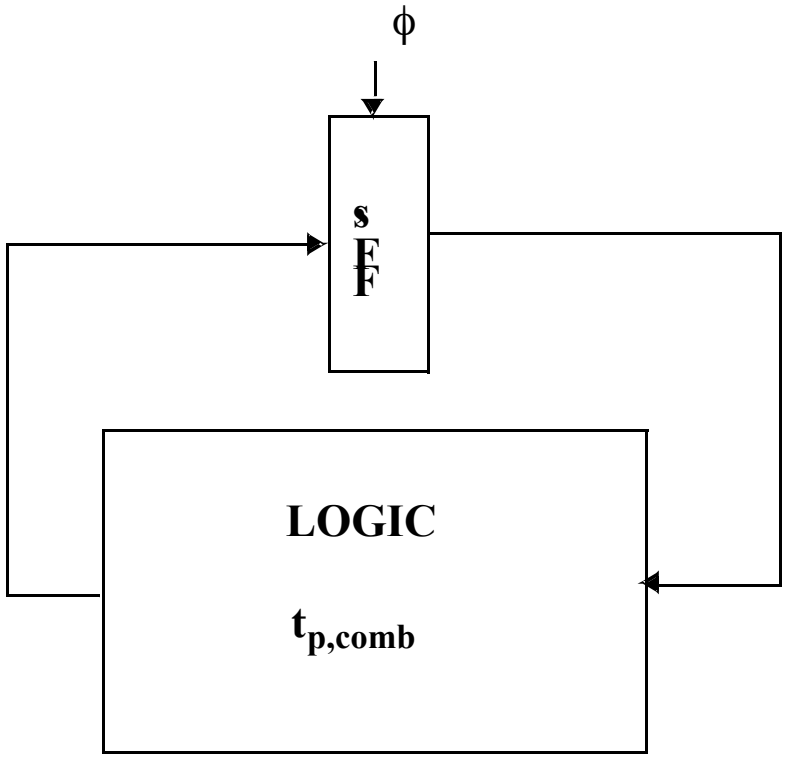
Maximum Clock Frequency



$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$

Also:

$t_{cdreg} + t_{cdlogic} > t_{hold}$

t_{cd}: contamination delay = minimum delay

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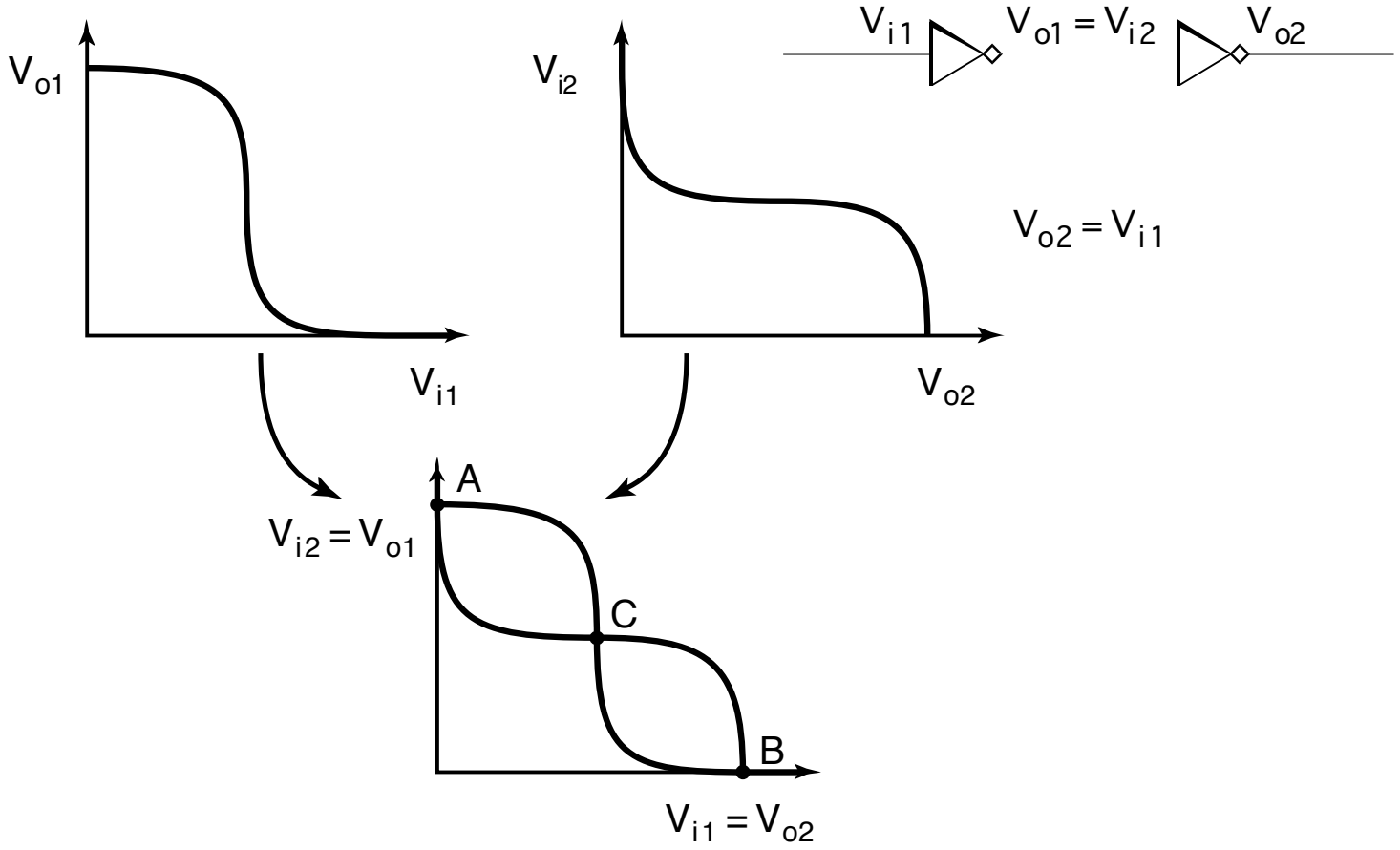
Positive Feedback: Bi-Stability



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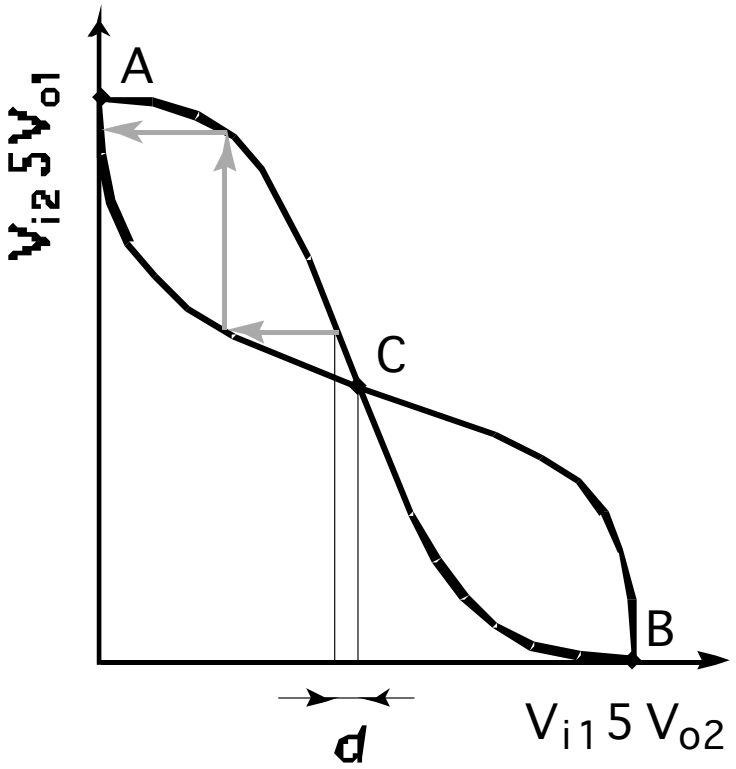
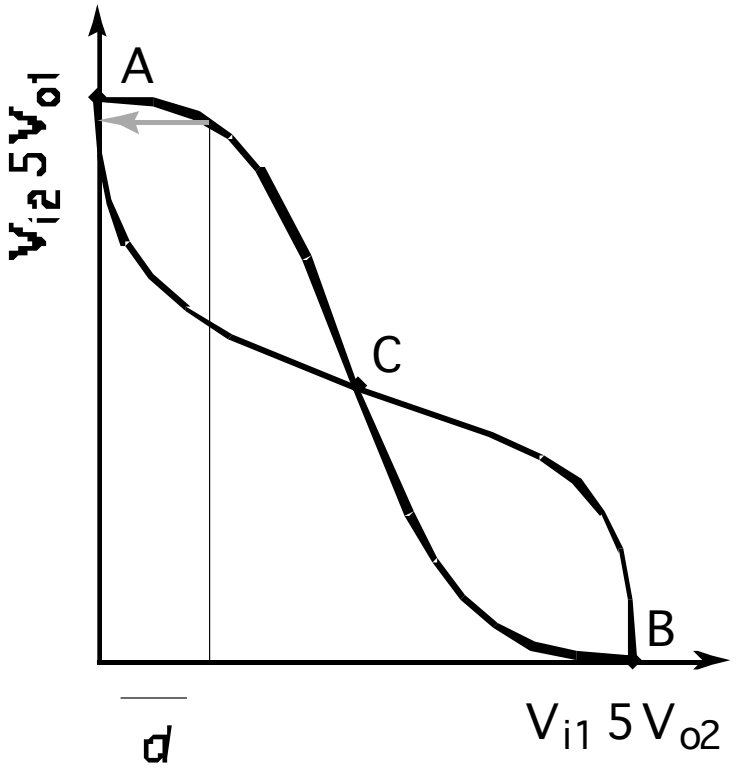
Meta-Stability





Gain should be larger than 1 in the transition region

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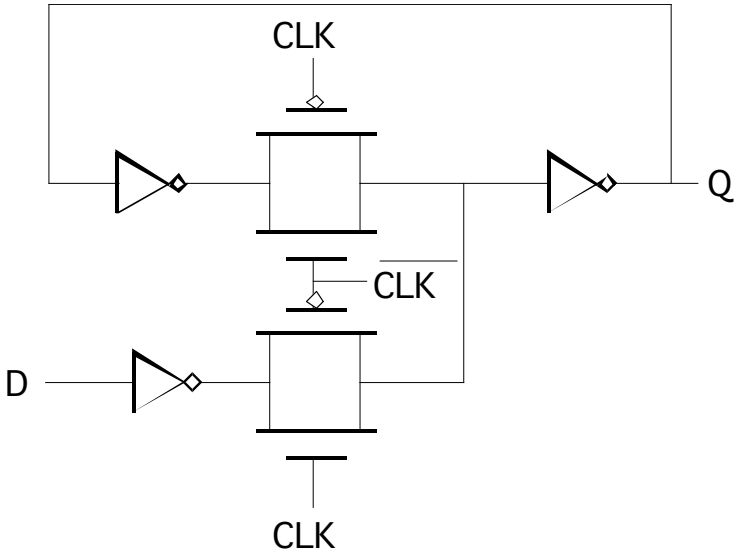
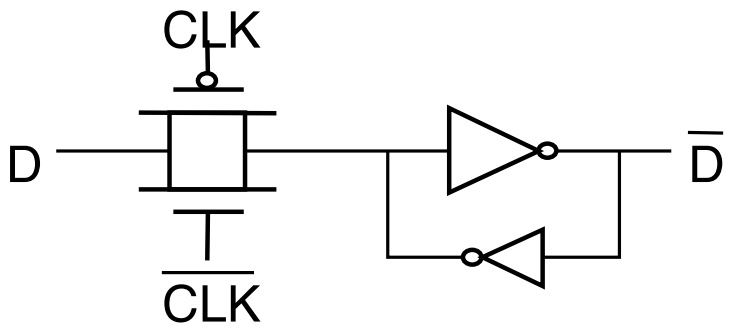
Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states



Converting into a MUX



Forcing the state
(can implement as NMOS-only)

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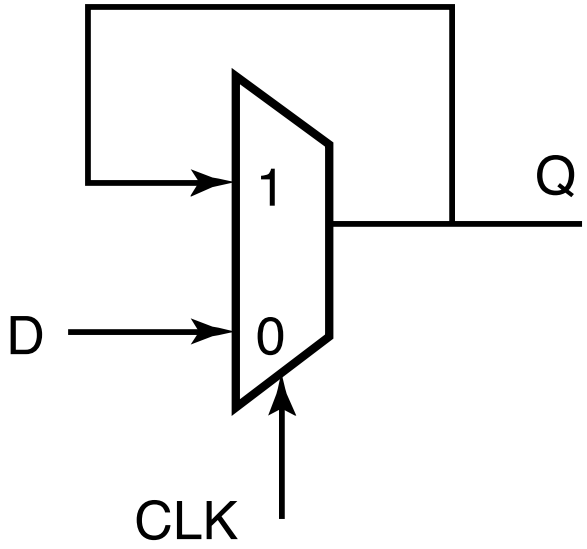
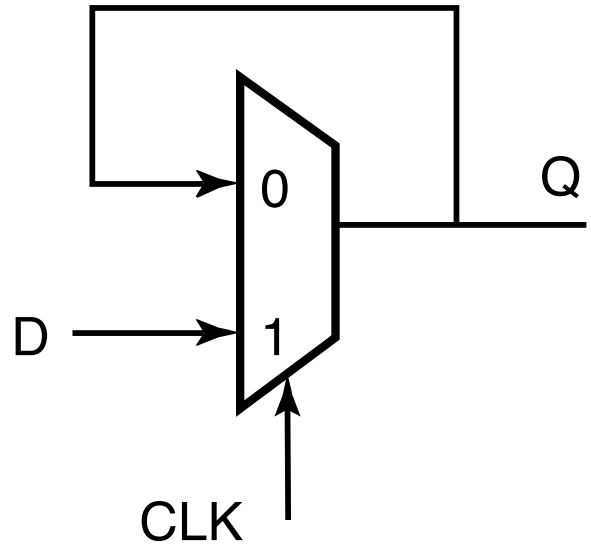
Mux-Based Latches

Negative latch
(transparent when CLK= 0)



$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Positive latch
(transparent when CLK= 1)



$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

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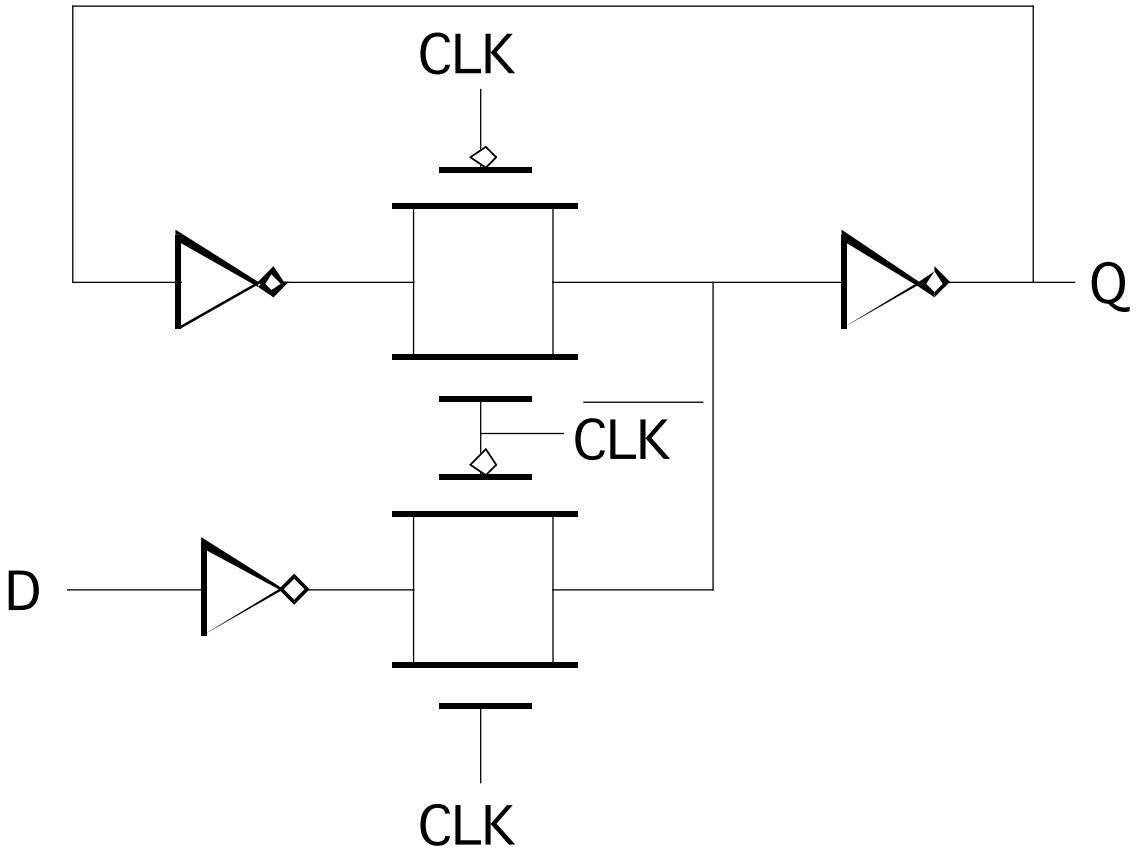
Mux-Based Latch



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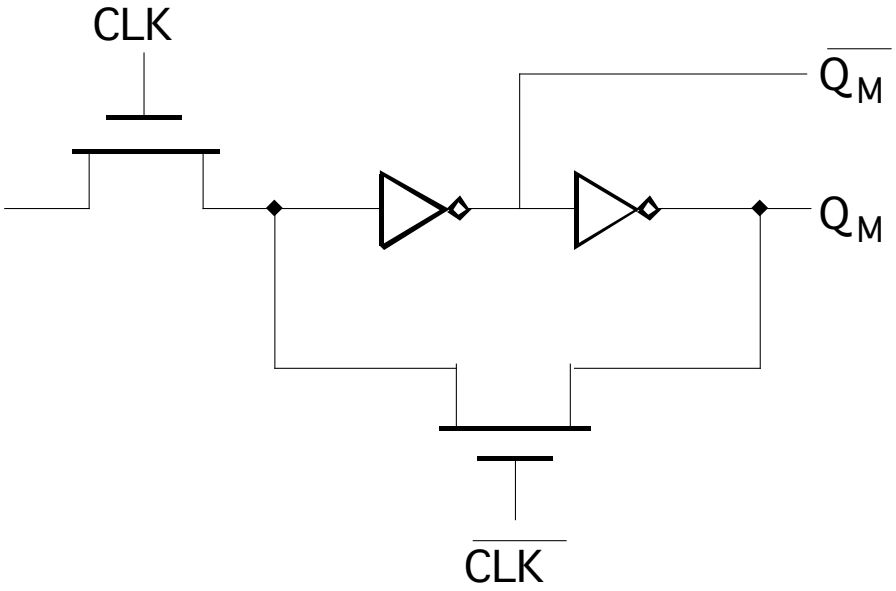
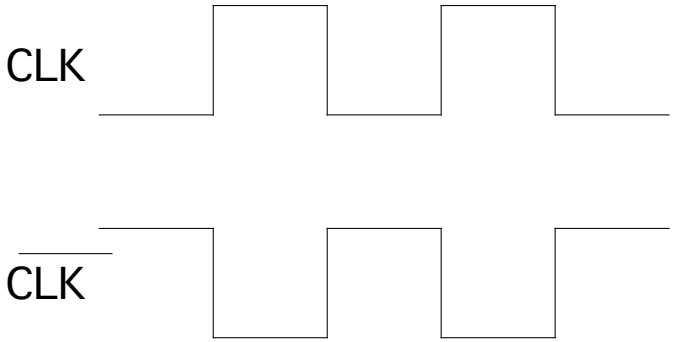
Mux-Based Latch



NMOS only



Non-overlapping clocks

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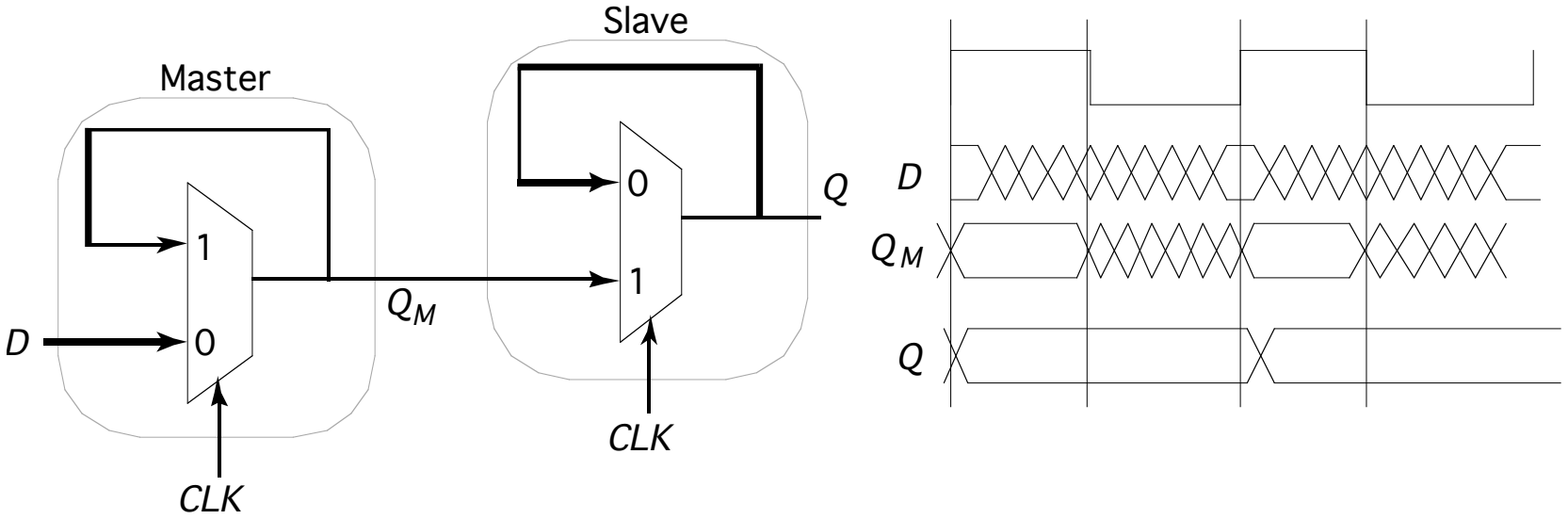
Master-Slave (Edge-Triggered) Register



Two opposite latches trigger on edge
Also called master-slave latch pair

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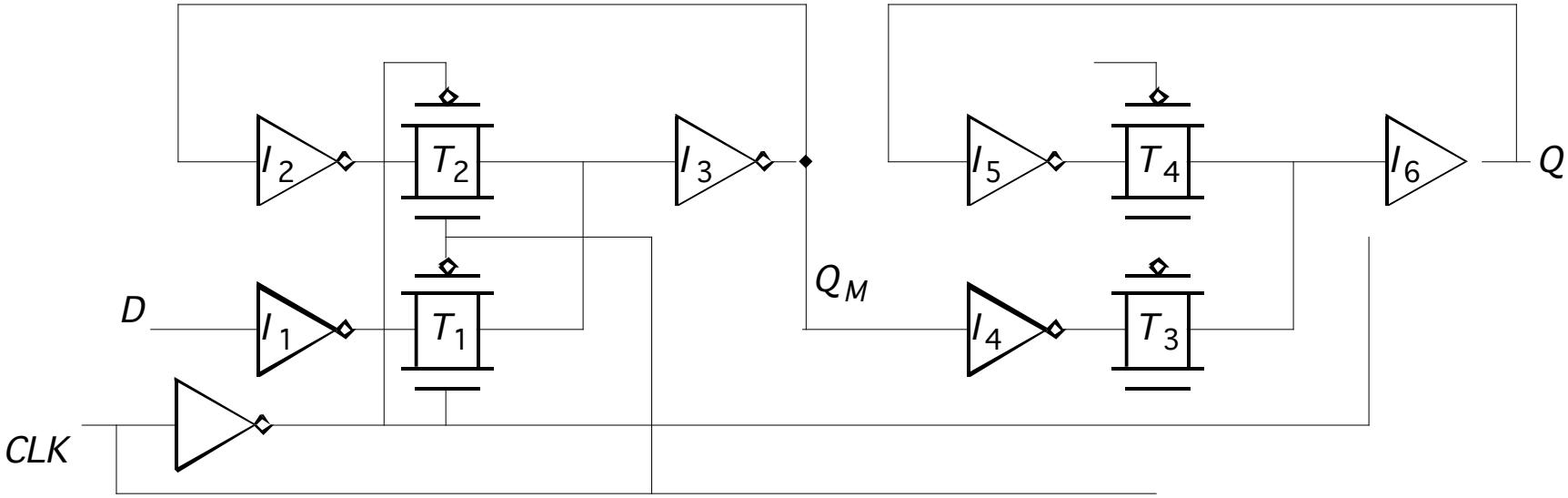
Master-Slave Register

Multiplexer-based latch pair



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Semiconductor Memory Classification

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

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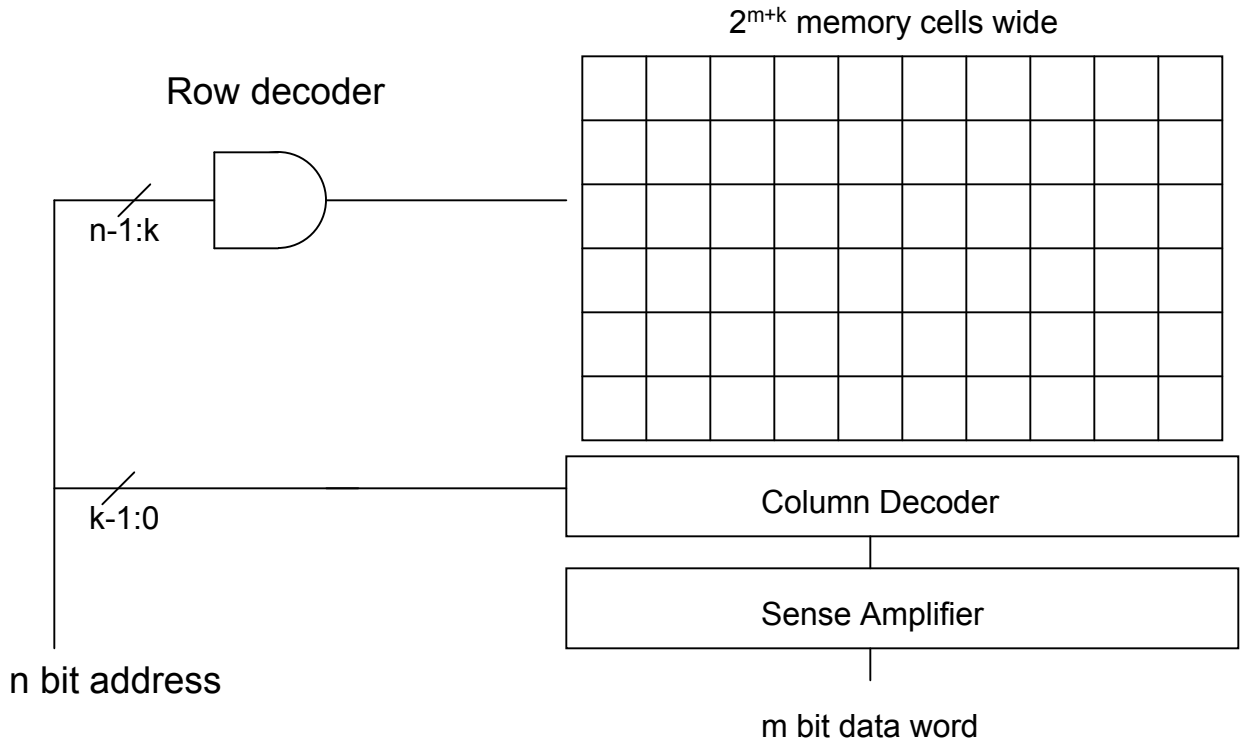
Memory Design

- Random Access Memory



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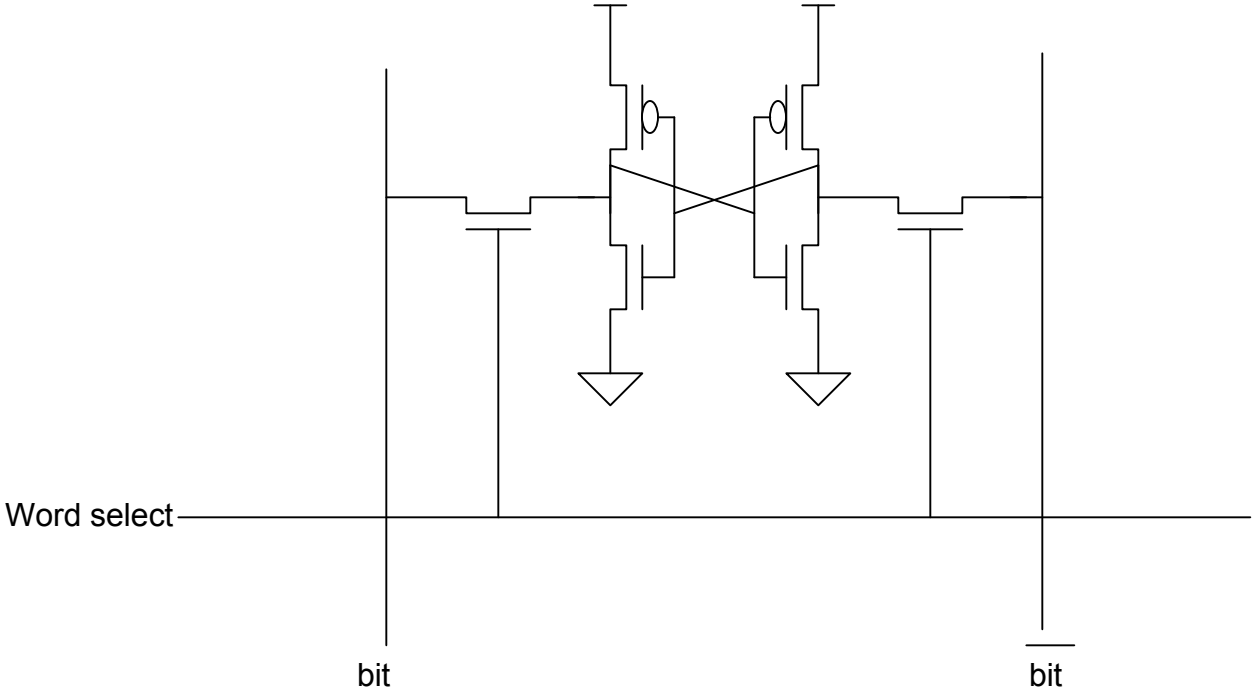
Memory Design

- Static RAM Cell



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Memory Design

- Reads are straightforward
  - May need precharge circuitry to pull up bit line
- Writes are trickier
  - Use driver transistors that will pull-up or pull-down bit line as necessary

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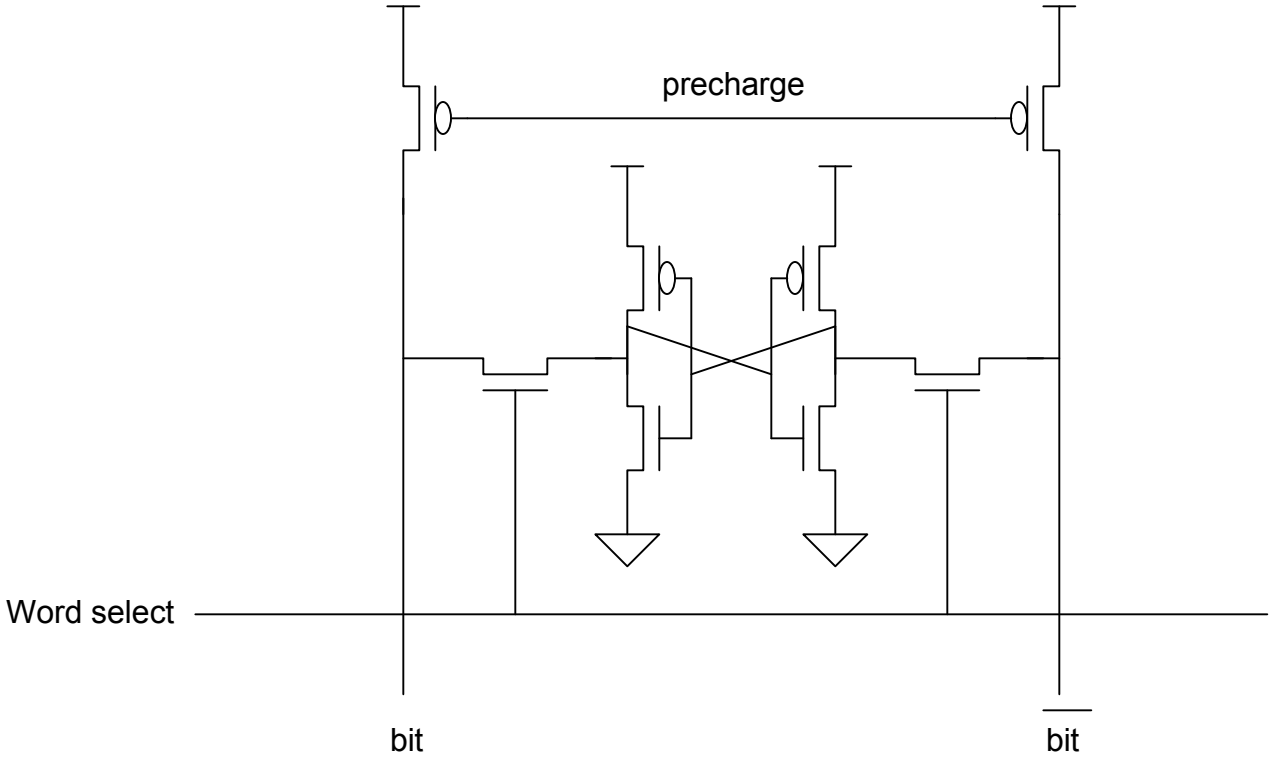
Memory Design

- Static RAM Cell with precharge



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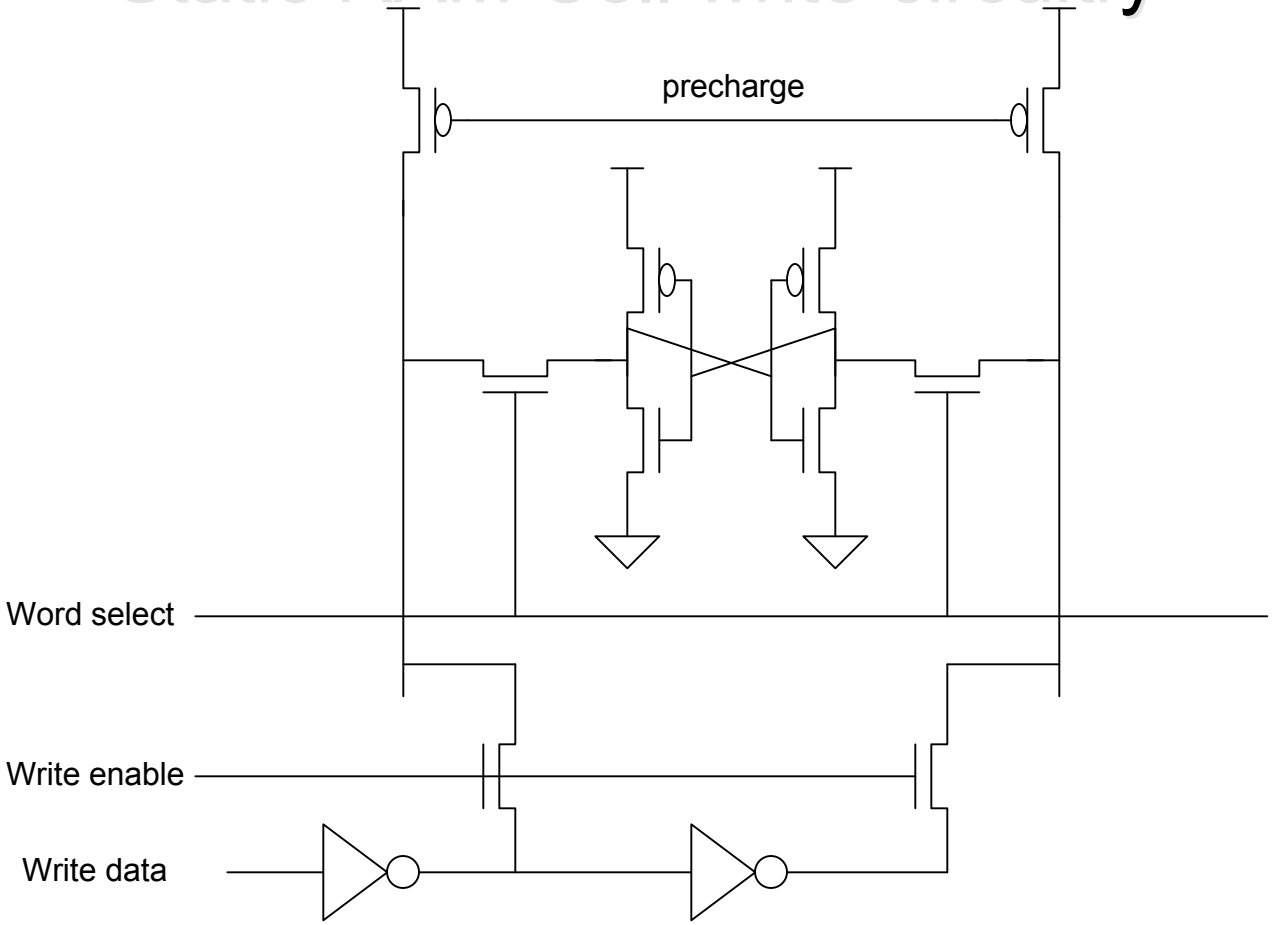
Memory Design

- Static RAM Cell write circuitry



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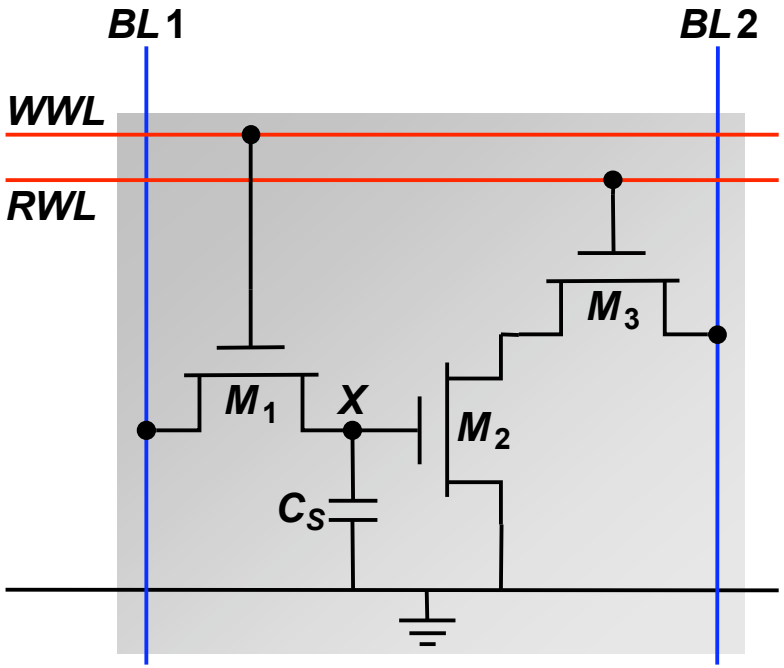
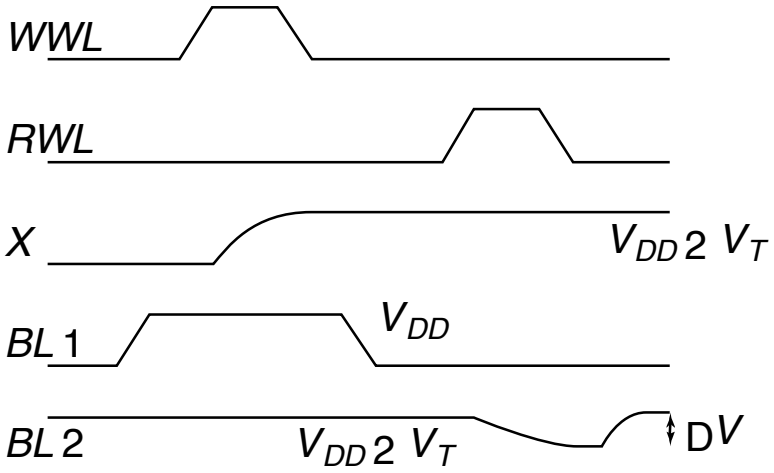
3-Transistor DRAM Cell



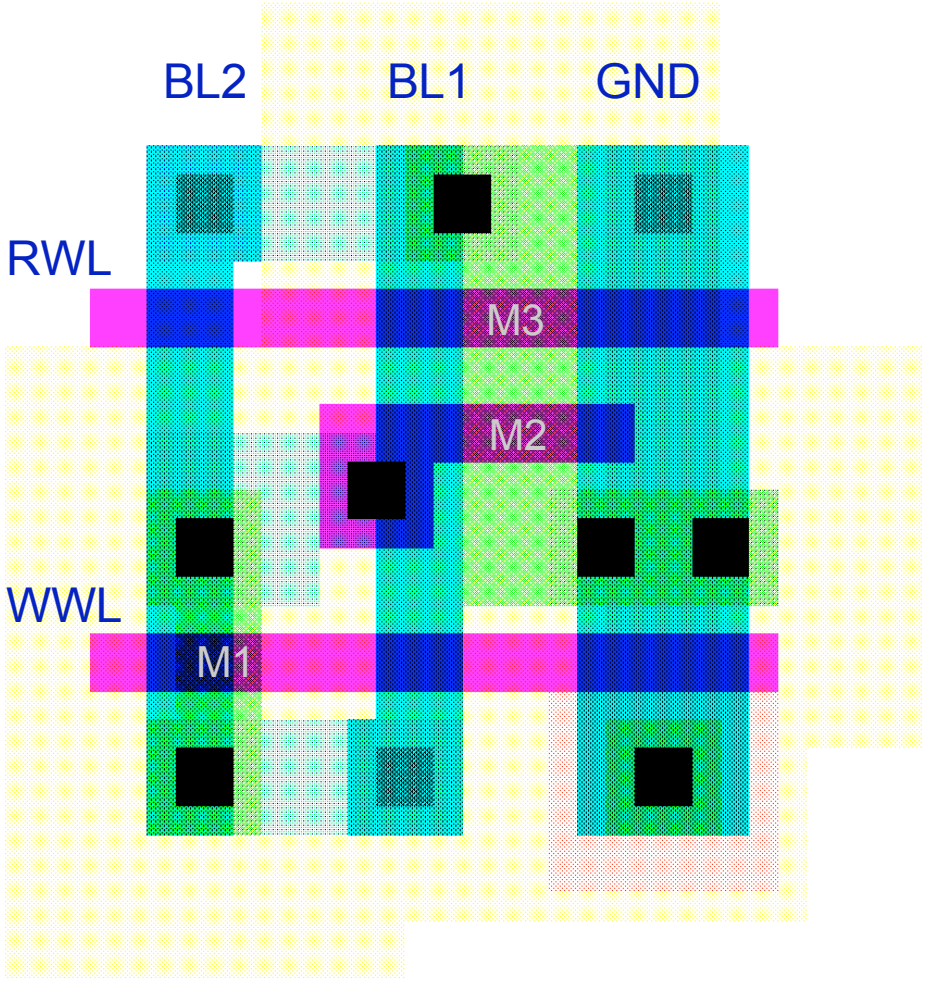


No constraints on device ratios

Reads are non-destructive

Value stored at node X when writing a "1" = V_{WWL}-V_{Tn}

3T-DRAM — Layout



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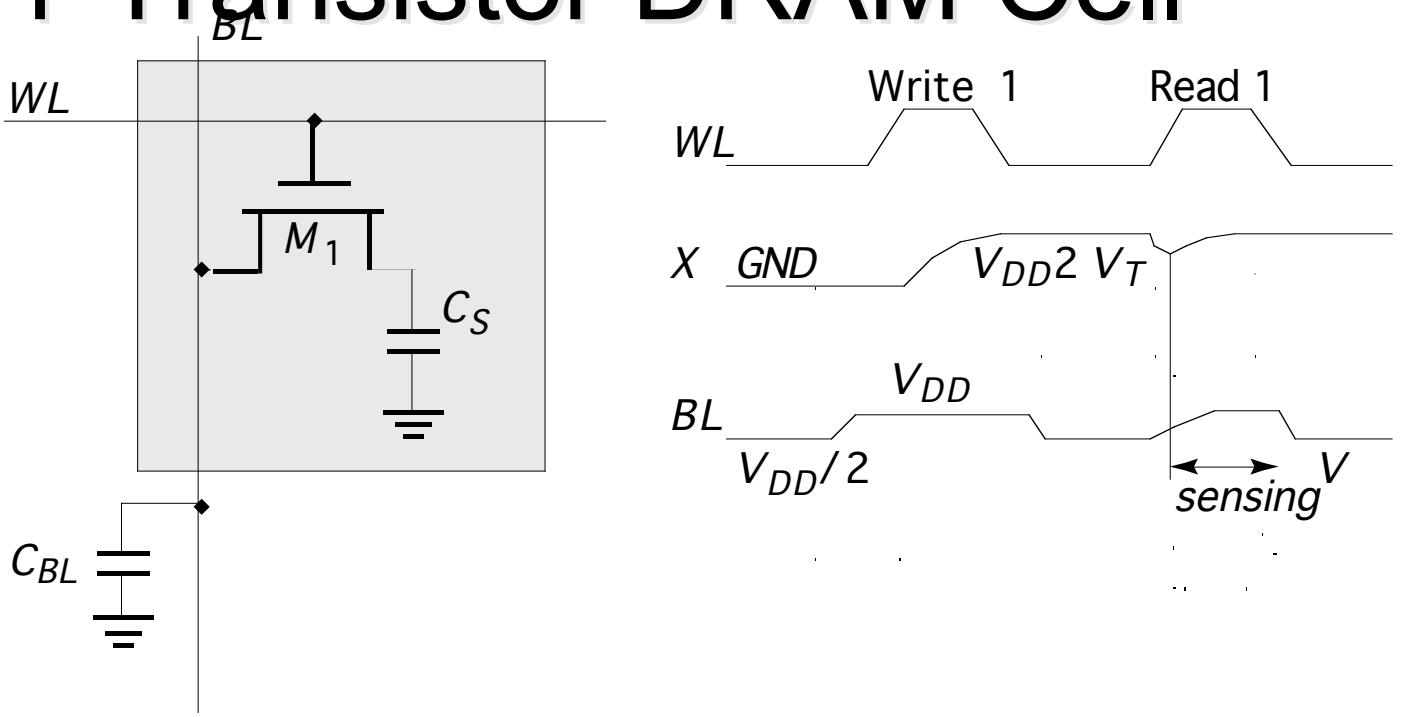
1-Transistor DRAM Cell



Write: C_S is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes places between bit line and storage capacitance

$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.

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DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a "1" into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

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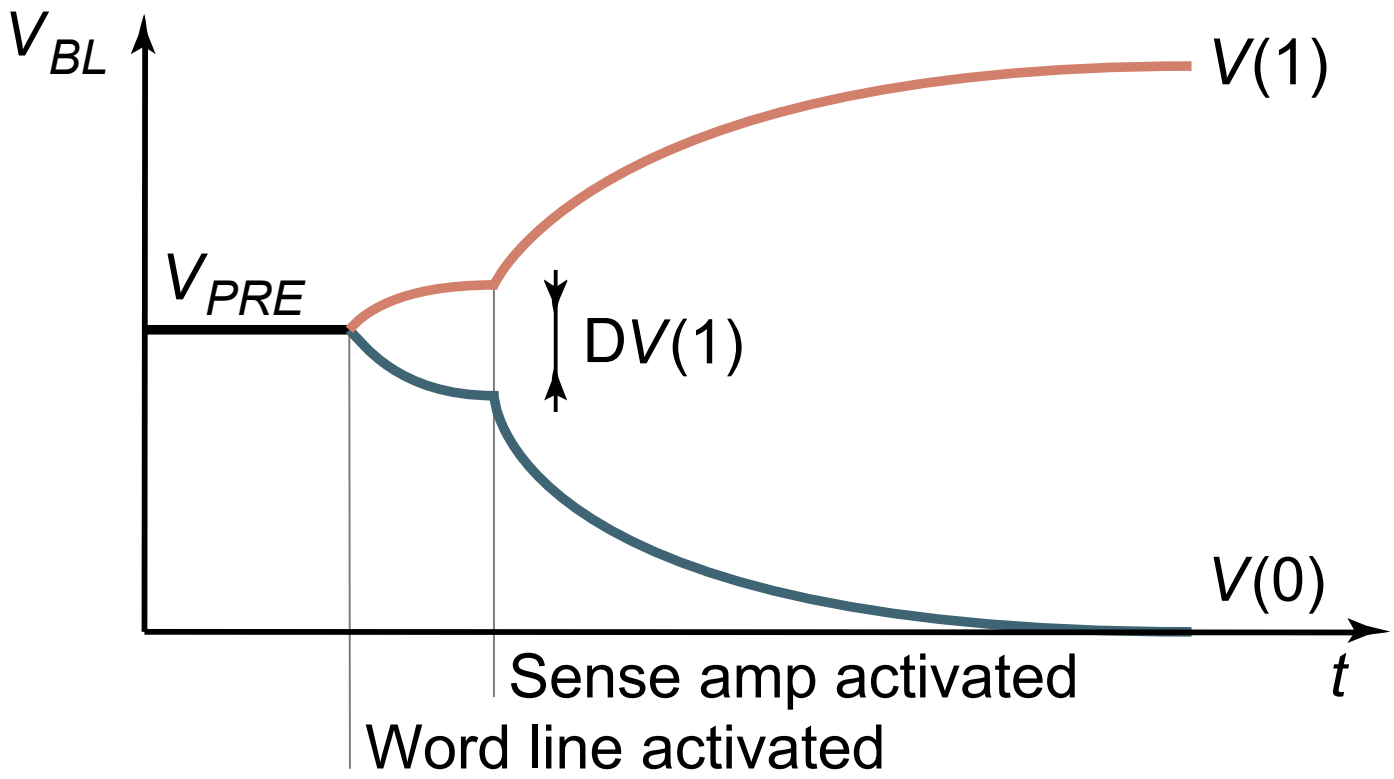
Sense Amp Operation



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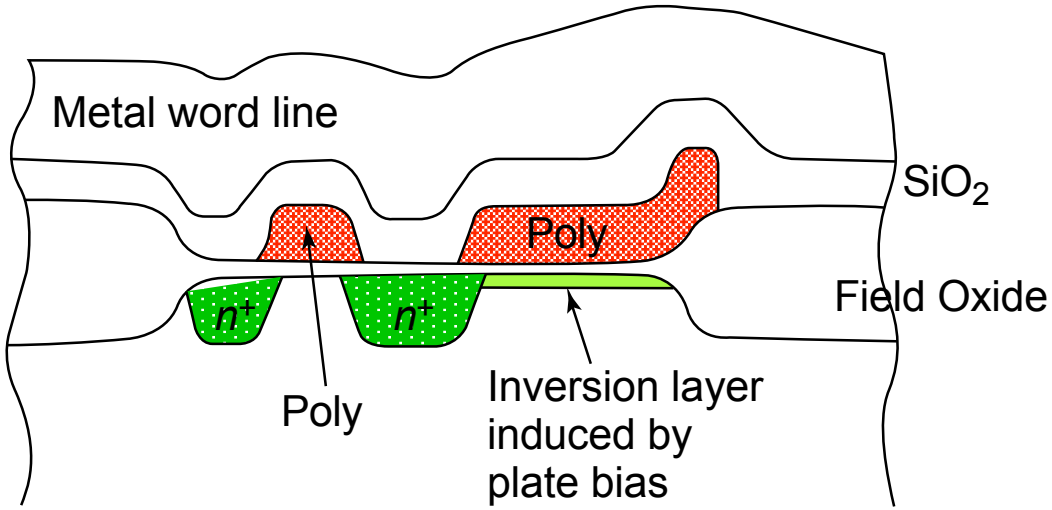
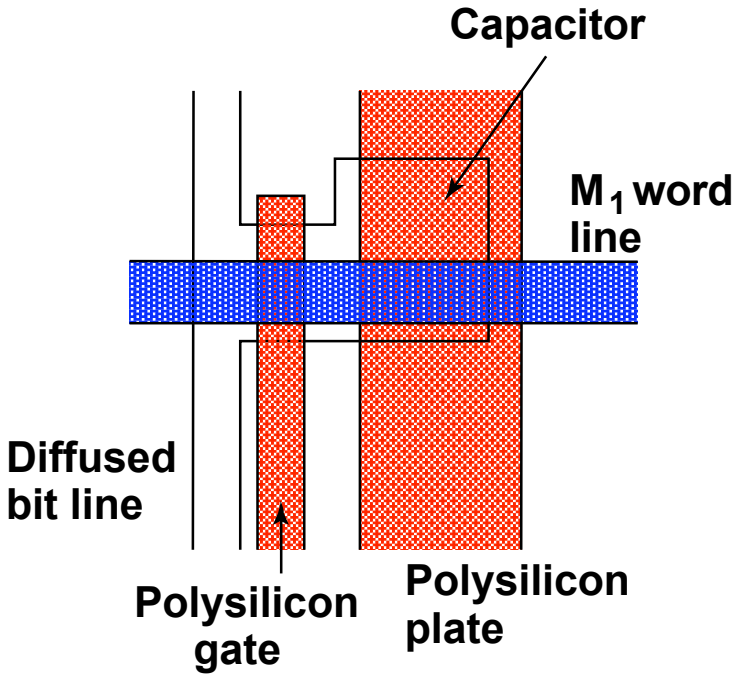
1-T DRAM Cell



Cross-section



Layout

Uses Polysilicon-Diffusion Capacitance

Expensive in Area

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Memory Design

- RAMs
  - Static RAM is faster, does not need to be refreshed
  - Dynamic RAM is more compact

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Next class

- More about memory
- Control logic

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