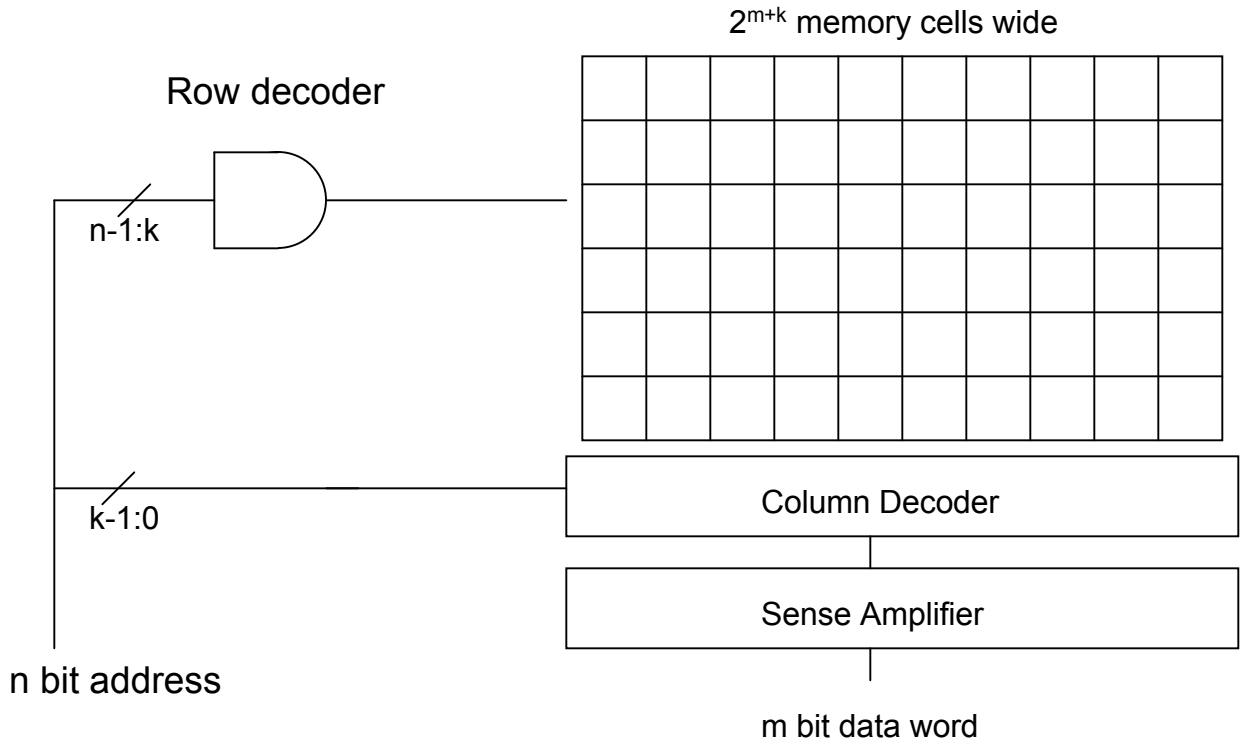
Memory Design

- Random Access Memory



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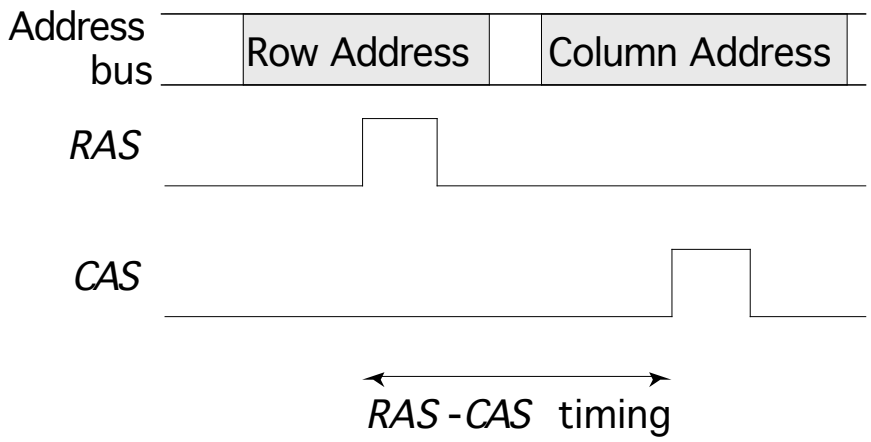
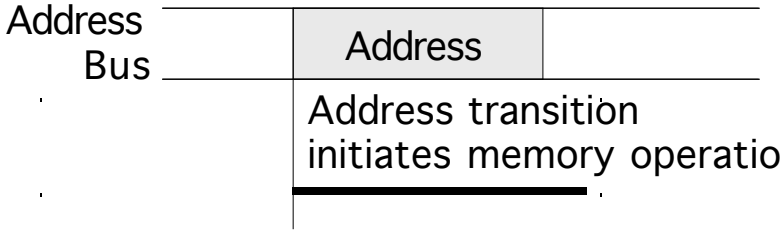
Memory Timing: Approaches



DRAM Timing
Multiplexed Adressing



SRAM Timing
Self-timed

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Memory Timing

- DRAM read cycle
  - Activate RAS, and place row address on bus
  - Row decoders select appropriate row
  - Activate CAS, and place column address on bus
  - Sense amps are activated and data is placed on the data bus

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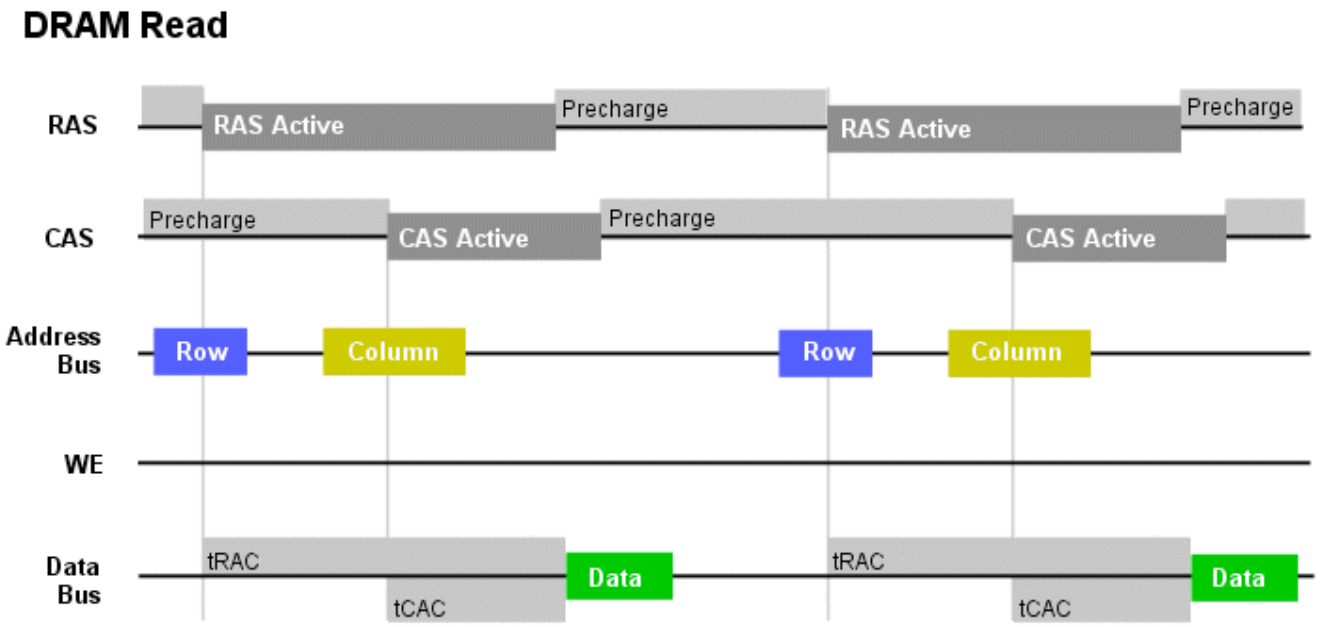
Memory Timing



from “Ars Technica RAM Guide”, by Jon Stokes, ©Ars Technica LLC

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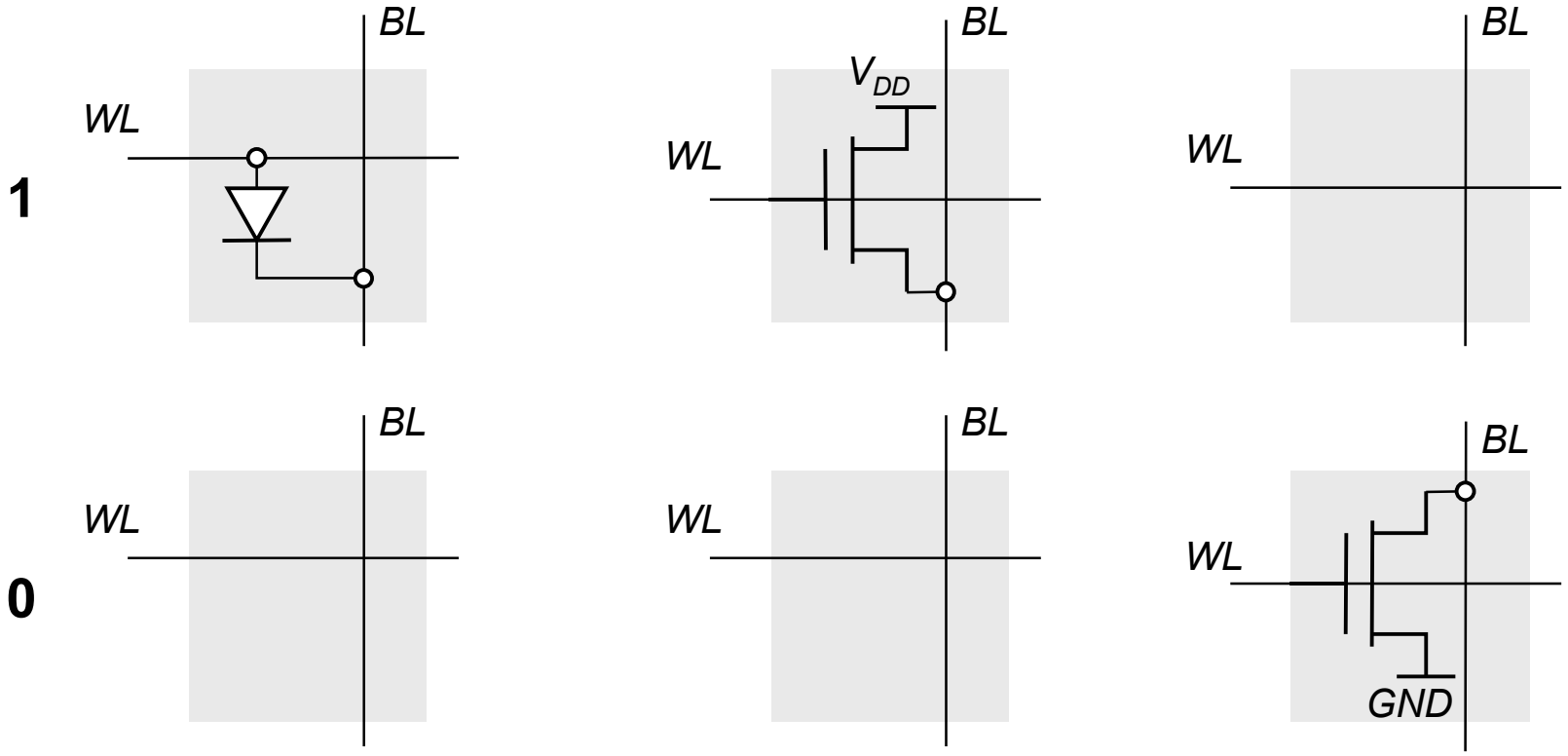
Read-Only Memory Cells



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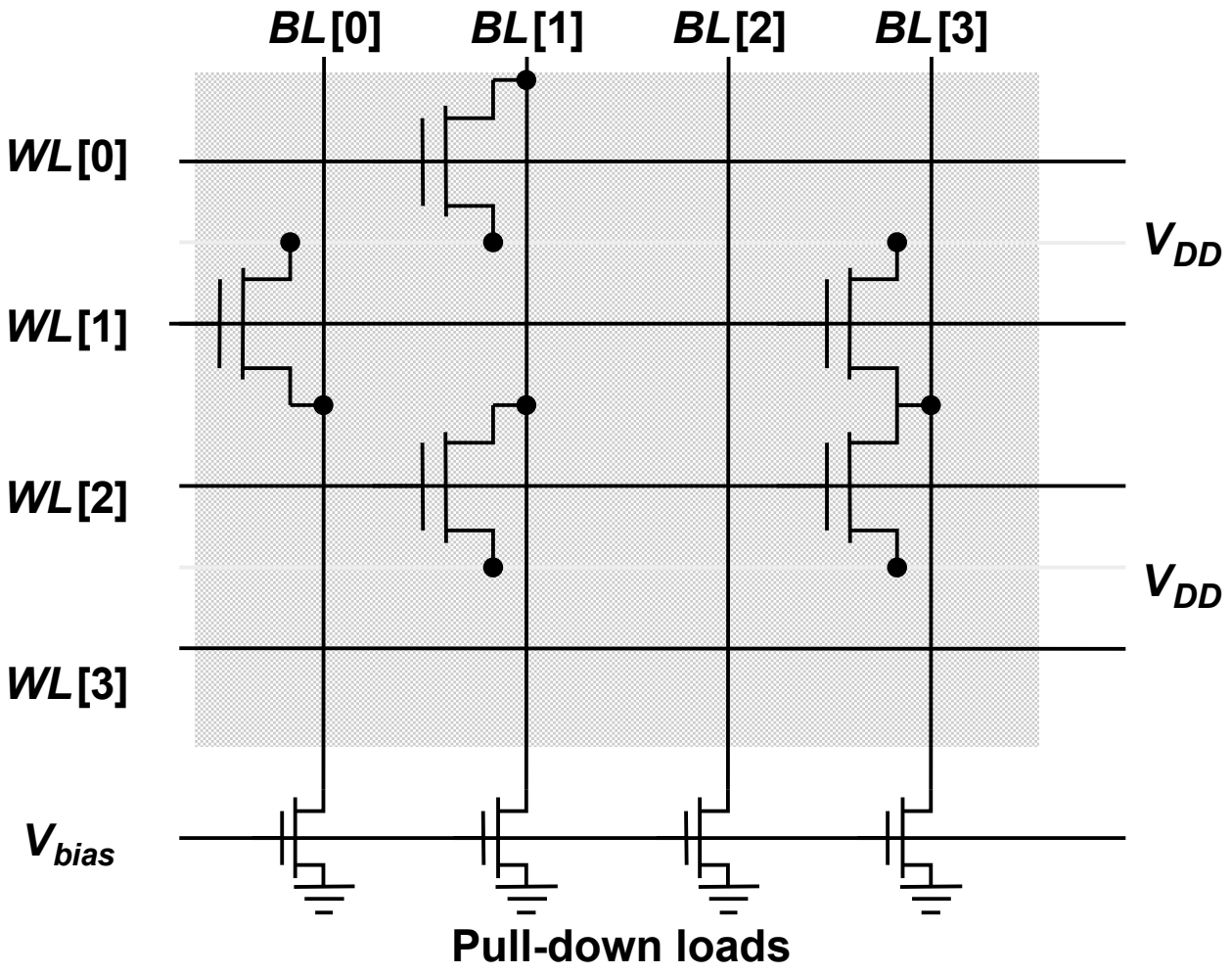
MOS OR ROM



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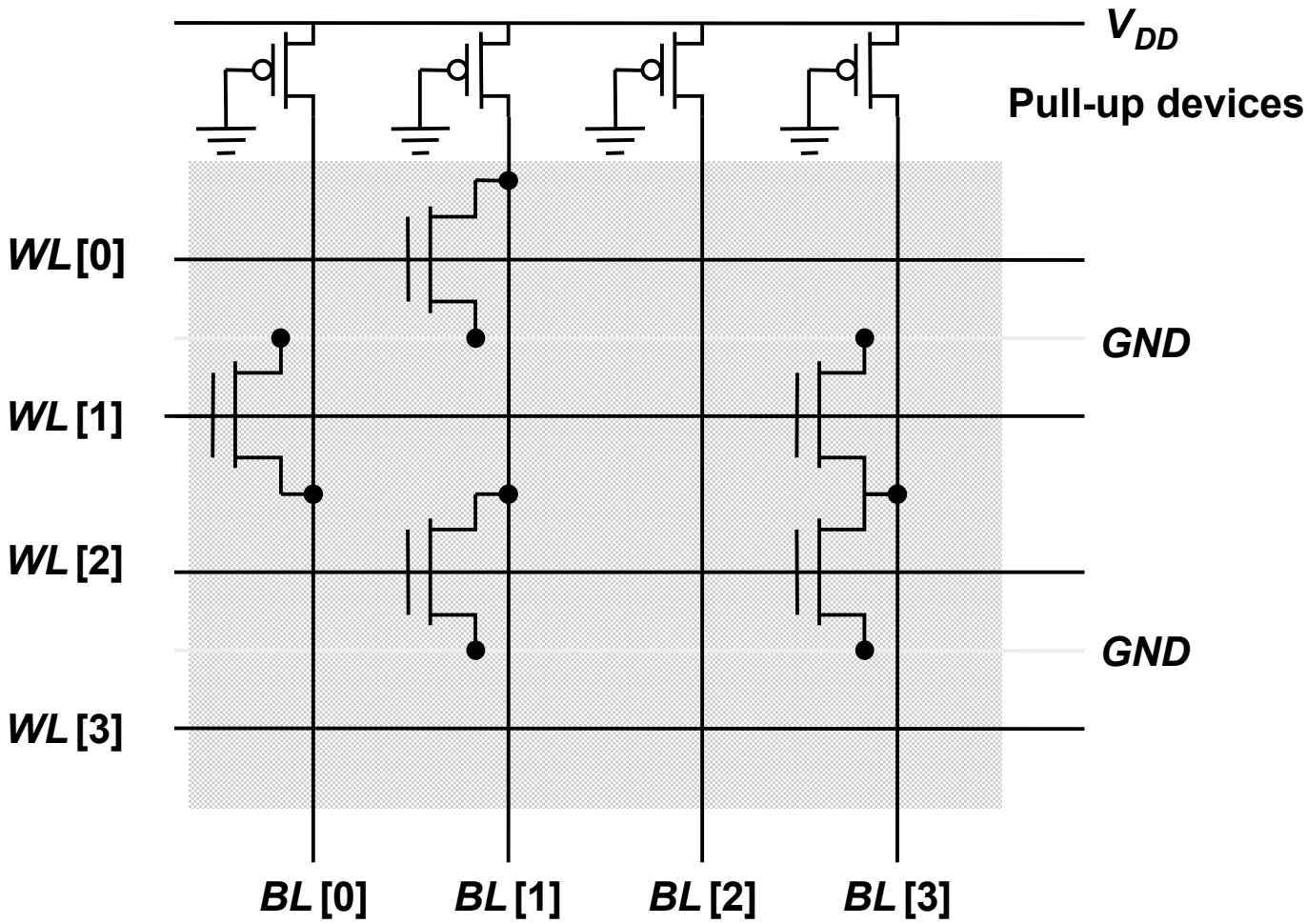
MOS NOR ROM



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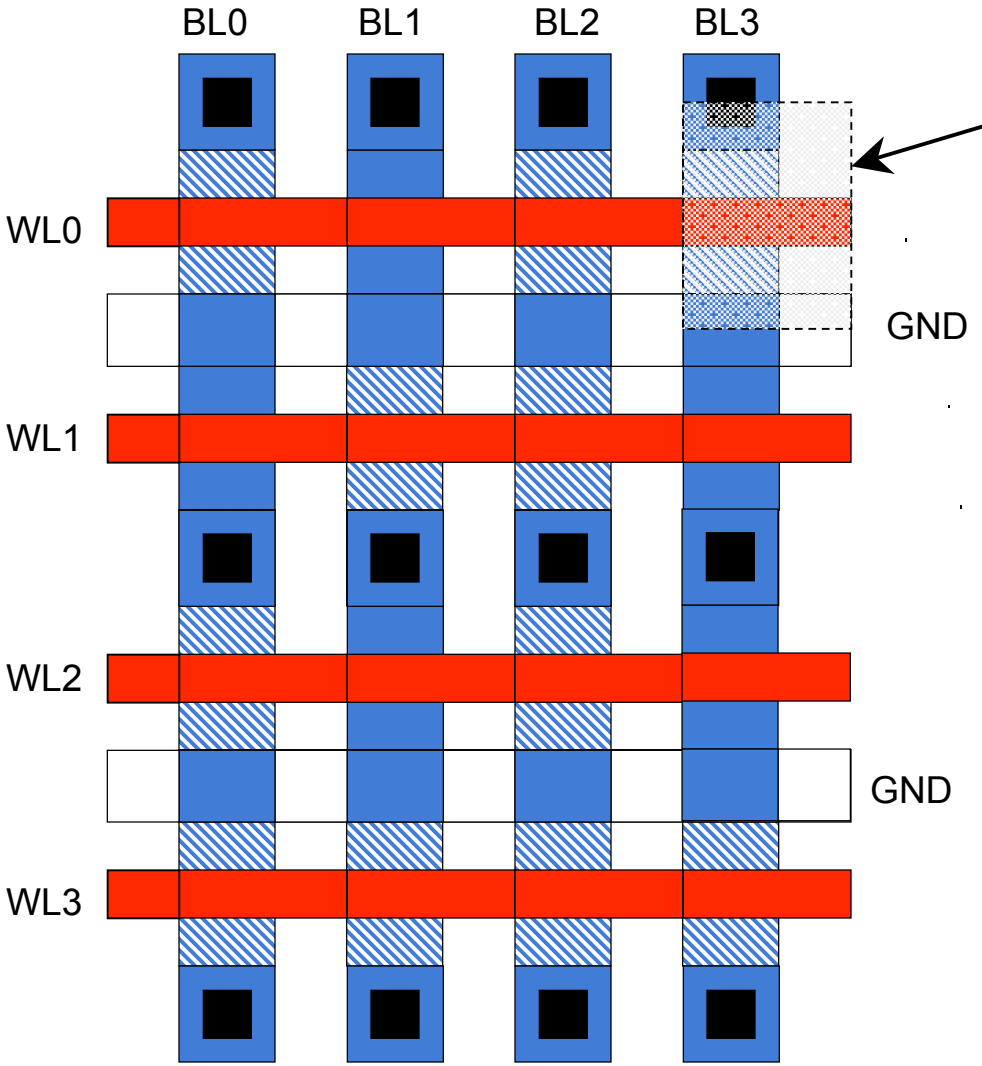
MOS NOR ROM Layout



Cell (9.5λ x 7λ)

Programmming using the Active Layer Only

Polysilicon

Metal1

Diffusion

Metal1 on Diffusion

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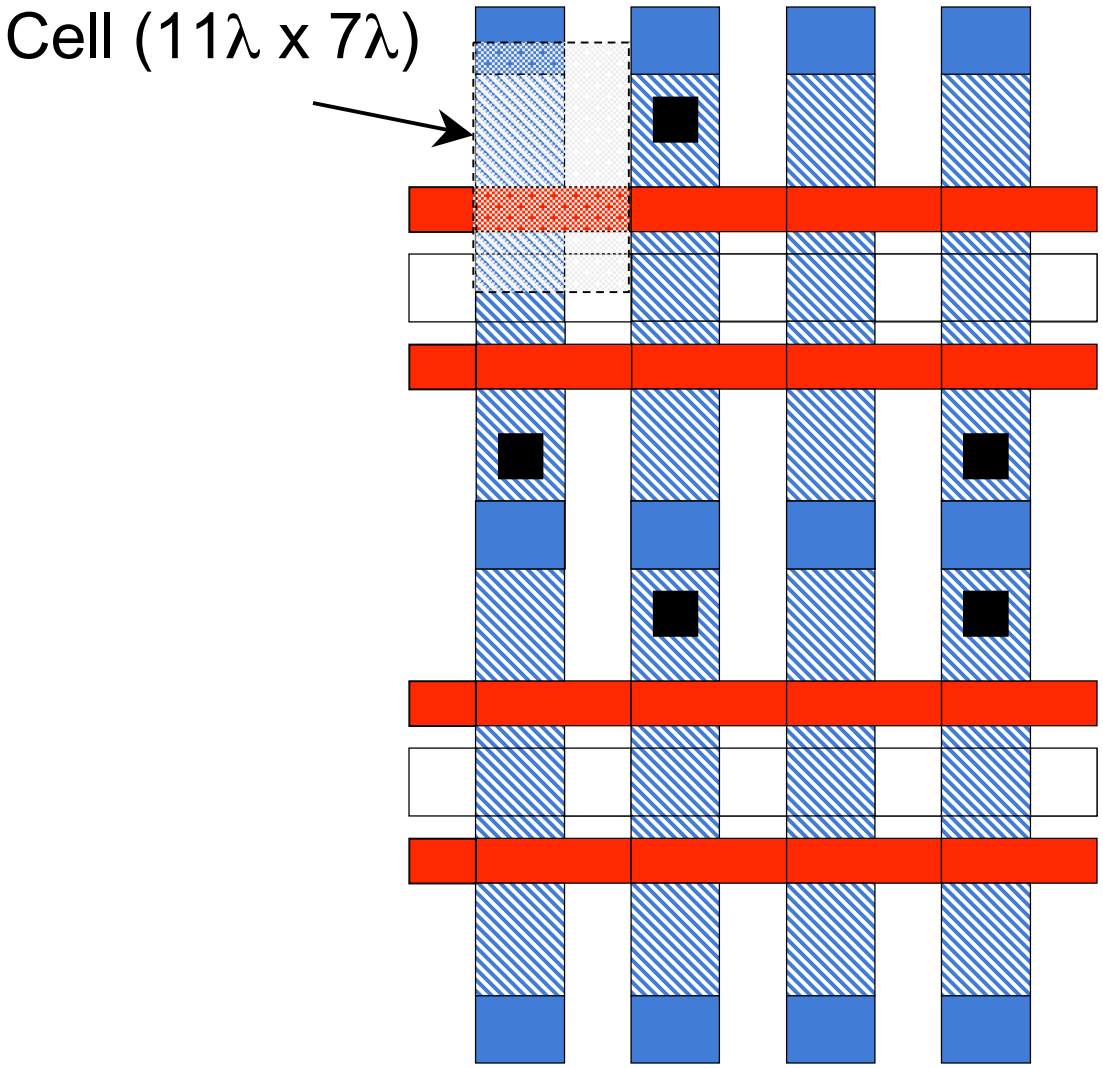
MOS NOR ROM Layout



Programmming using the Contact Layer Only

Polysilicon

Metal1

Diffusion

Metal1 on Diffusion

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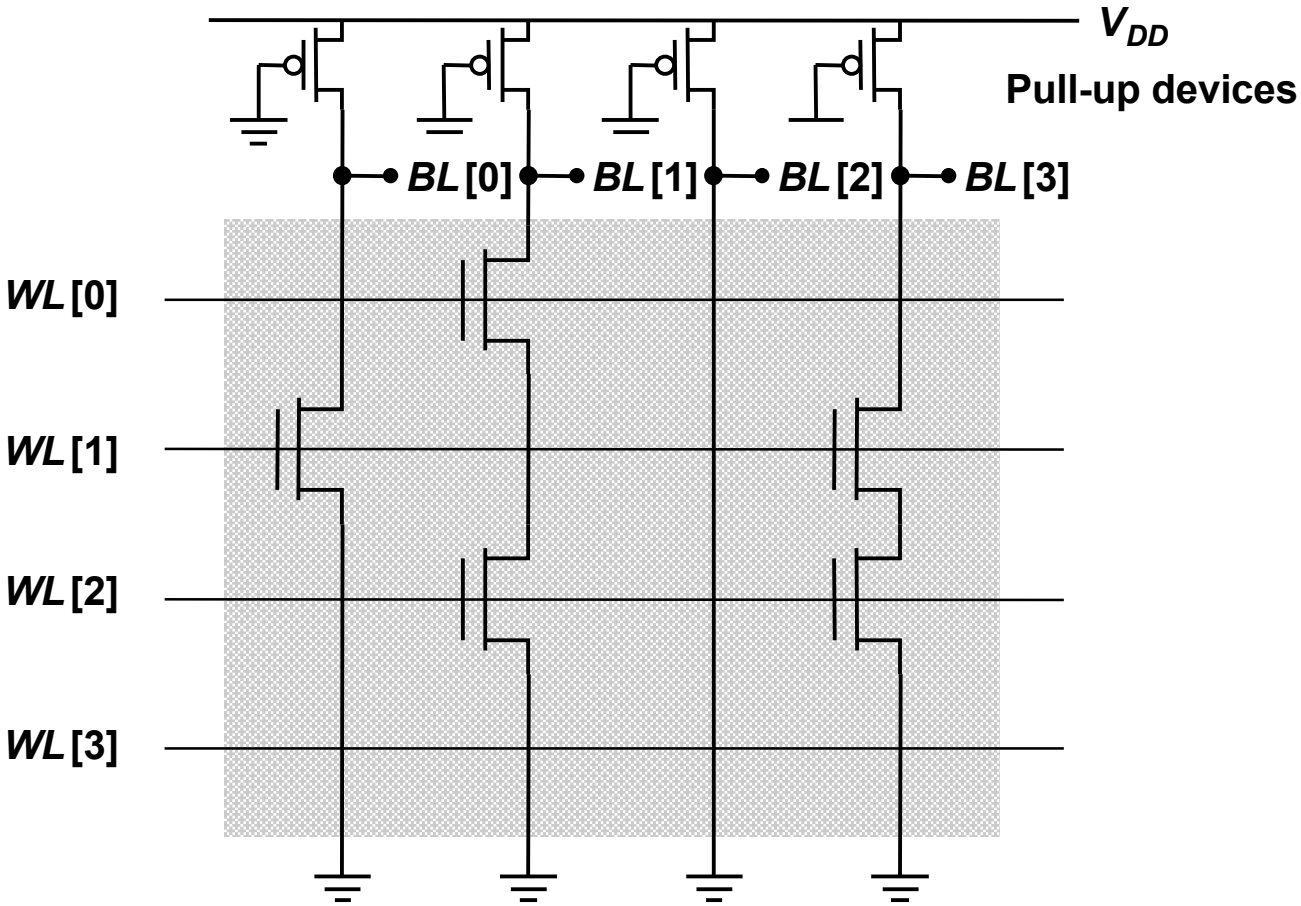
MOS NAND ROM



All word lines high by default with exception of selected row

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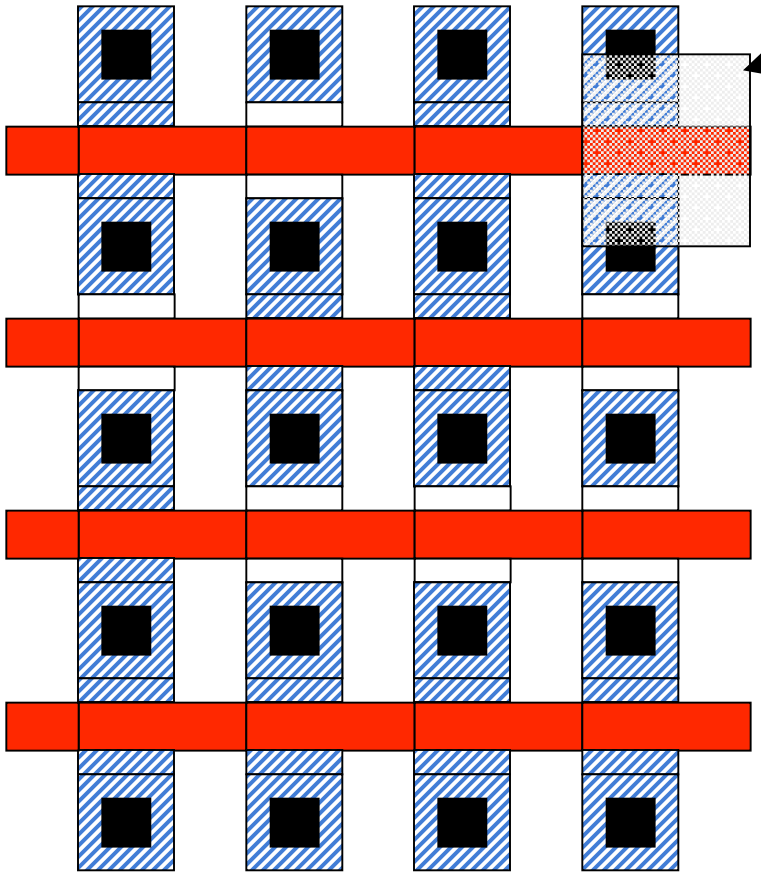
MOS NAND ROM Layout



Programmming using the Metal-1 Layer Only

No contact to VDD or GND necessary; drastically reduced cell size

Loss in performance compared to NOR ROM

Polysilicon

Diffusion

Metal1 on Diffusion

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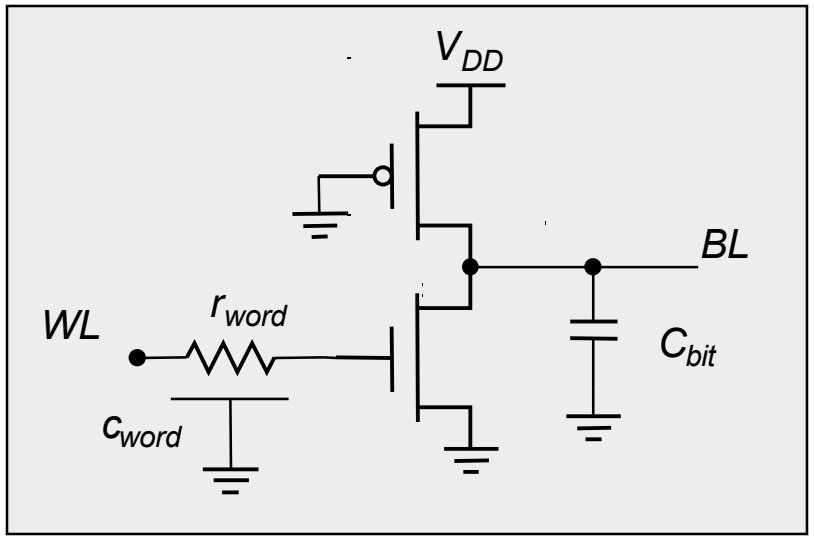
Equivalent Transient Model for MOS NOR ROM

Model for NOR ROM



- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance

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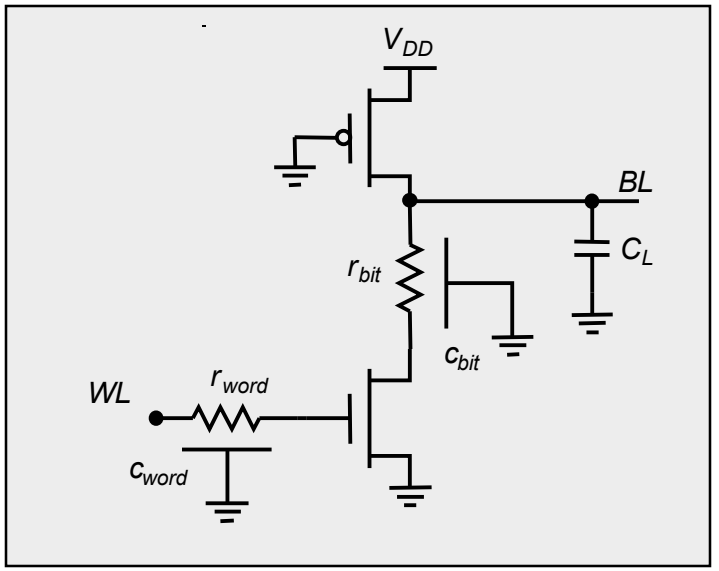
Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM



- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance

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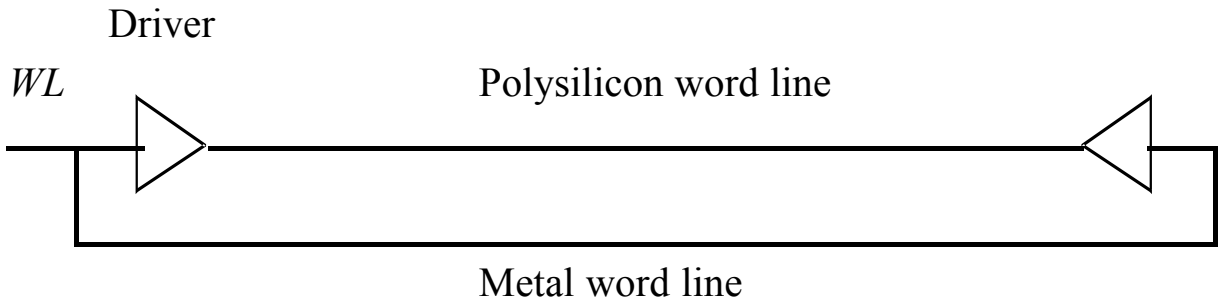
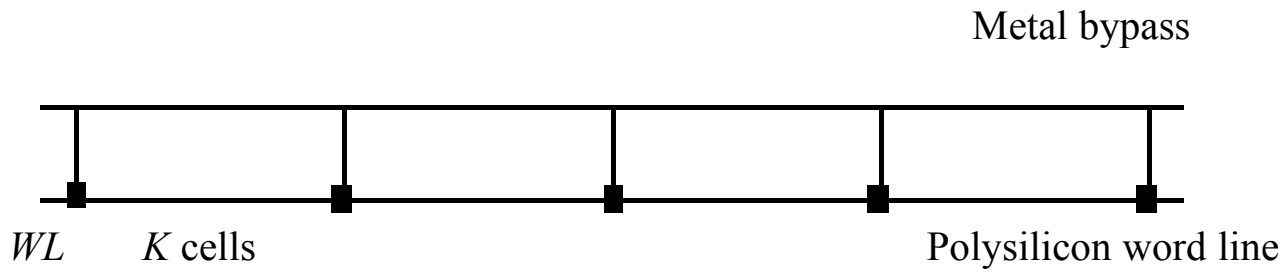
Decreasing Word Line Delay



(a) Driving the word line from both sides



(b) Using a metal bypass

(c) Use silicides

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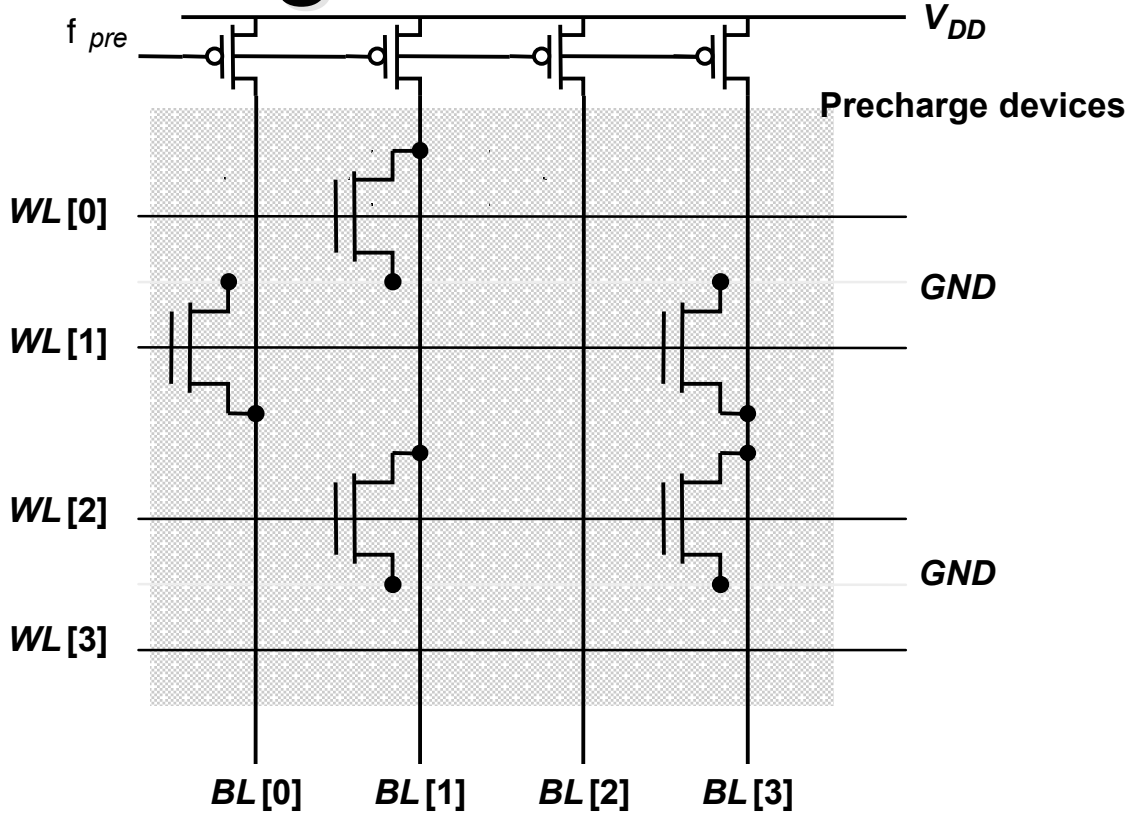
Precharged MOS NOR ROM



PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.

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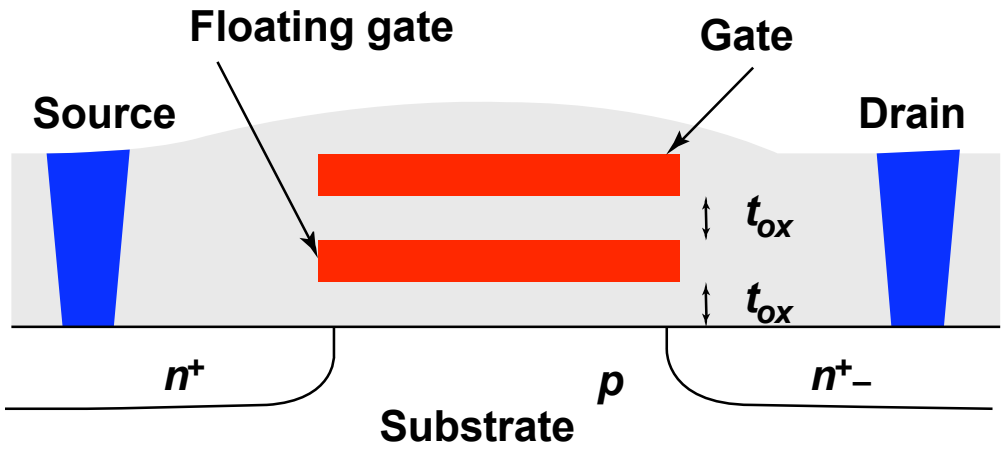
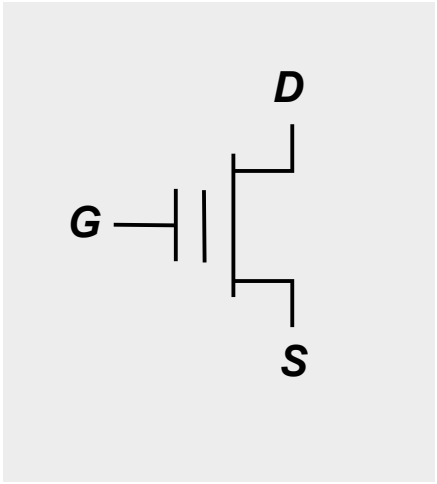
Non-Volatile Memories
The Floating-gate transistor (FAMOS)



Device cross-section



Schematic symbol

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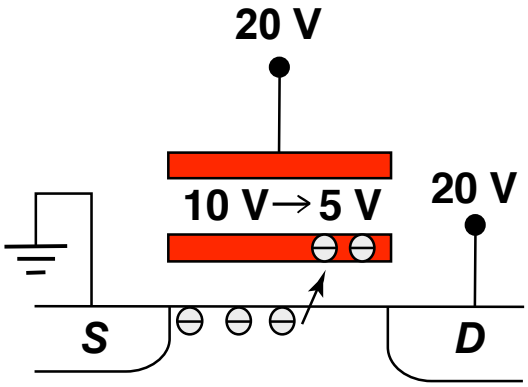
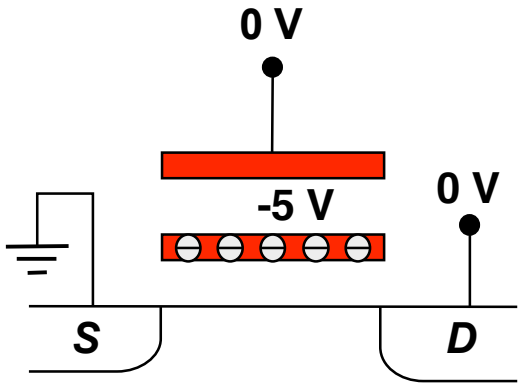
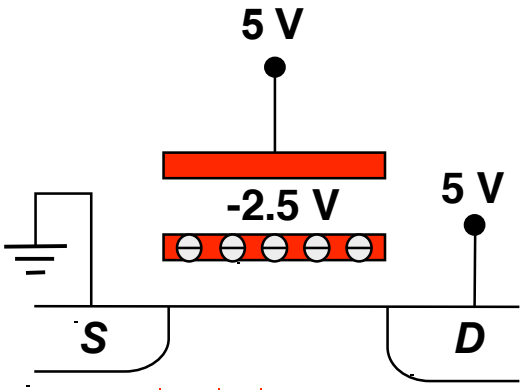
Floating-Gate Transistor Programming



Avalanche injection



Removing programming voltage leaves charge trapped



Programming results in higher V_T.

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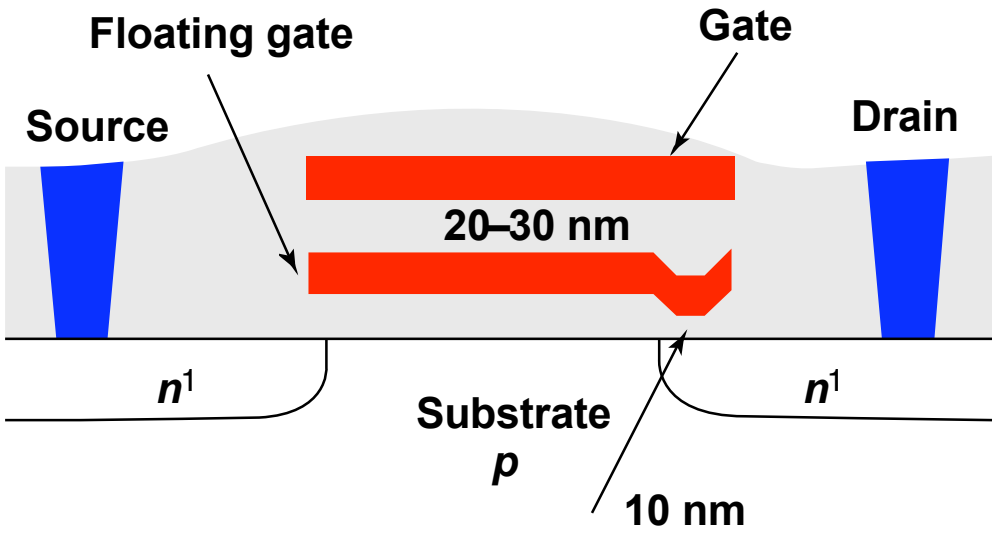
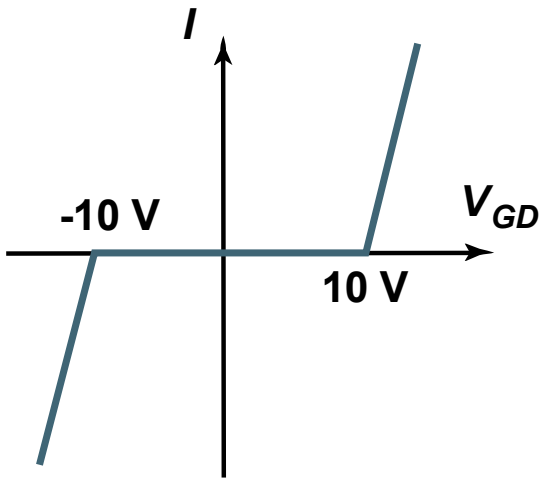
FLOTOX EEPROM



FLOTOX transistor



Fowler-Nordheim
I-V characteristic

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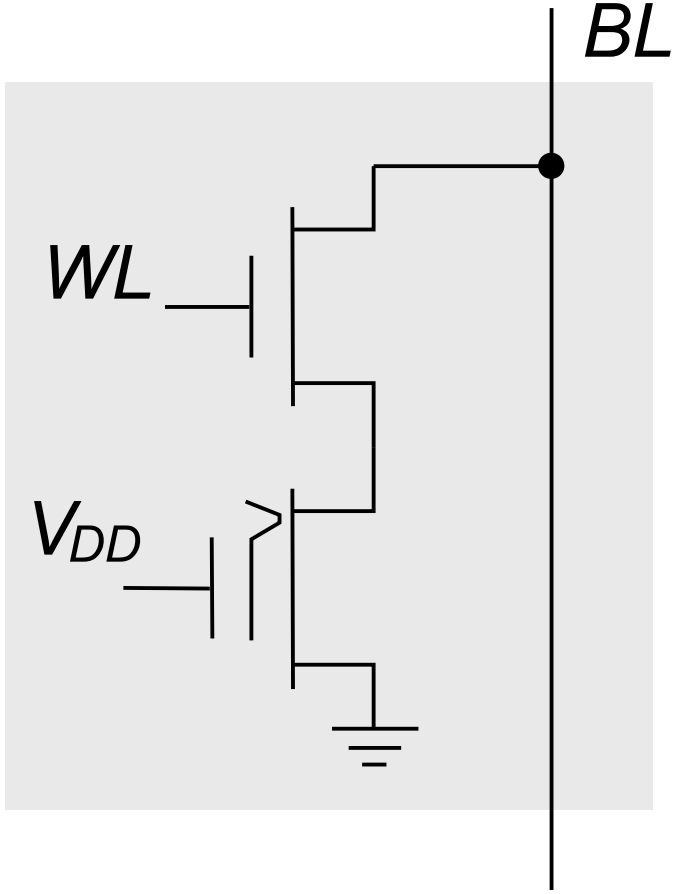
EEPROM Cell



Absolute threshold control is hard
Unprogrammed transistor might be depletion
⇨ 2 transistor cell

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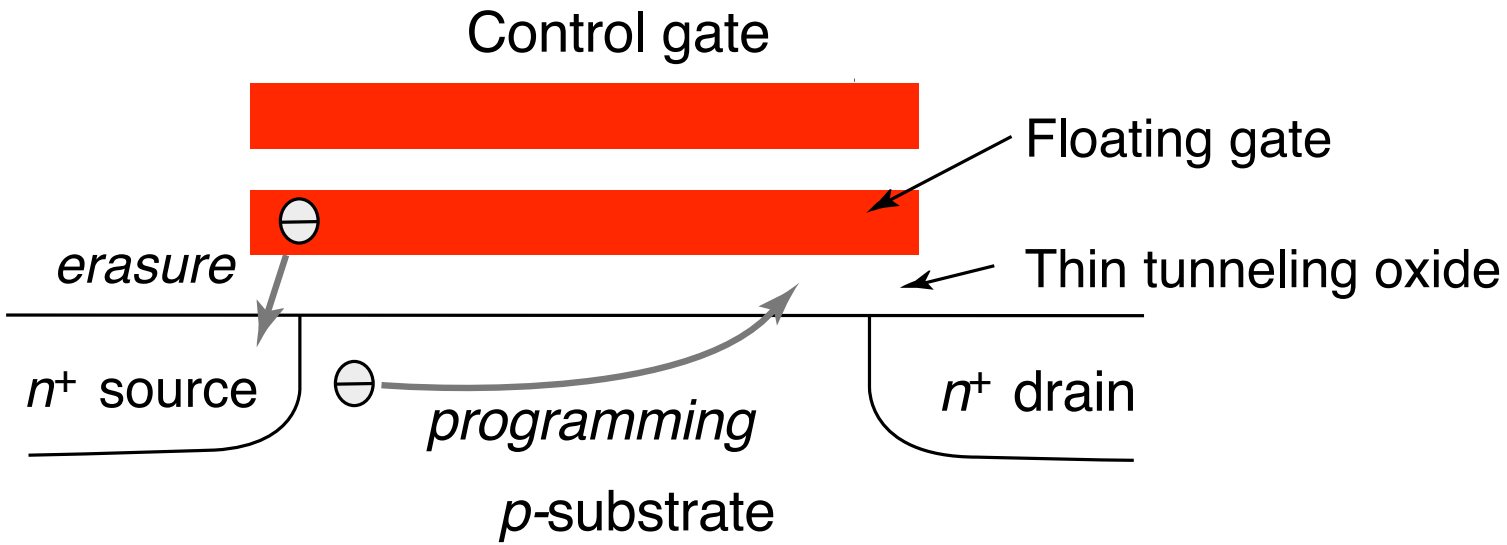
Flash EEPROM



Many other options …

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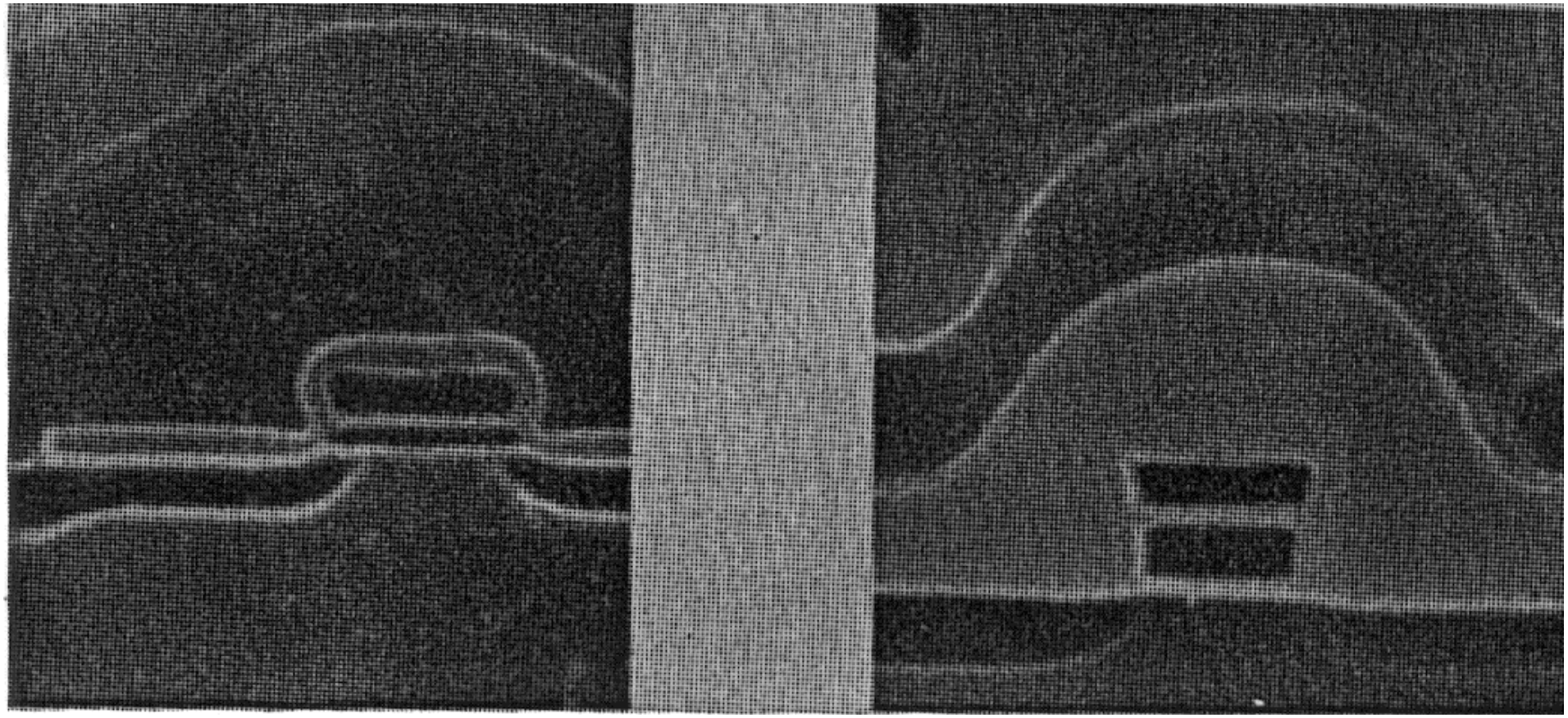
Cross-sections of NVM cells



Flash **EPROM**

Courtesy Intel

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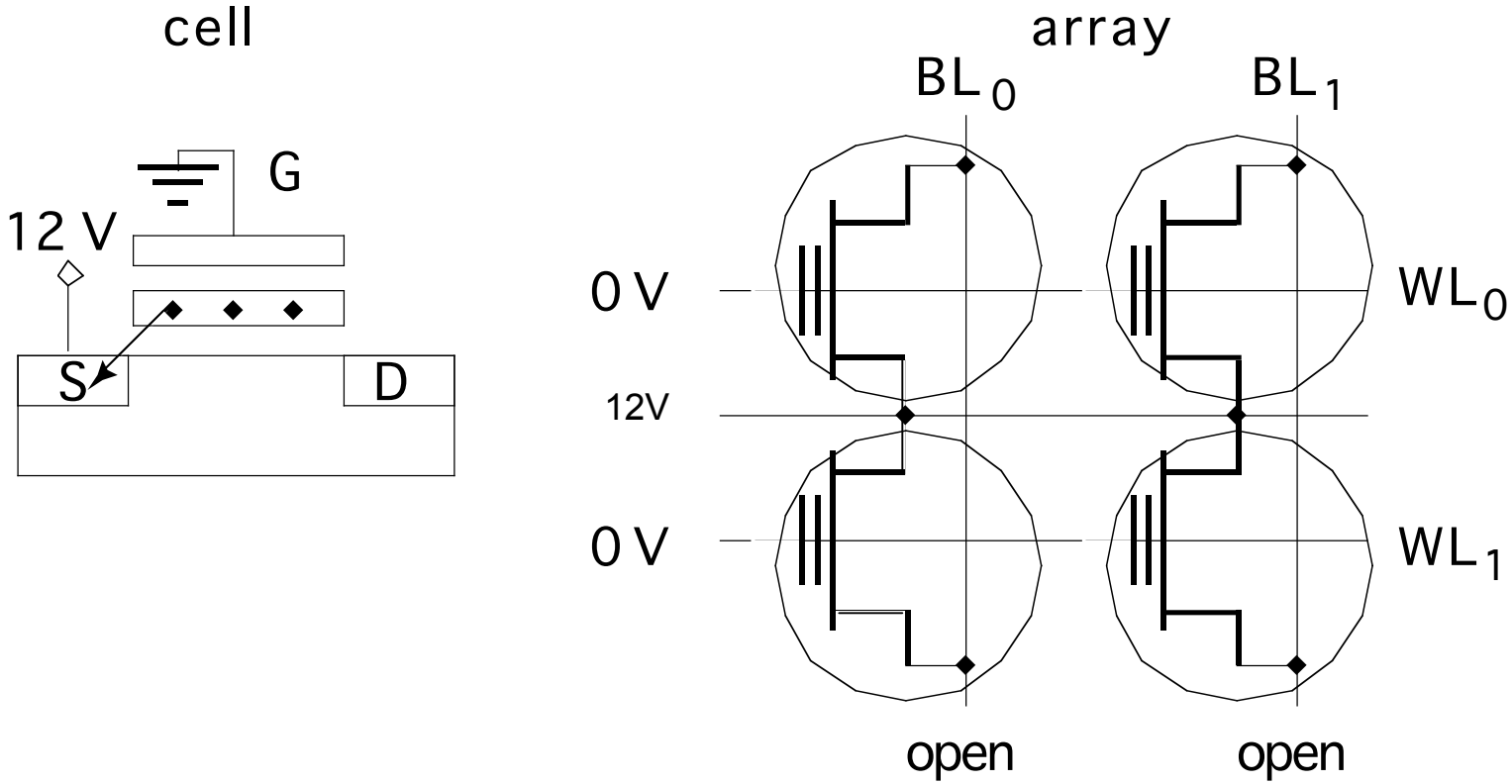
Basic Operations in a NOR Flash Memory_ Erase



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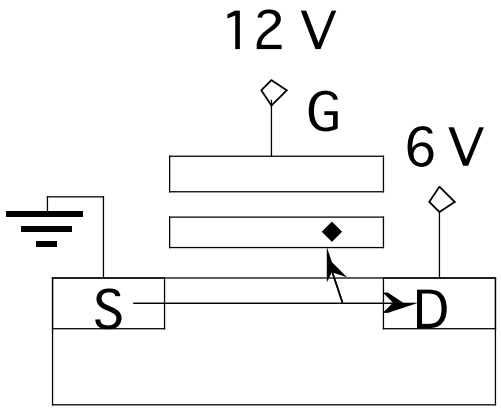
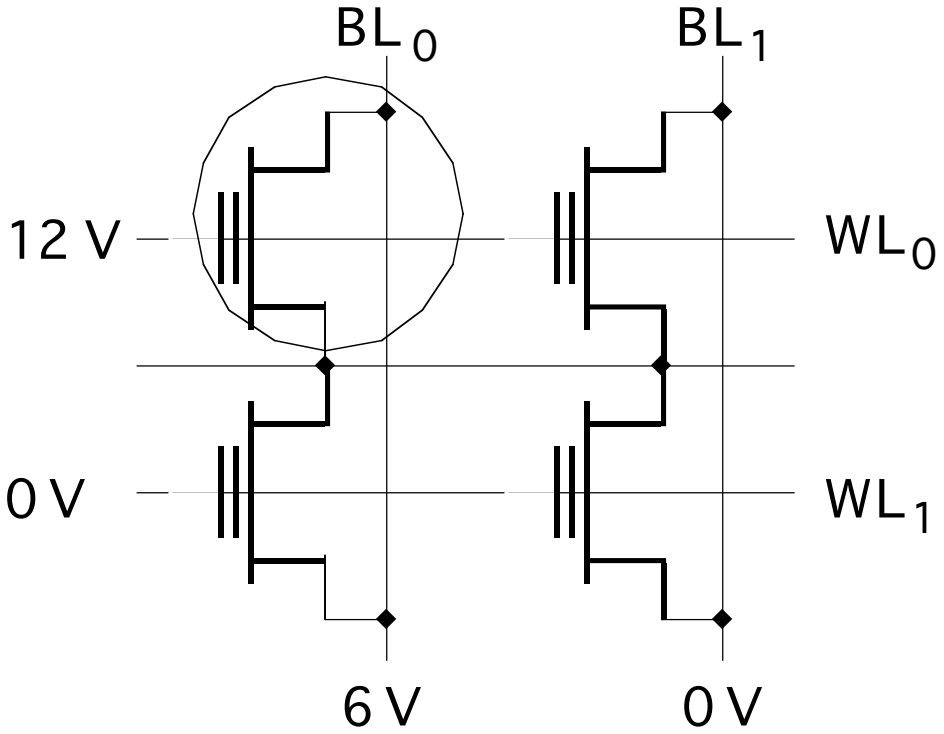
Basic Operations in a NOR Flash Memory_ Write





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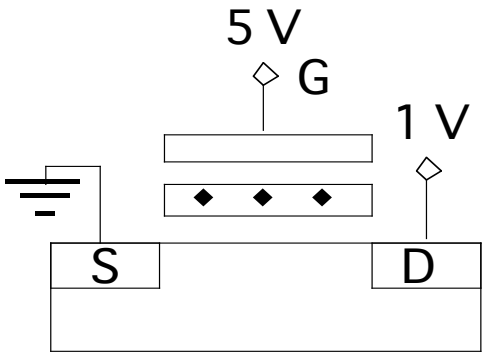
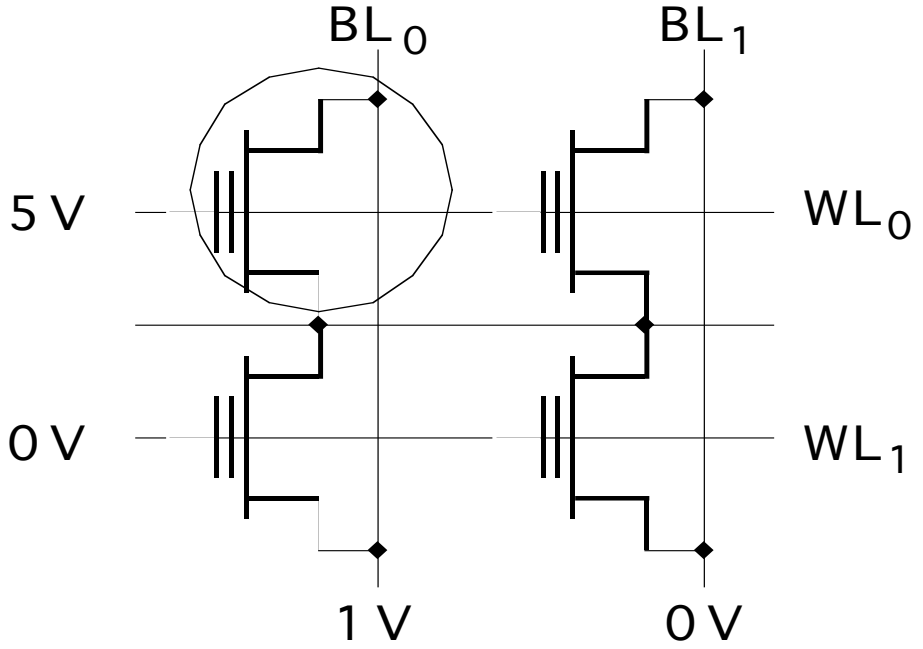
Basic Operations in a NOR Flash Memory_ Read





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Memory Design

- Register File
  - RAM with multiple read or write ports
  - You can read or write multiple data values at the same time
  - Useful in data processing applications

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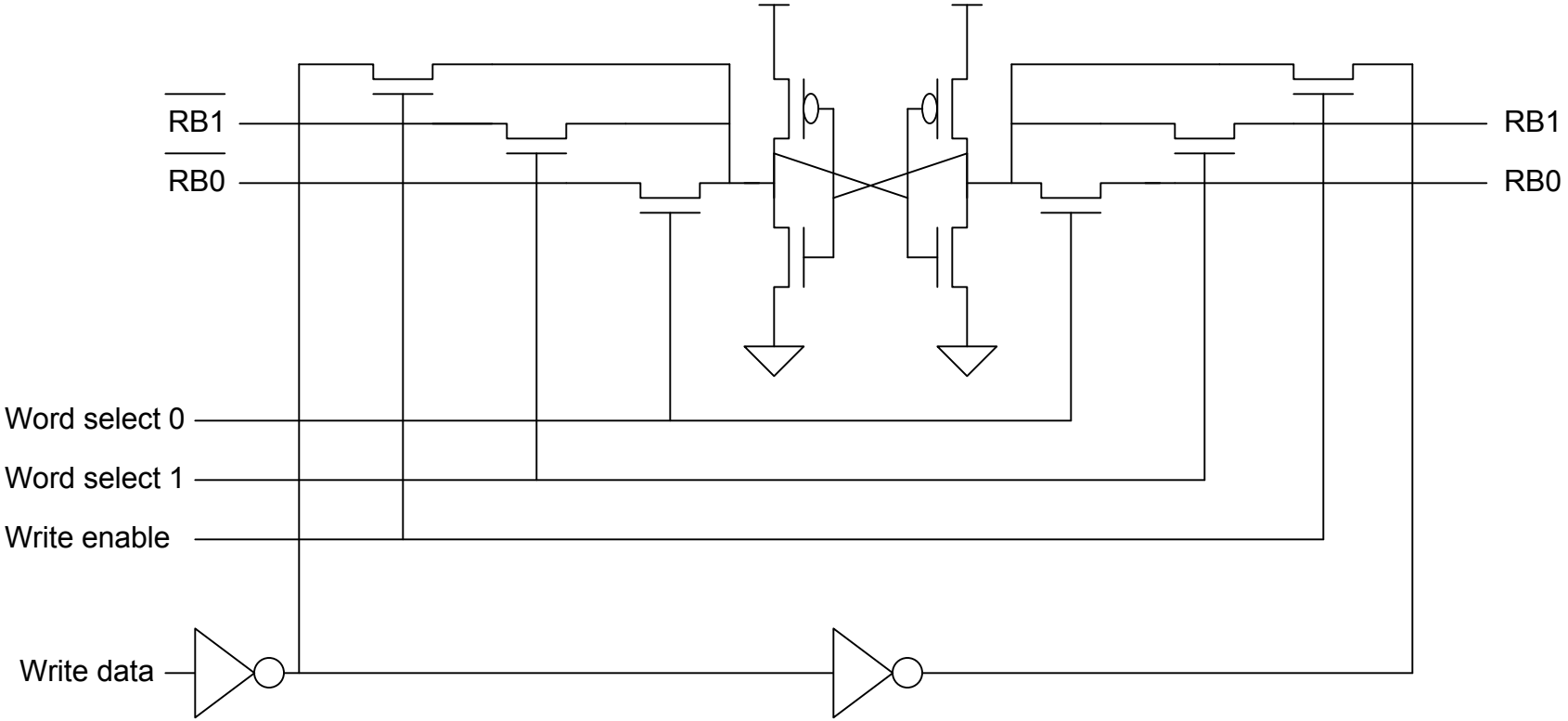
Memory Design

- Register File Cell



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Memory Design

- Content Addressable Memory (CAM)
  - Instead of finding memory by address, find it by content
  - Search or match every single word in memory array

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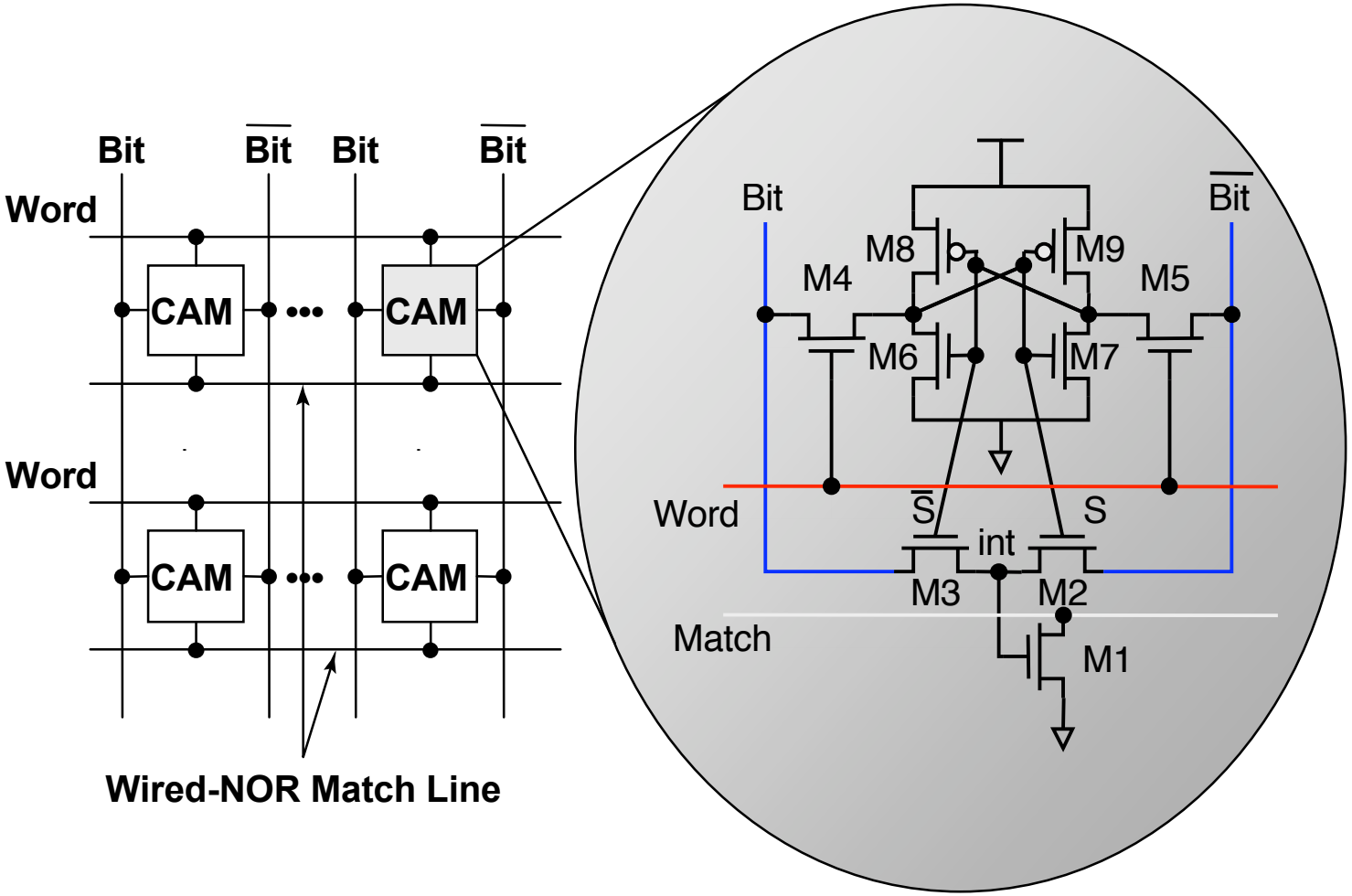
Static CAM Memory Cell



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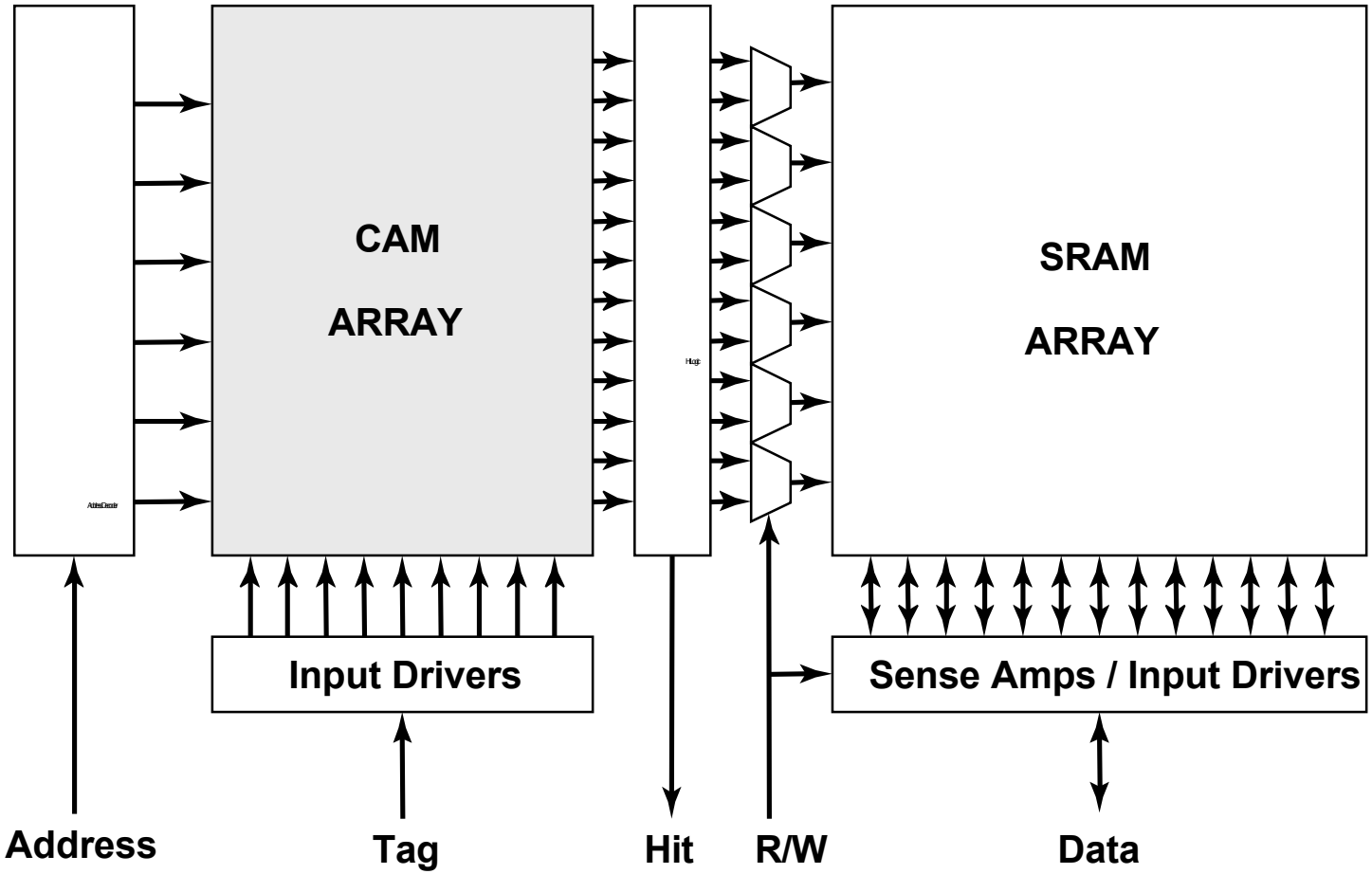
CAM in Cache Memory



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Memory Design

- Other memory structures
  - FIFOs
  - LIFOs
  - SIPOs

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Periphery

- Decoders
- Sense Amplifiers
- Input/Output Buffers
- Control / Timing Circuitry

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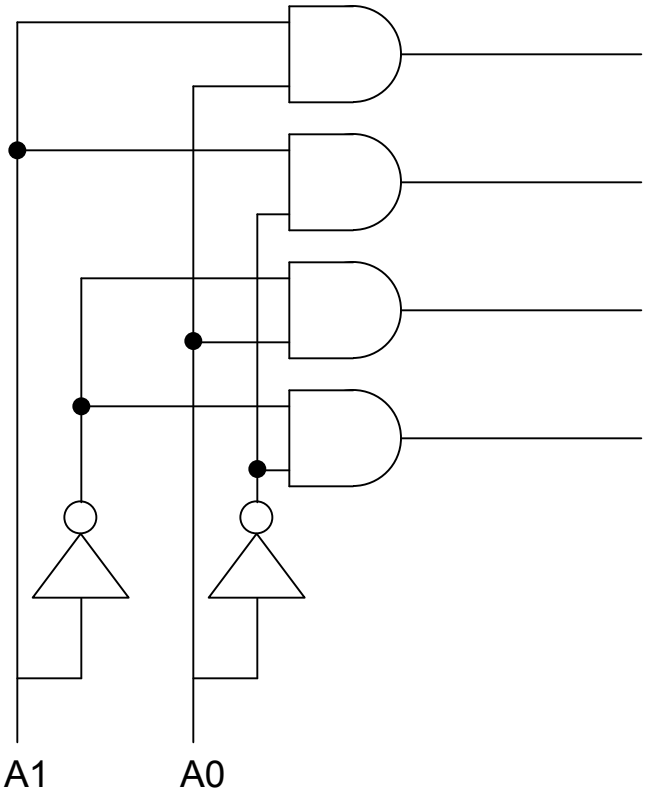
Memory Design

- Row decoder



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Memory Design

- Row decoder
  - With multiple inputs (>4), two problems
    - Speed of gates becomes a problem
      - Use hierarchy of NANDS/NORS
      - Use predecoding - decode upper bits first and use lower bits to select from there
    - Increased fanout
      - Use minimum sized input gates

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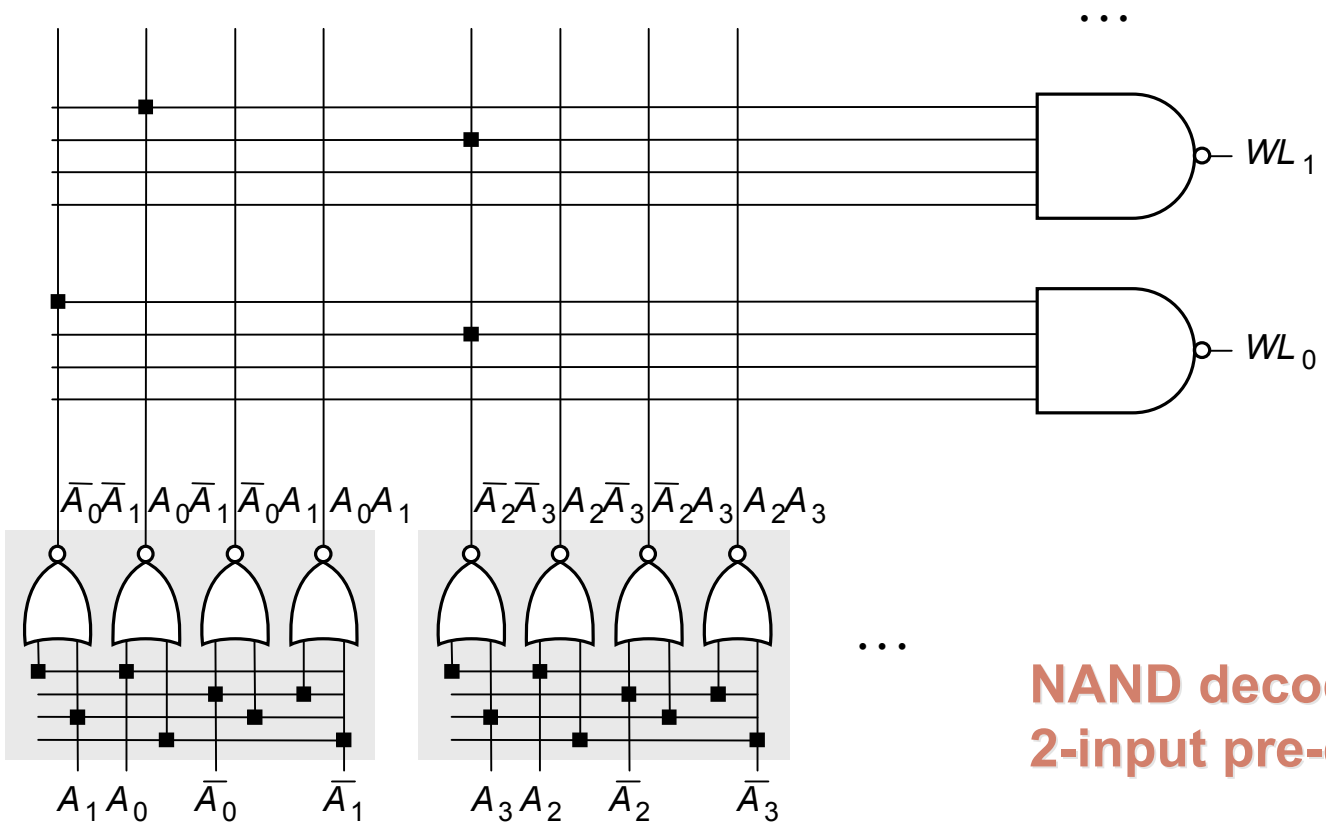
Hierarchical Decoders

Multi-stage implementation improves performance



NAND decoder using 2-input pre-decoders

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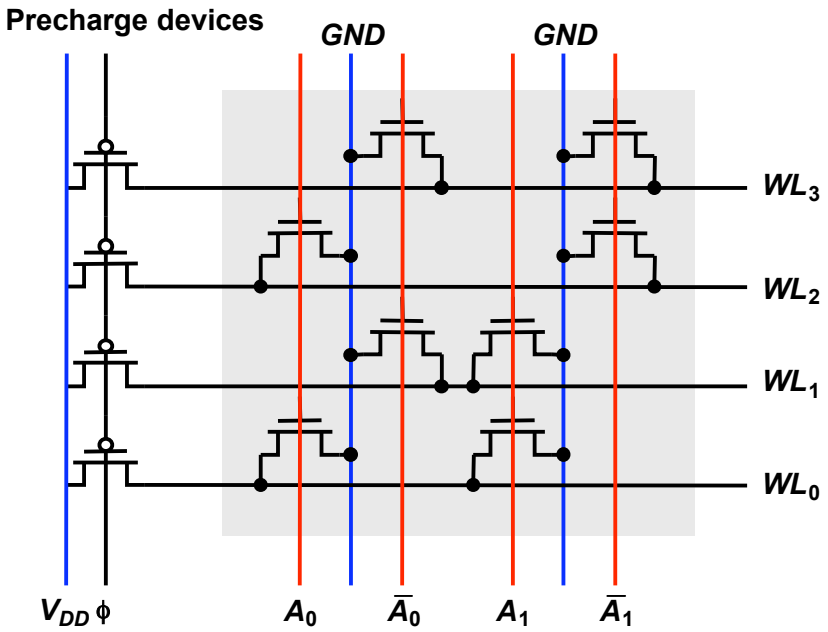
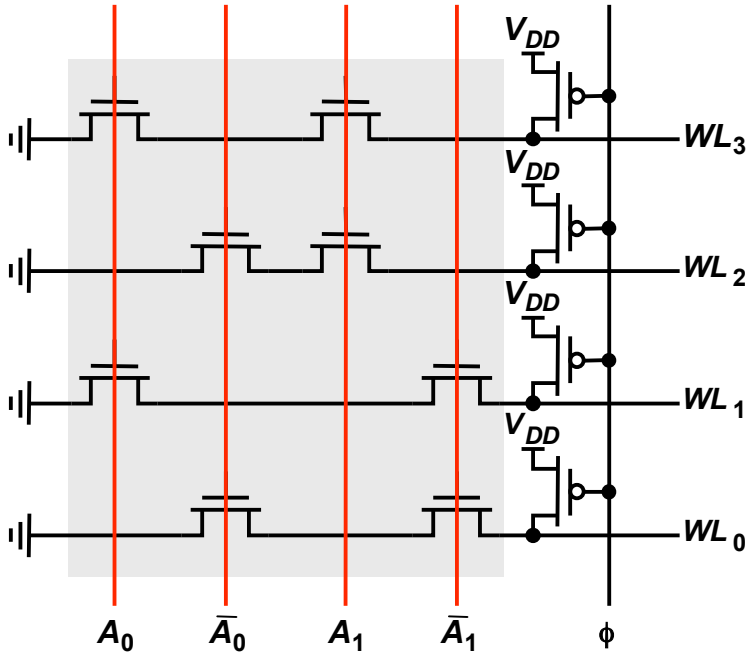
Dynamic Decoders



2-input NOR decoder



2-input NAND decoder

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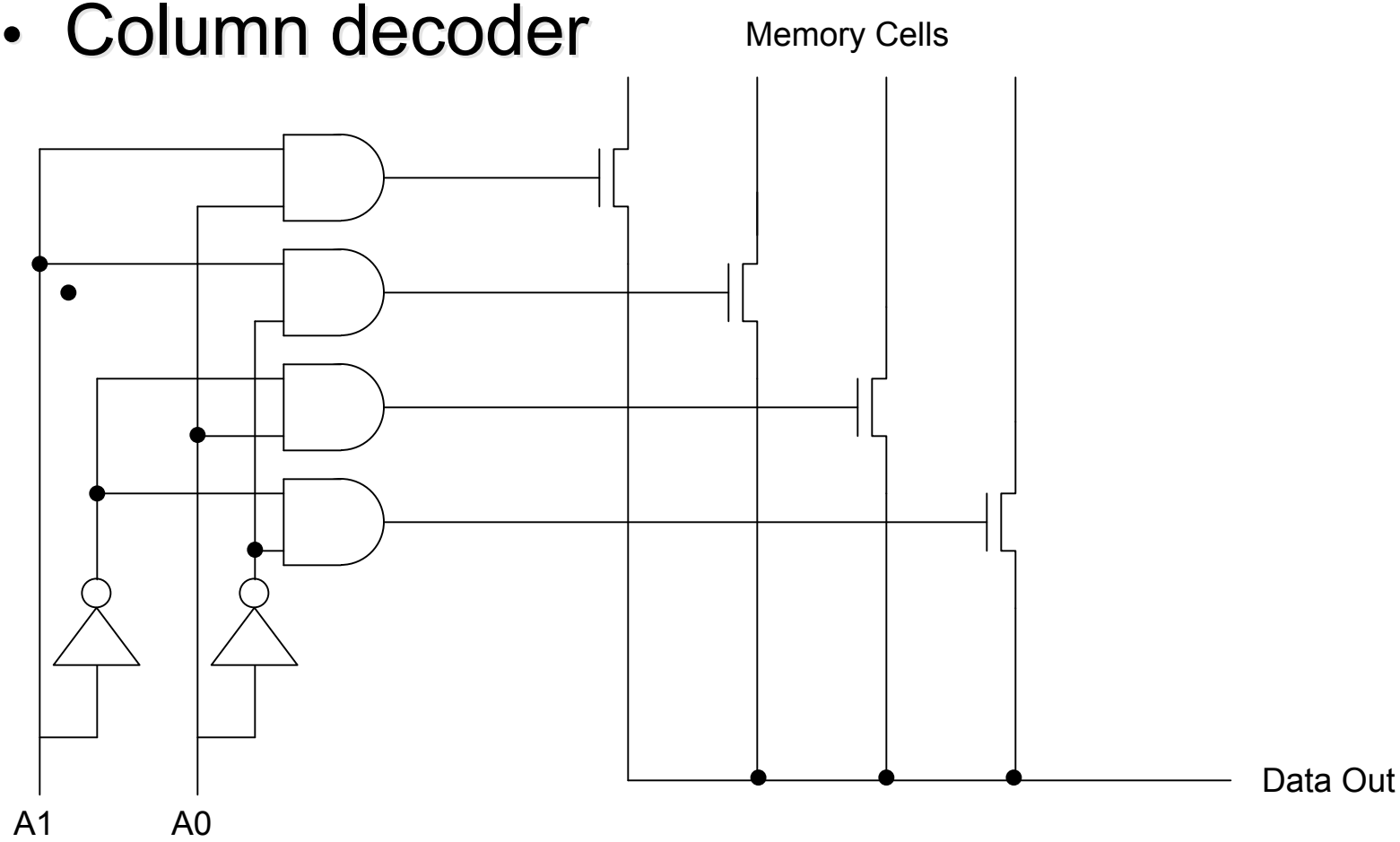
Memory Design

- Column decoder



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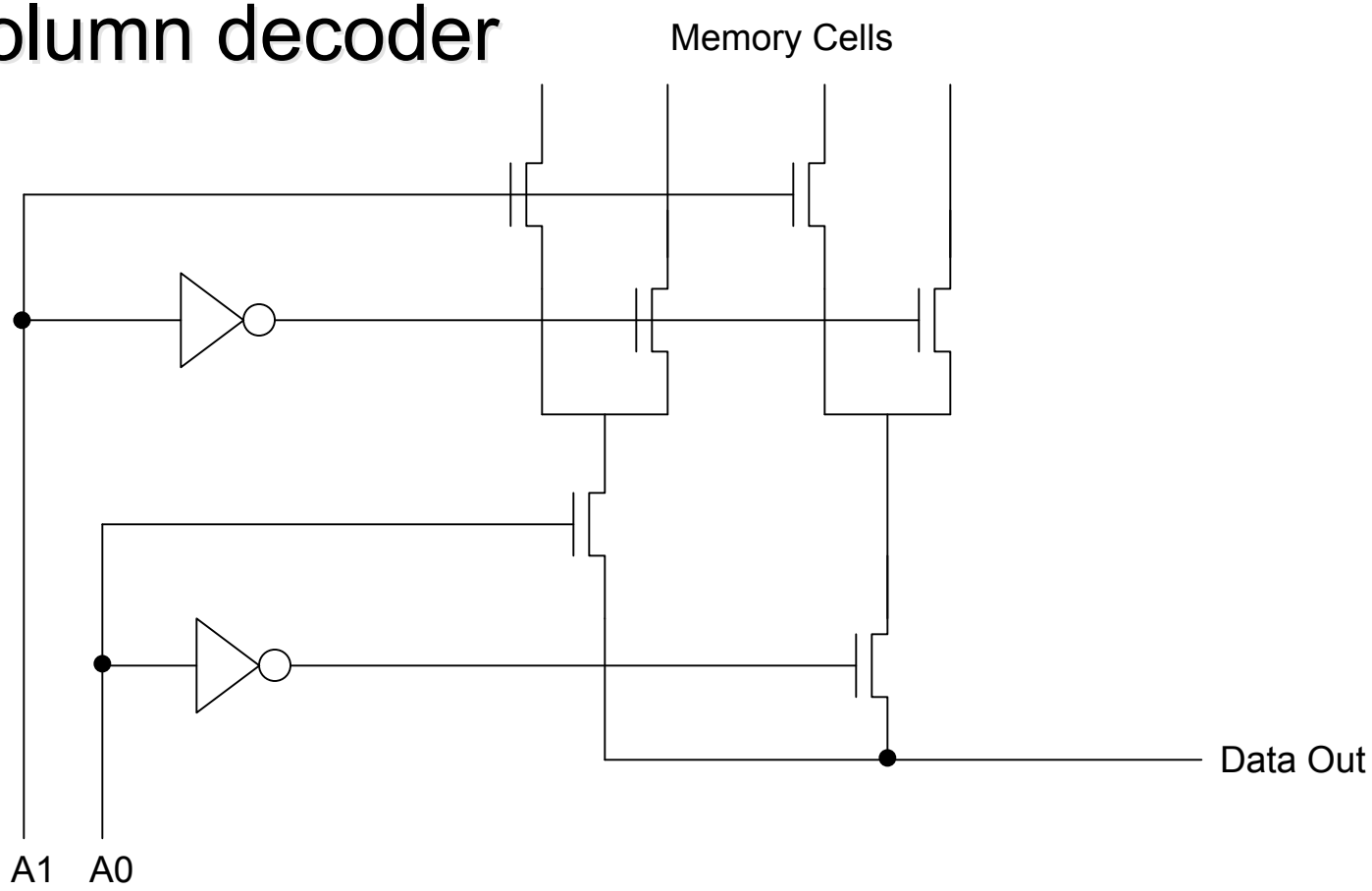
Memory Design

- Column decoder



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Memory Design

- Column decoder
  - AND-decoder based
    - On the order of $N \cdot 2^N$ transistors
  - Binary tree based
    - Slow because of the series of pass-transistors
  - Usually use a combination of the two

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Memory Design

- Sense Amplifier
  - Time to get through row decoder, column pull-down and column decoder can be very long
  - Use a sense amplifier to speed it up
    - Sense small differences in voltage and amplify it to rail voltage
    - Can be differential or single-ended
    - Usually use transistors with high threshold voltages

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Sense Amplifiers

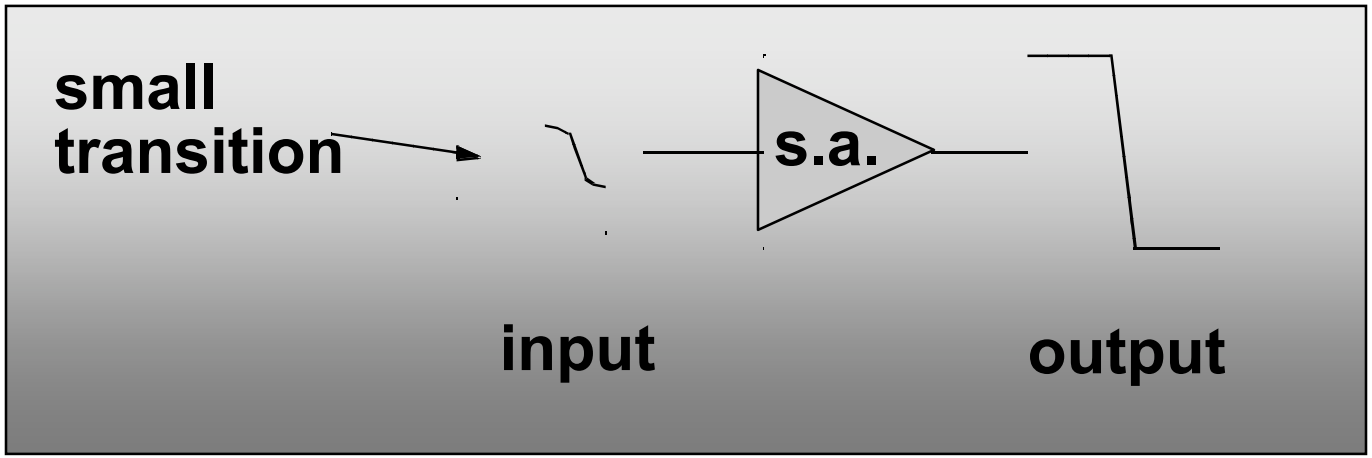
$$t_p = \frac{C \cdot \Delta V}{I_{av}}$$

make ΔV as small as possible

large

small

Idea: Use Sense Amplifer



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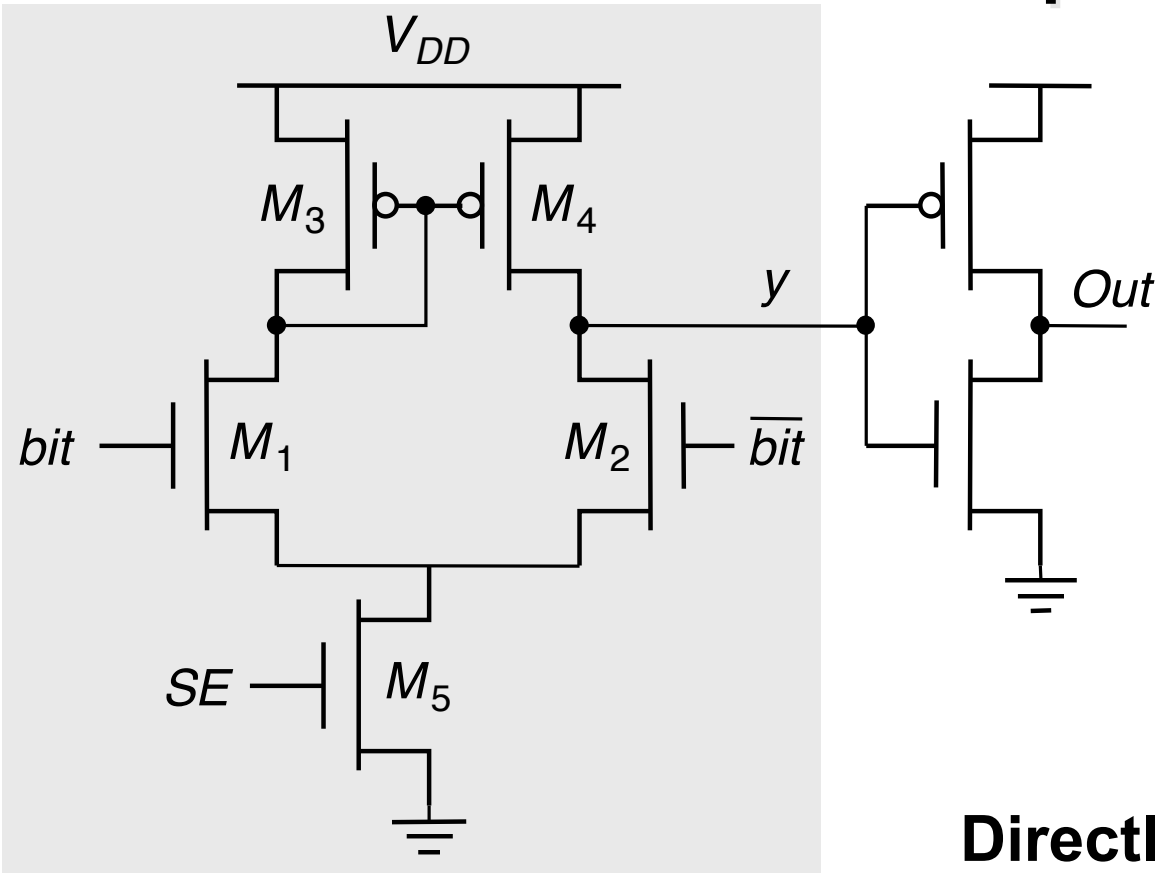
Differential Sense Amplifier



Directly applicable to SRAMs

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Next class

- Memory Reliability and Yield
- Control logic

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