Topics

- Memory Reliability and Yield
- Control Logic

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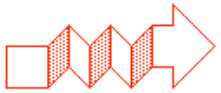
Reliability and Yield

- Semiconductor memories trade off noise-margin for density and performance



Highly Sensitive to Noise (Crosstalk, Supply Noise)

- High Density and Large Die size cause Yield Problems

$$Y = 100 \frac{Number\,of\,Good\,Chips\,on\,Wafer}{Number\,of\,Chips\,on\,Wafer}$$

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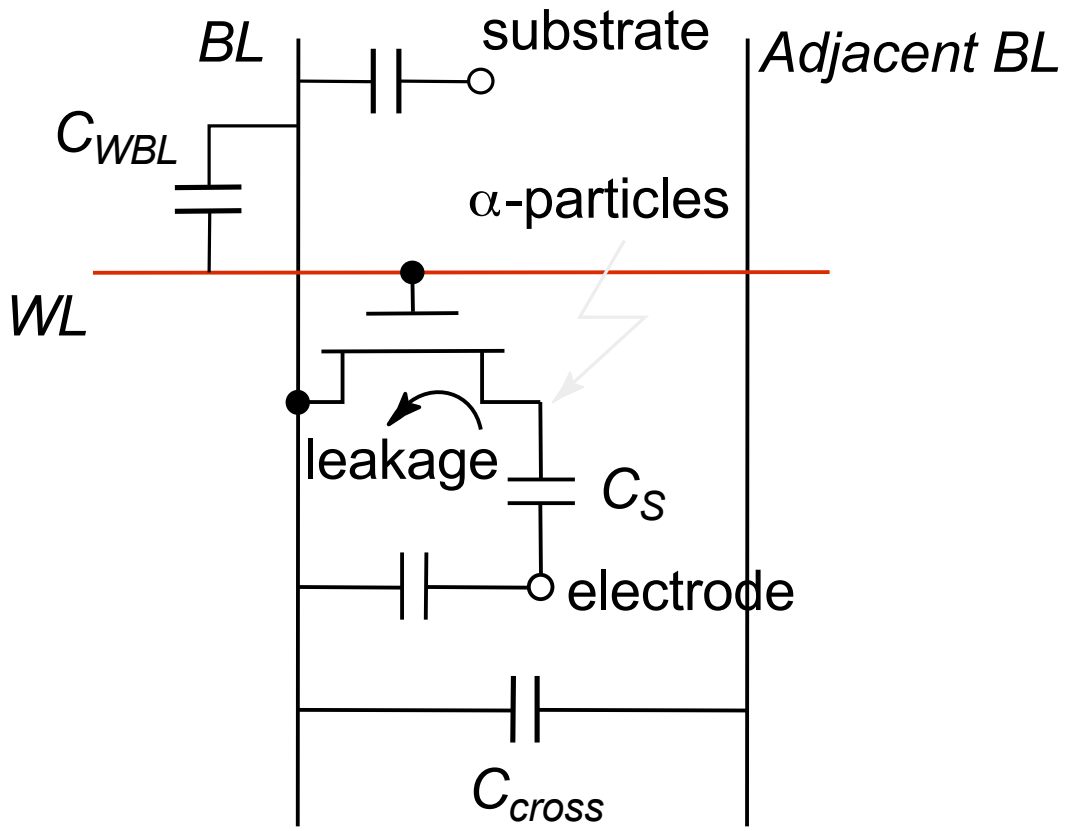
Noise Sources in 1T DRam



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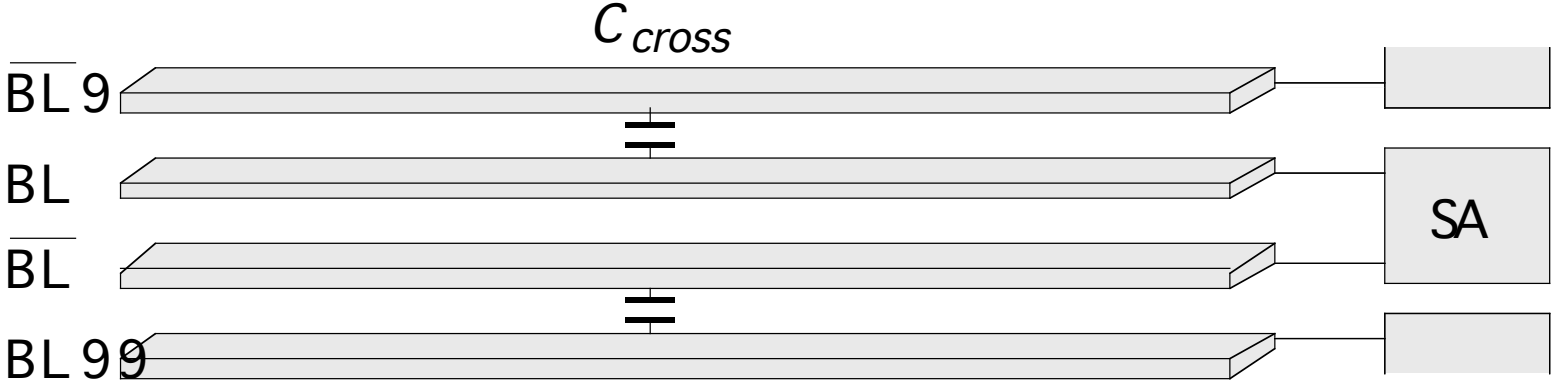
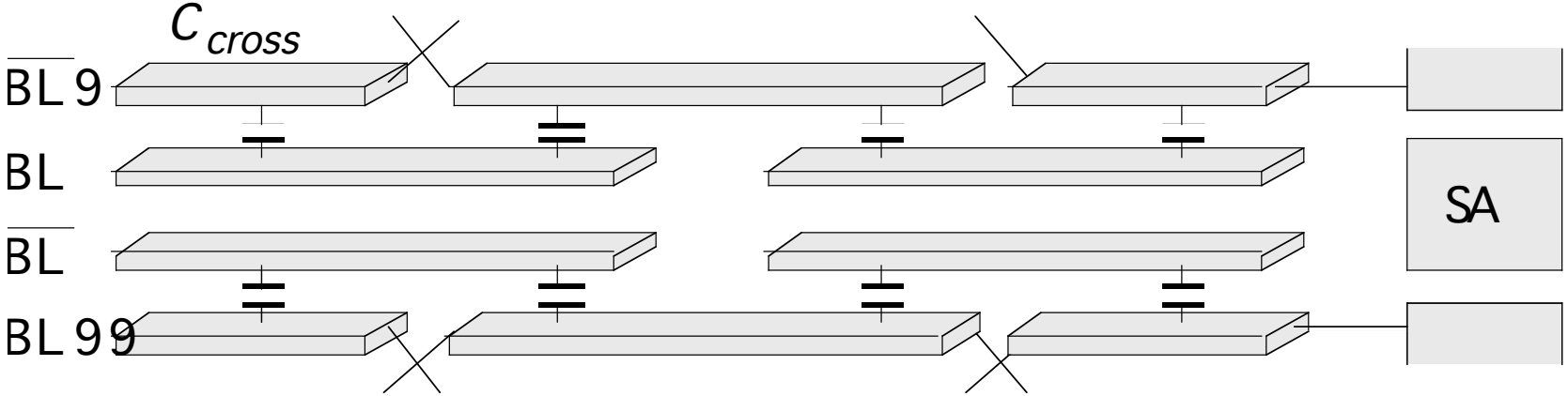
Transposed-Bitline Architecture



(a) Straightforward bit-line routing



(b) Transposed bit-line architecture

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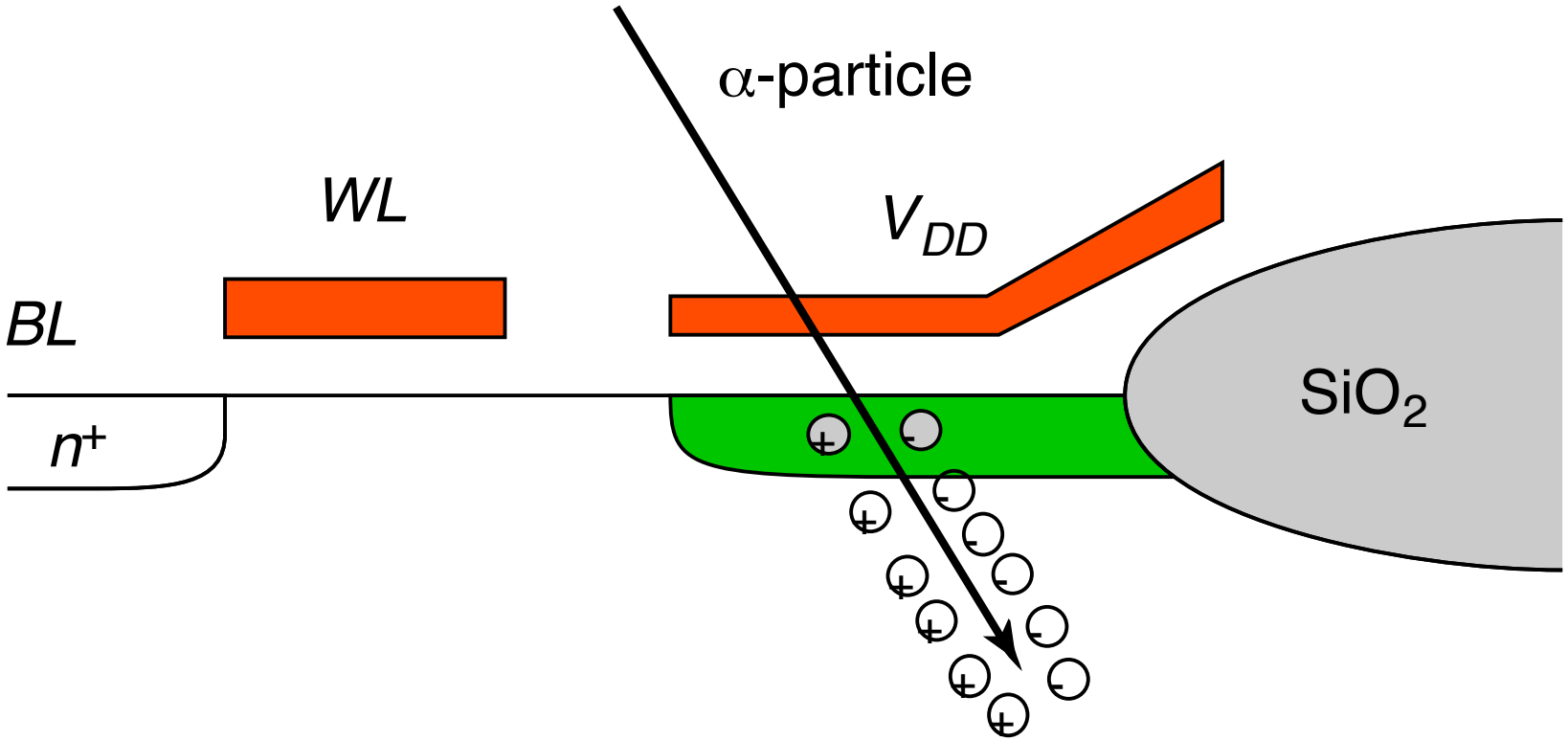
Alpha-particles (or Neutrons)



1 Particle ~ 1 Million Carriers

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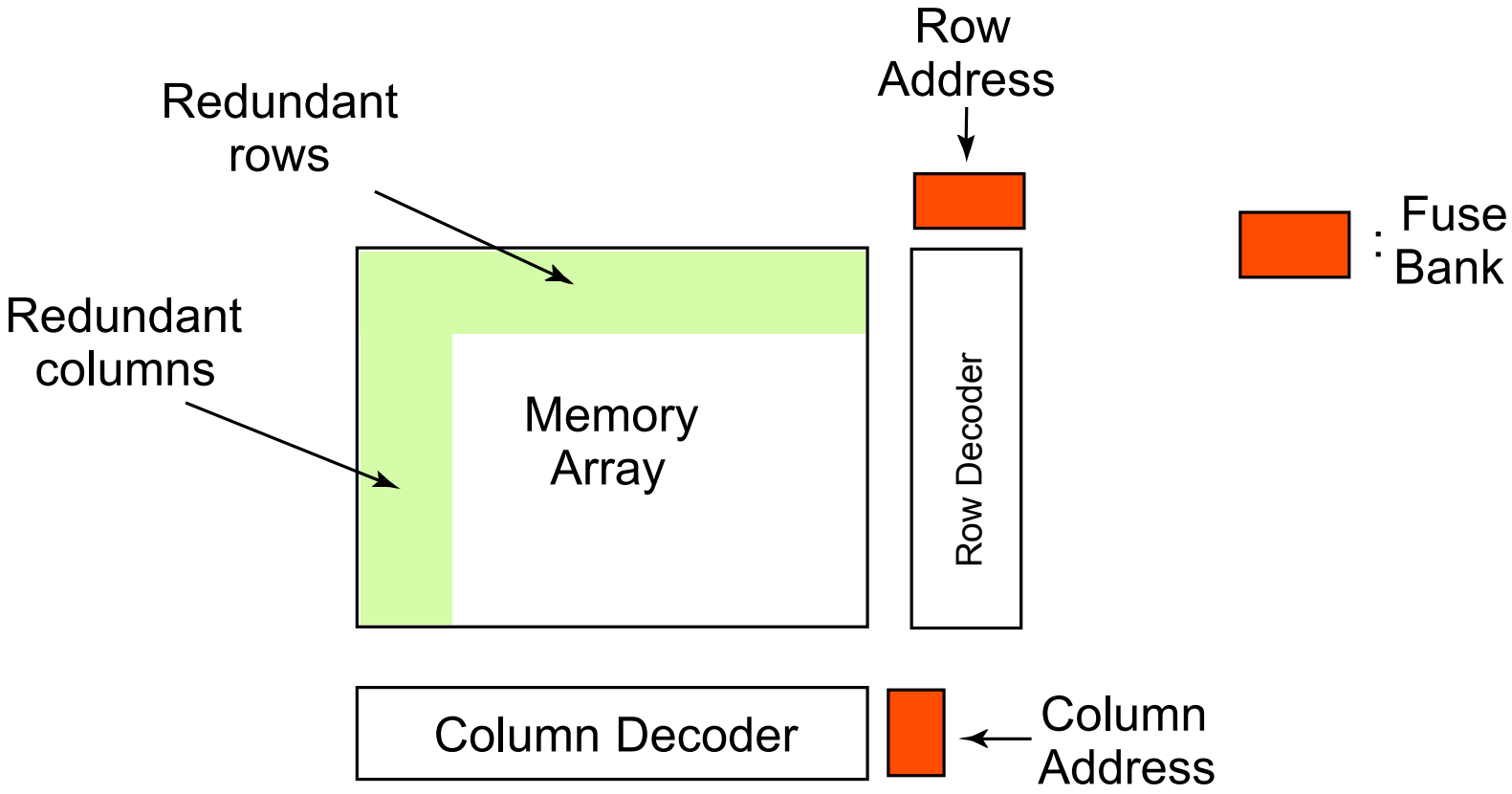
Redundancy



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Error-Correcting Codes

Example: Hamming Codes

$$P_1\, P_2\, B_3\, P_4\, B_5\, B_6\, B_7$$

with

$$P_1 \oplus B_3 \oplus B_5 \oplus B_7 = 0$$

$$P_2 \oplus B_3 \oplus B_6 \oplus B_7 = 0$$

$$P_4 \oplus B_5 \oplus B_6 \oplus B_7 = 0$$

e.g. B3 Wrong

1

1 **= 3**

0

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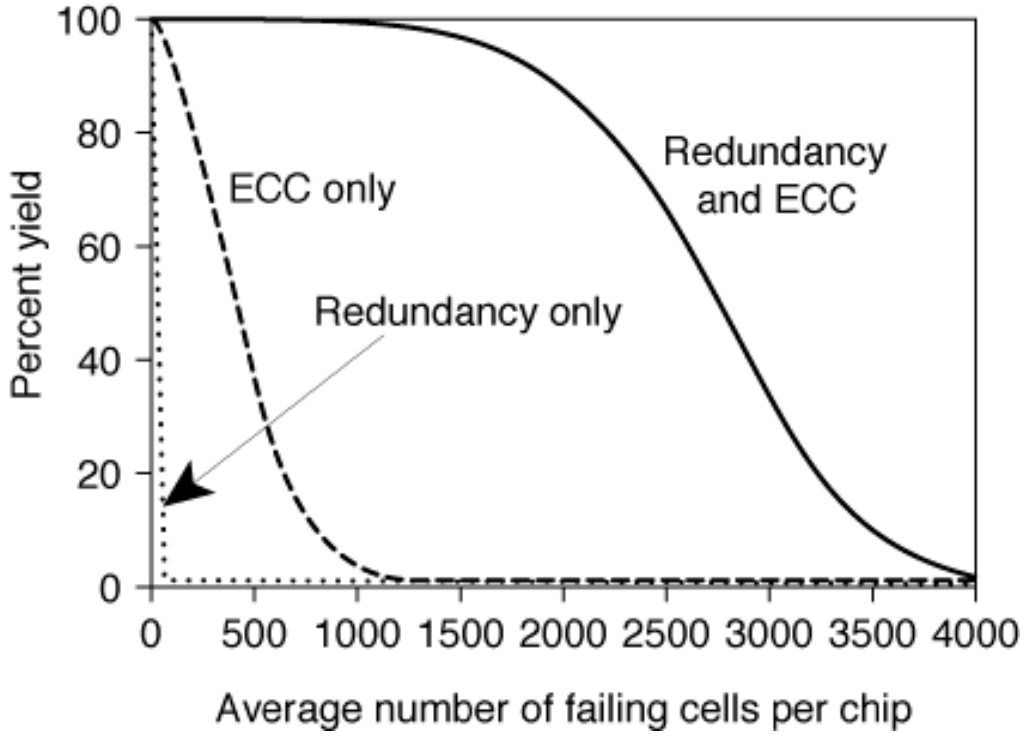
Redundancy and Error Correction

- 16Mbit DRAMs [Kalter90]



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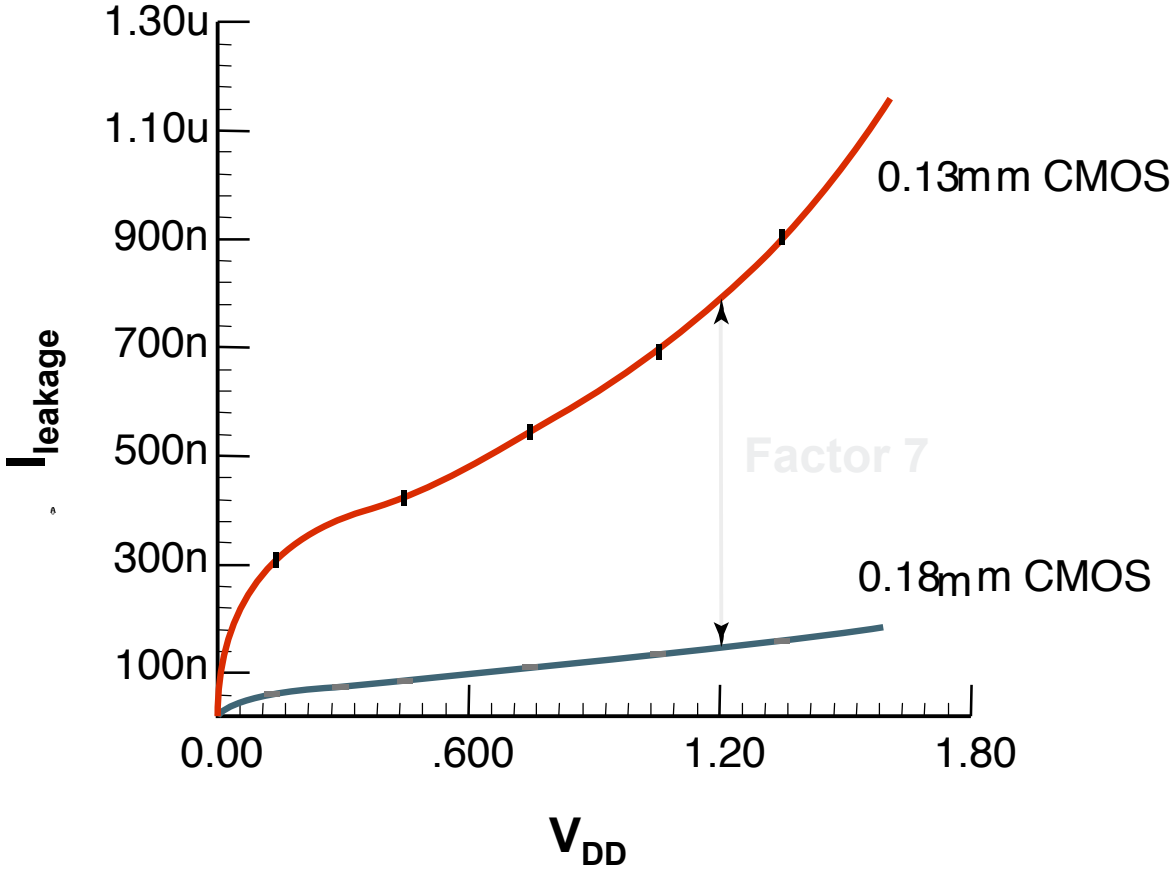
Data Retention in SRAM



SRAM leakage increases with technology scaling

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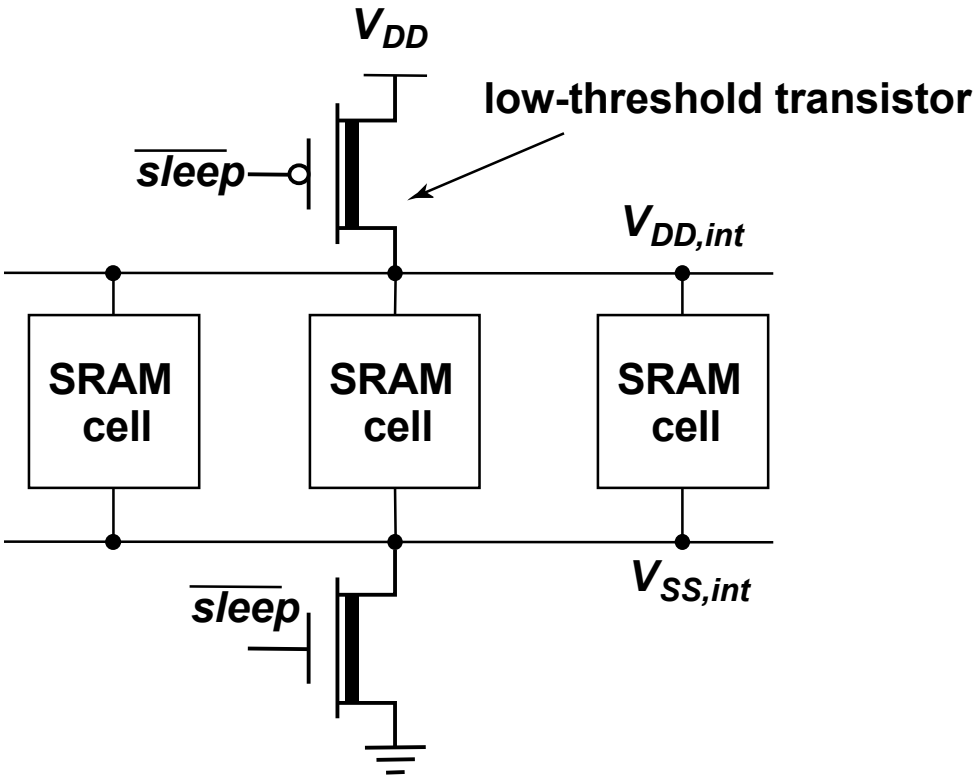
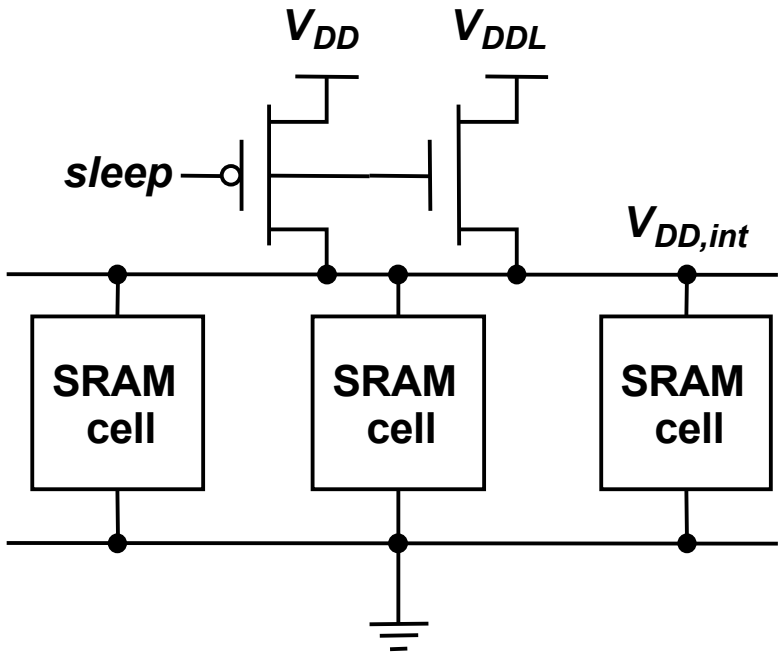
Suppressing Leakage in SRAM





Inserting Extra Resistance

Reducing the supply voltage

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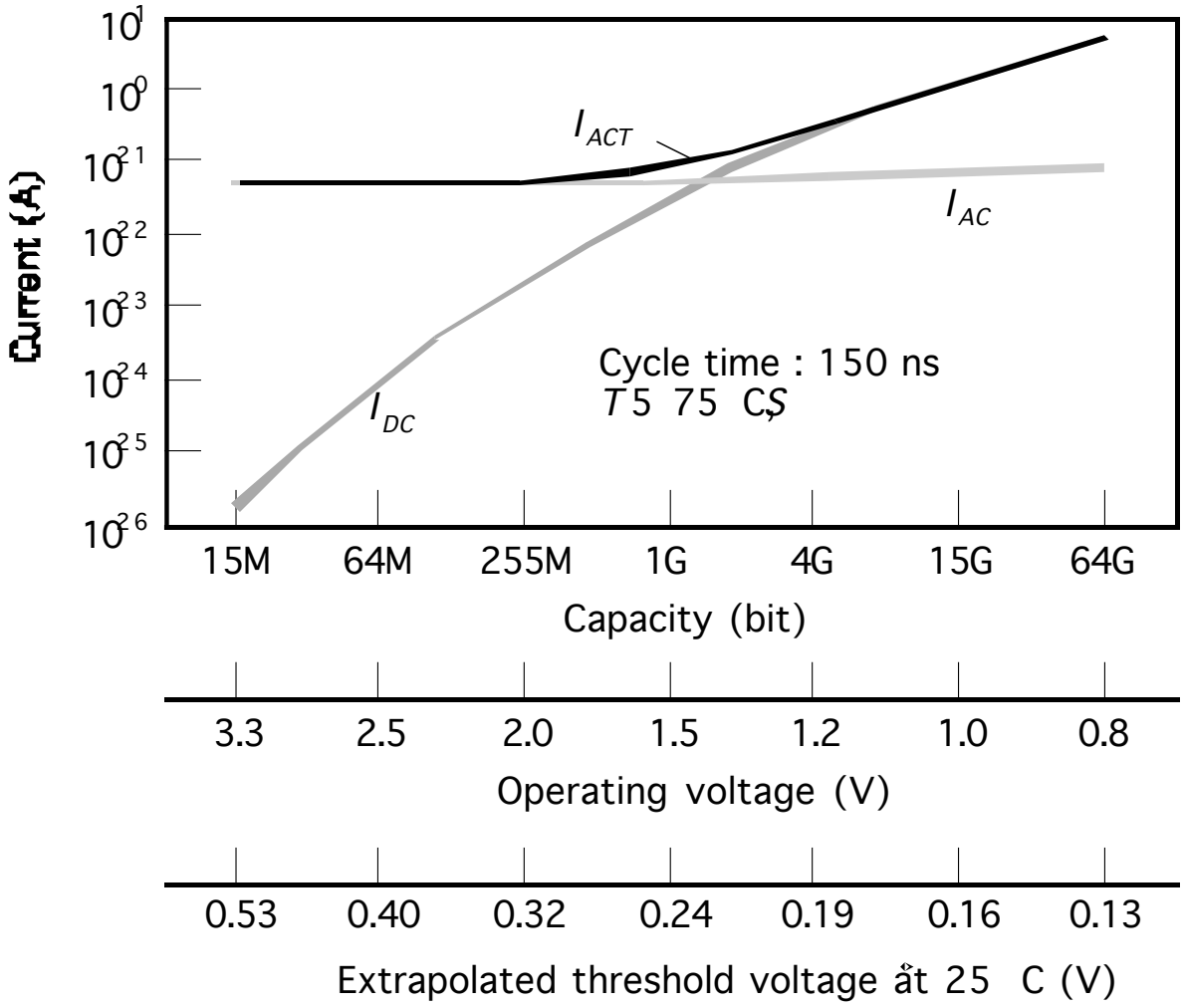
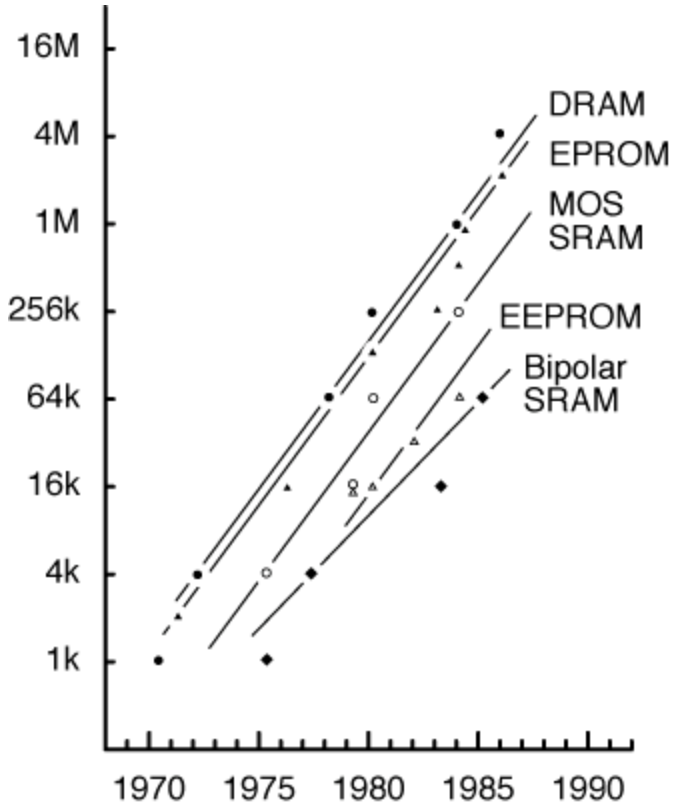
Data Retention in DRAM



From [Itoh00]

Semiconductor Memory Trends (up to the 90's)



Memory Size as a function of time: x 4 every three years

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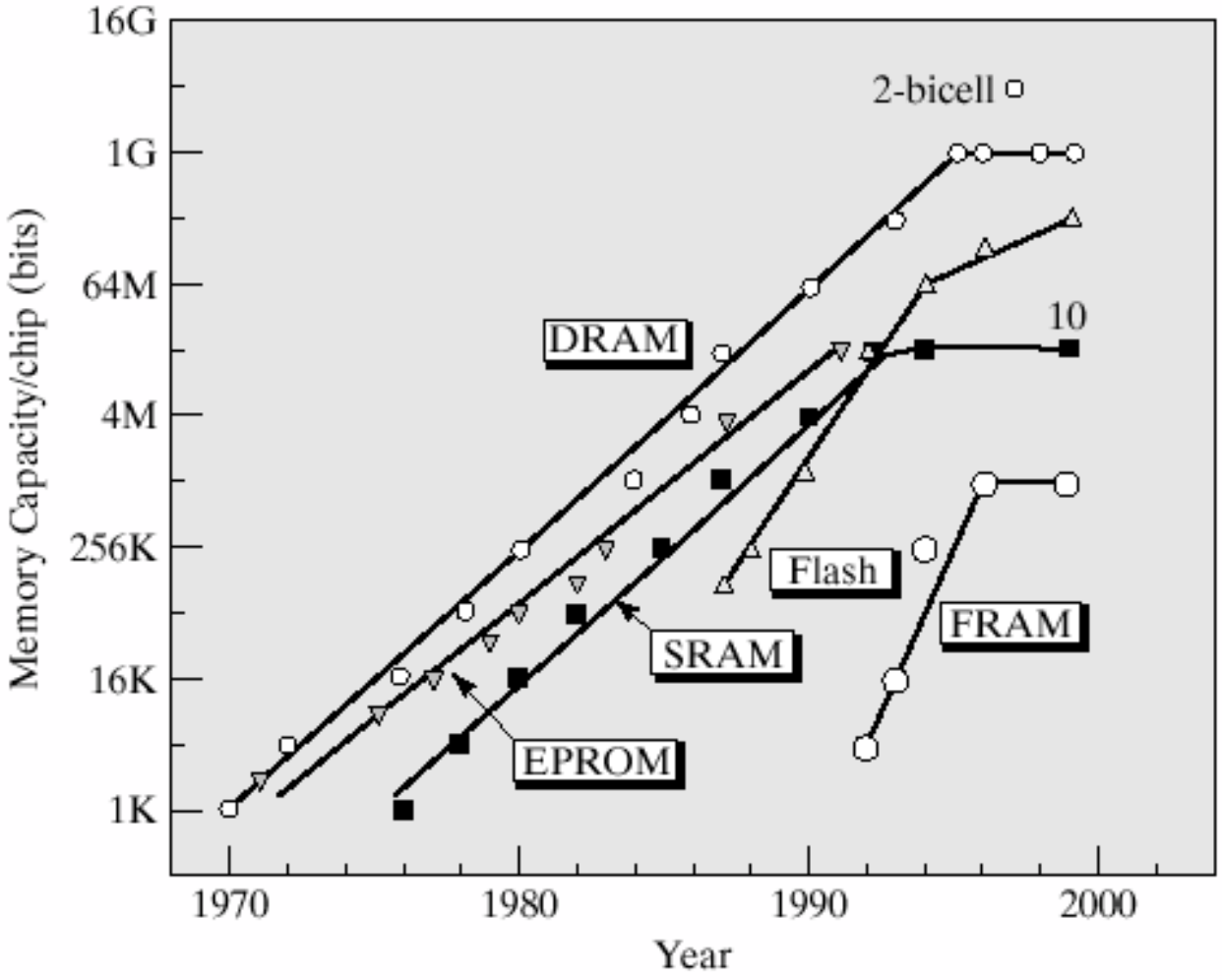
Semiconductor Memory Trends (updated)



From [Itoh01]

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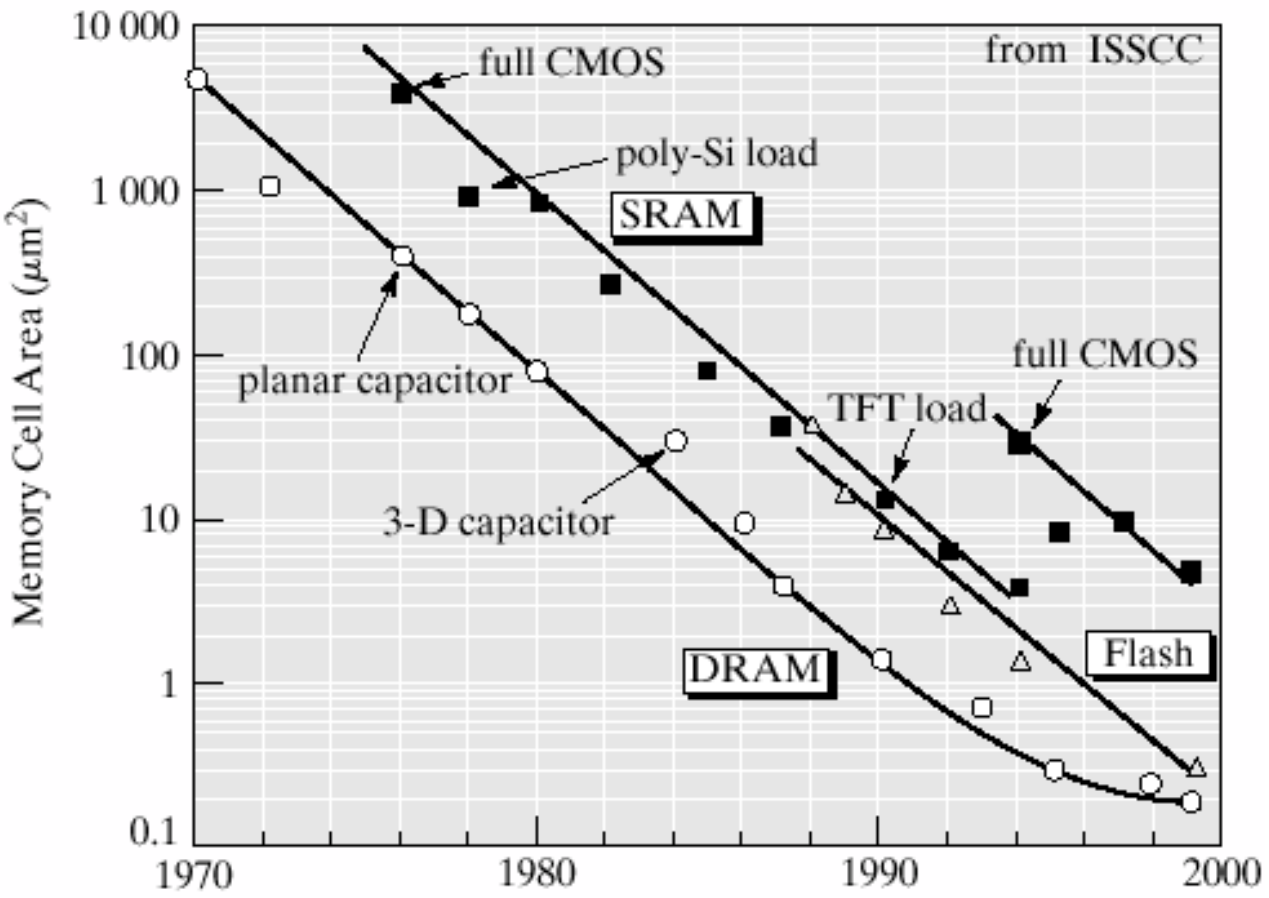
Trends in Memory Cell Area



From [Itoh01]

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Control Logic

- Finite State Machines
- Logic Implementations
  - PLA
  - ROM
  - Multilevel Logic

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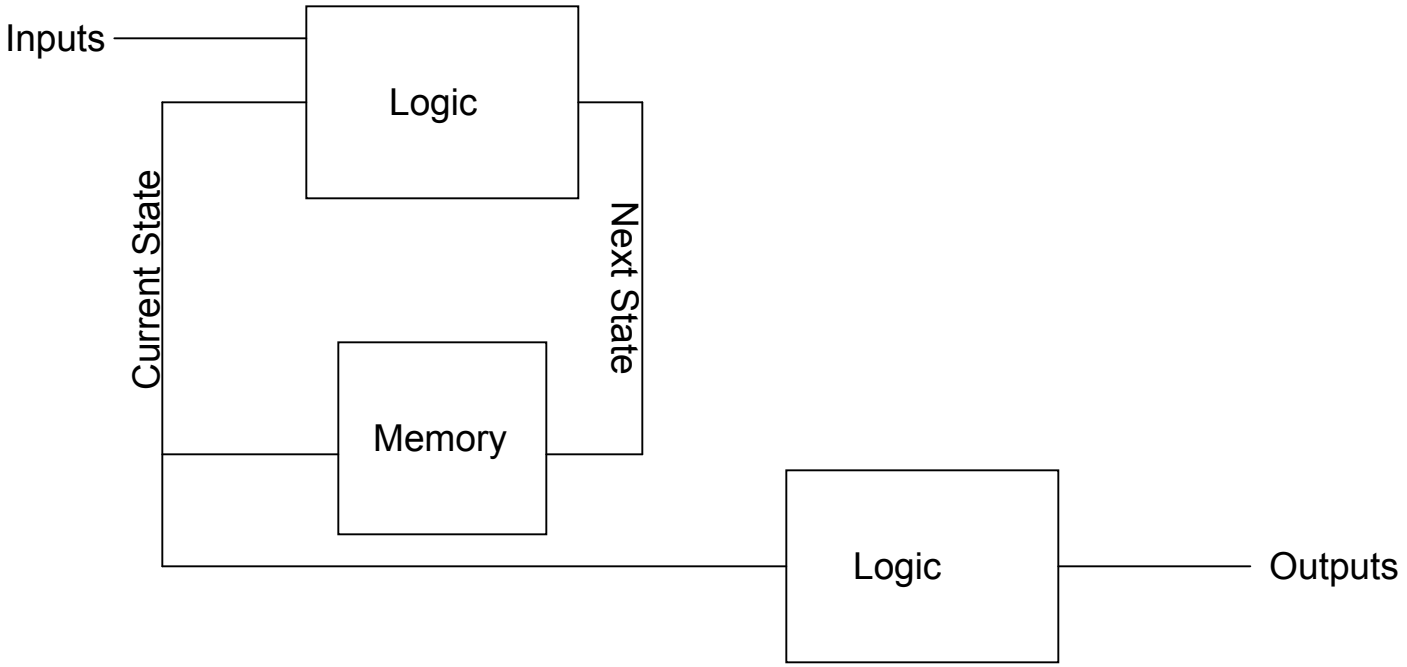
State Machines

- Moore Machine
  - Outputs are dependent only on current state



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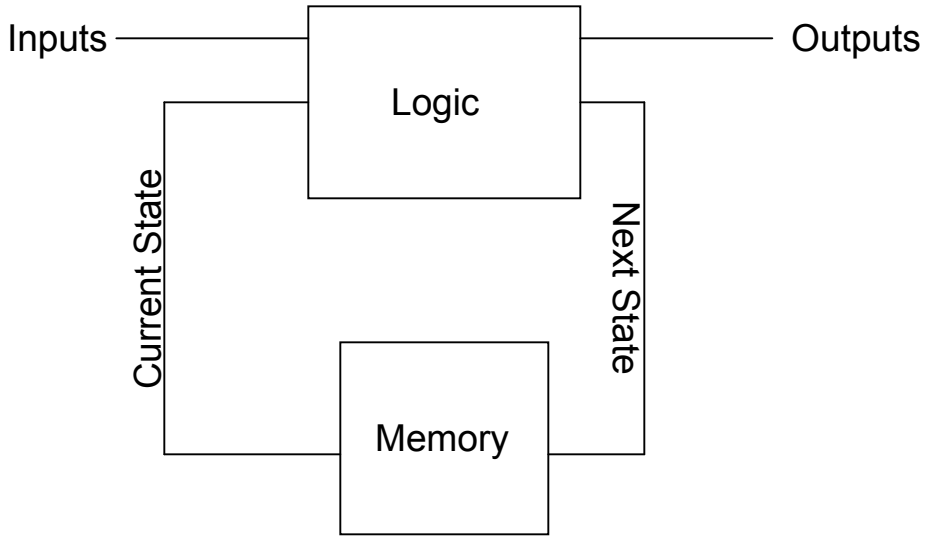
State Machines

- Mealy Machine
  - Outputs are dependent on current state and inputs



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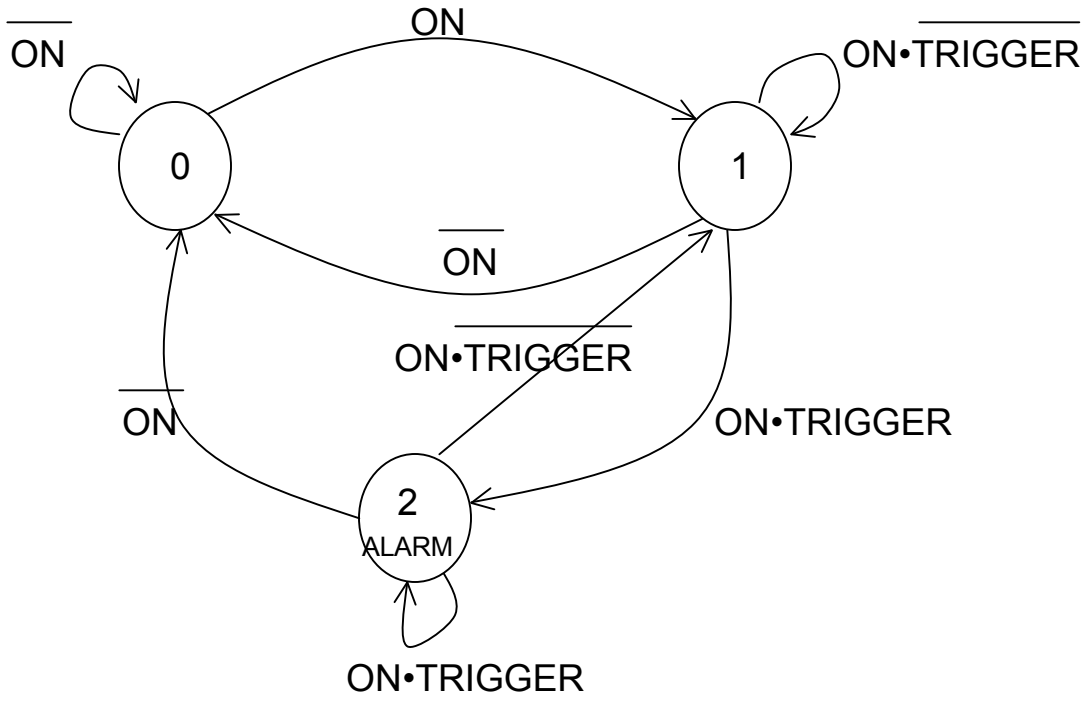
State Machine Design

- Moore Machine



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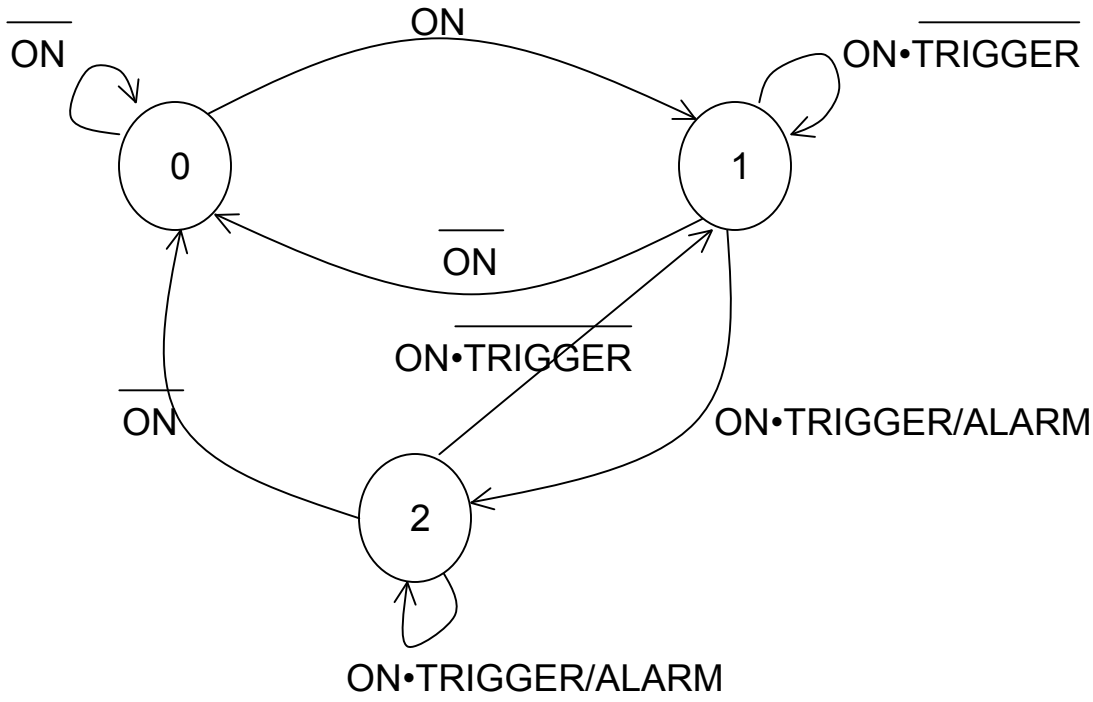
State Machine Design

- Mealy Machine



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State Machine Design

S1	S0	ON	TRIGGER	NS1	NS0	ALARM
0	0	0	X	0	0	0
0	0	1	X	0	1	0
0	1	0	X	0	0	0
0	1	1	0	0	1	0
0	1	1	1	1	0	0
1	0	0	X	0	0	1
1	0	1	0	0	1	1
1	0	1	1	1	0	1
1	1	X	X	X	X	X

$$NS0 = ON \cdot \overline{TRIGGER} + \overline{S1} \cdot \overline{S0} \cdot ON$$

$$NS1 = S1 \cdot ON \cdot TRIGGER + S0 \cdot ON \cdot TRIGGER$$

$$ALARM = S1 \cdot \overline{S0}$$

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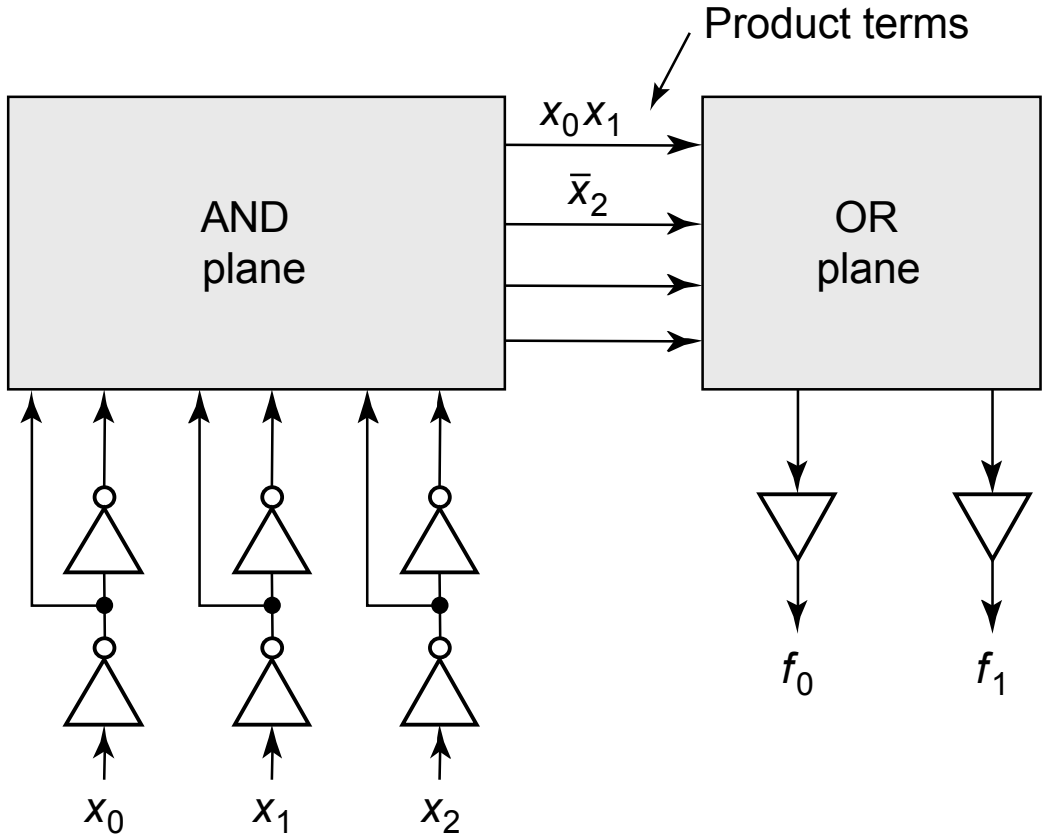
Programmable Logic Array



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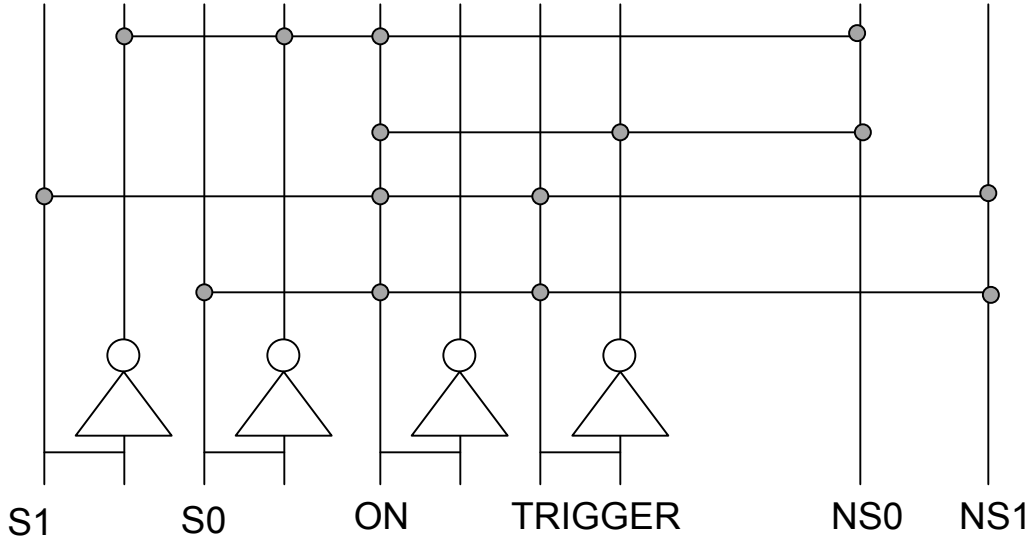
PLA Design

$$NS0 = ON \cdot \overline{TRIGGER} + \overline{S1} \cdot \overline{S0} \cdot ON$$

$$NS1 = S1 \cdot ON \cdot TRIGGER + S0 \cdot ON \cdot TRIGGER$$



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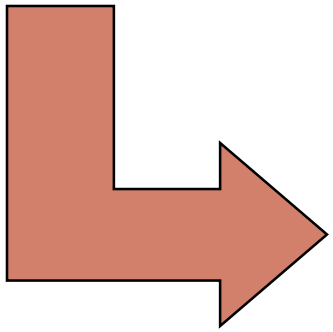
Two-Level Logic

Every logic function can be expressed in sum-of-products format (AND-OR)

$$f_0 = x_0 x_1 + \overline{x_2}$$

$$f_1 = x_o x_1 x_2 + \overline{x_2} + \overline{x_0} x_1$$

minterm



Inverting format (NOR-NOR) more effective

$$\overline{f_0} = \overline{\overline{(\overline{x_0} + \overline{x_1})} + \overline{x_2}}$$

$$\overline{f_1} = \overline{\overline{(\overline{x_0} + \overline{x_1} + \overline{x_2})} + \overline{x_2} + \overline{(x_0 + \overline{x_1})}}$$

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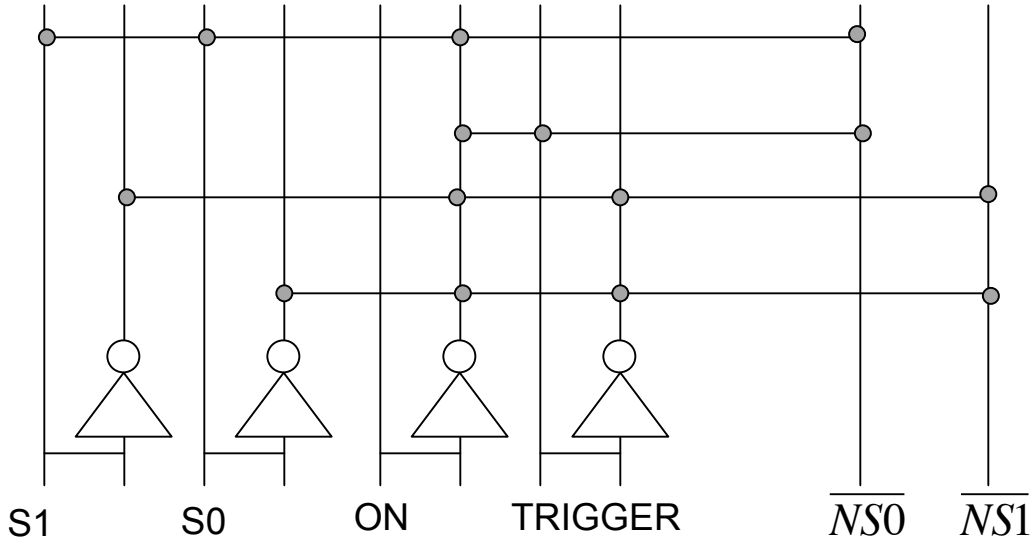
PLA Design

$$\overline{NS0} = \overline{\overline{ON} + TRIGGER + S1 + S0 + \overline{ON}}$$

$$\overline{NS1} = \overline{\overline{S1} + \overline{ON} + \overline{TRIGGER} + \overline{S0} + \overline{ON} + \overline{TRIGGER}}$$



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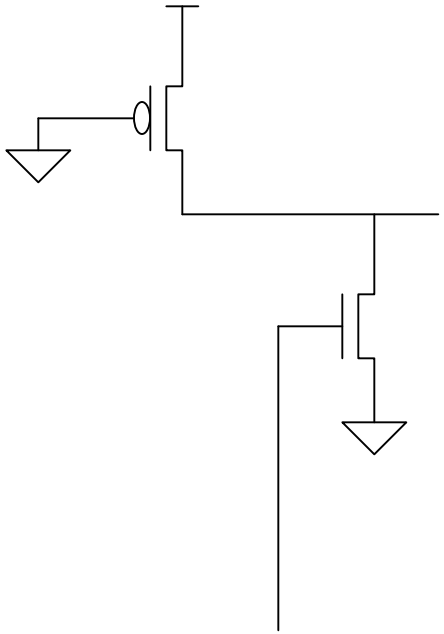
PLA Design



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PLA versus ROM

❑ Programmable Logic Array

structured approach to random logic
"two level logic implementation"
- **NOR-NOR (product of sums)**
- **NAND-NAND (sum of products)**

IDENTICAL TO ROM!

❑ Main difference

ROM: fully populated
PLA: one element per minterm

Note: Importance of PLA's has drastically reduced
1. **slow**
2. **better software techniques (mutli-level logic synthesis)**

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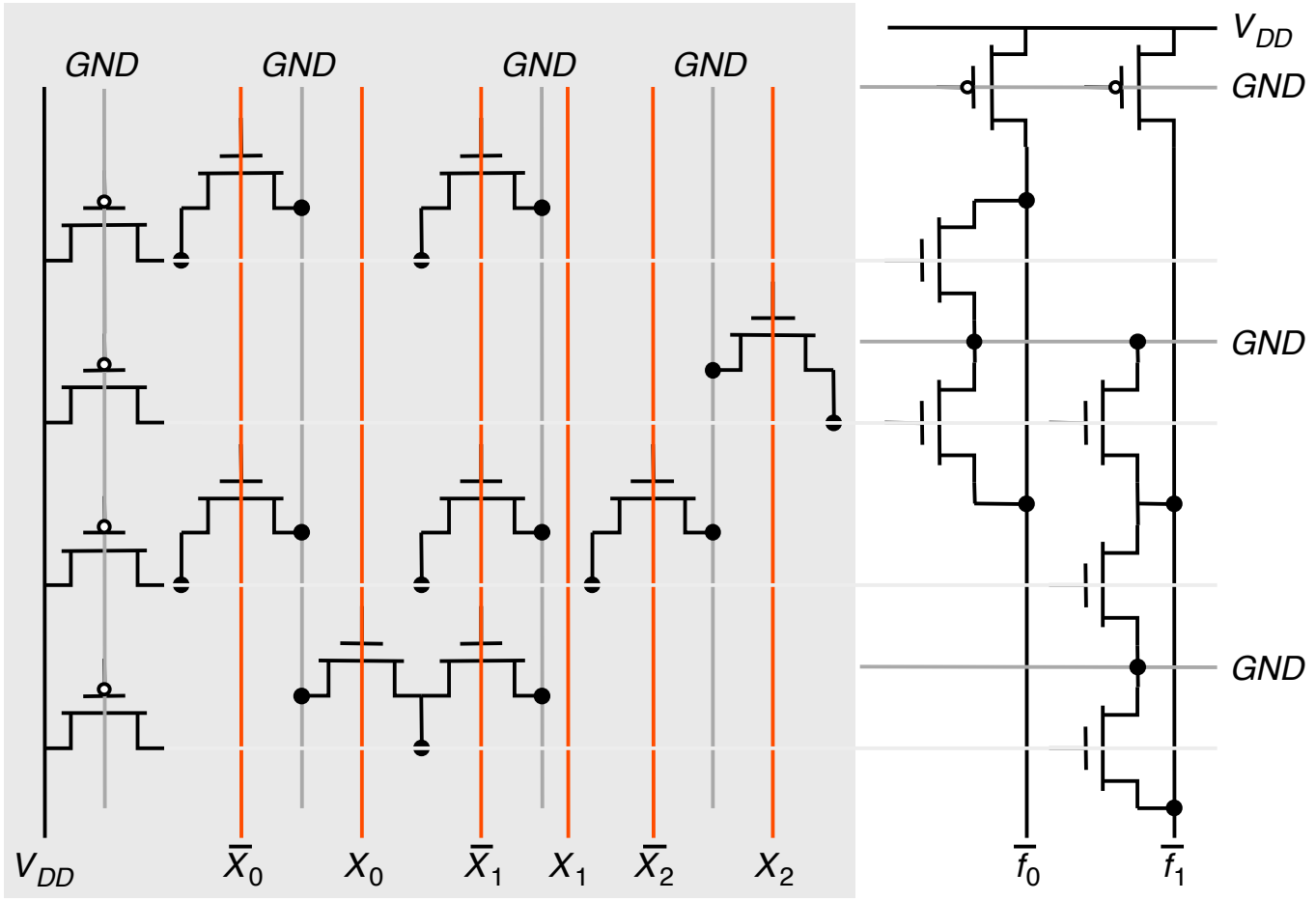
Programmable Logic Array

Pseudo-NMOS PLA



AND-plane **OR-plane**

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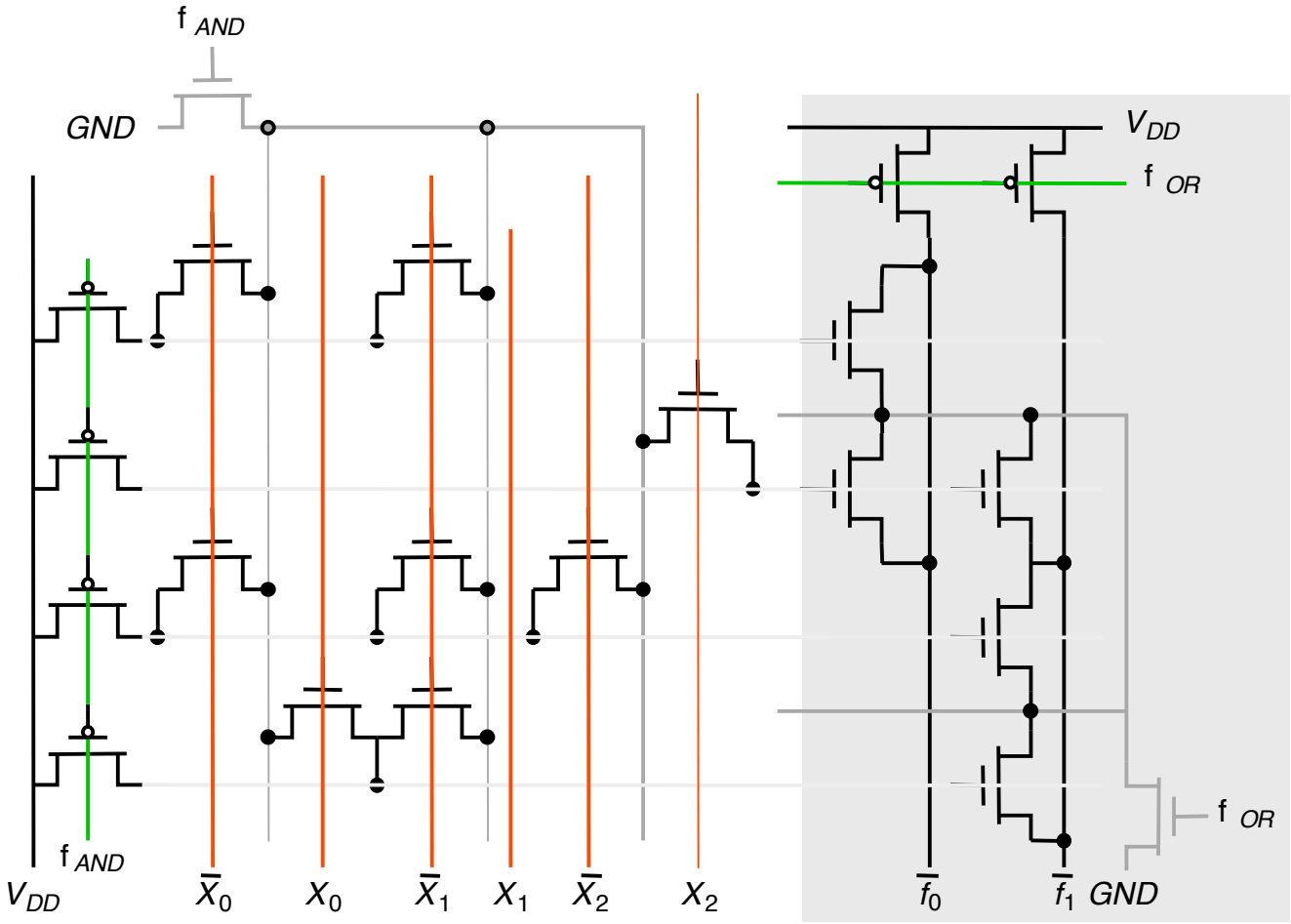
Dynamic PLA



AND-plane **OR-plane**

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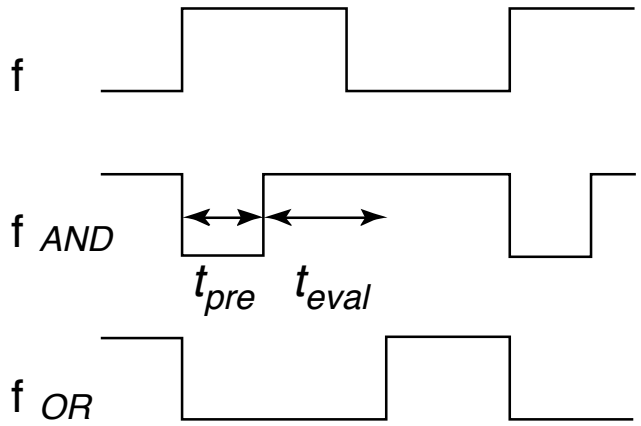
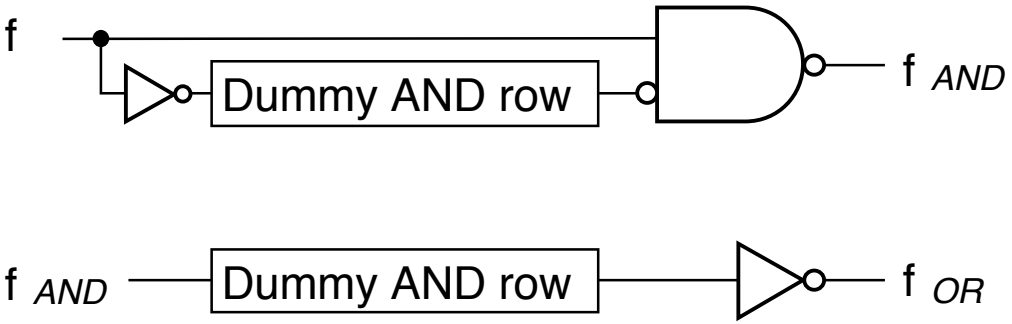
Clock Signal Generation for self-timed dynamic PLA



(a) Clock signals



(b) Timing generation circuitry

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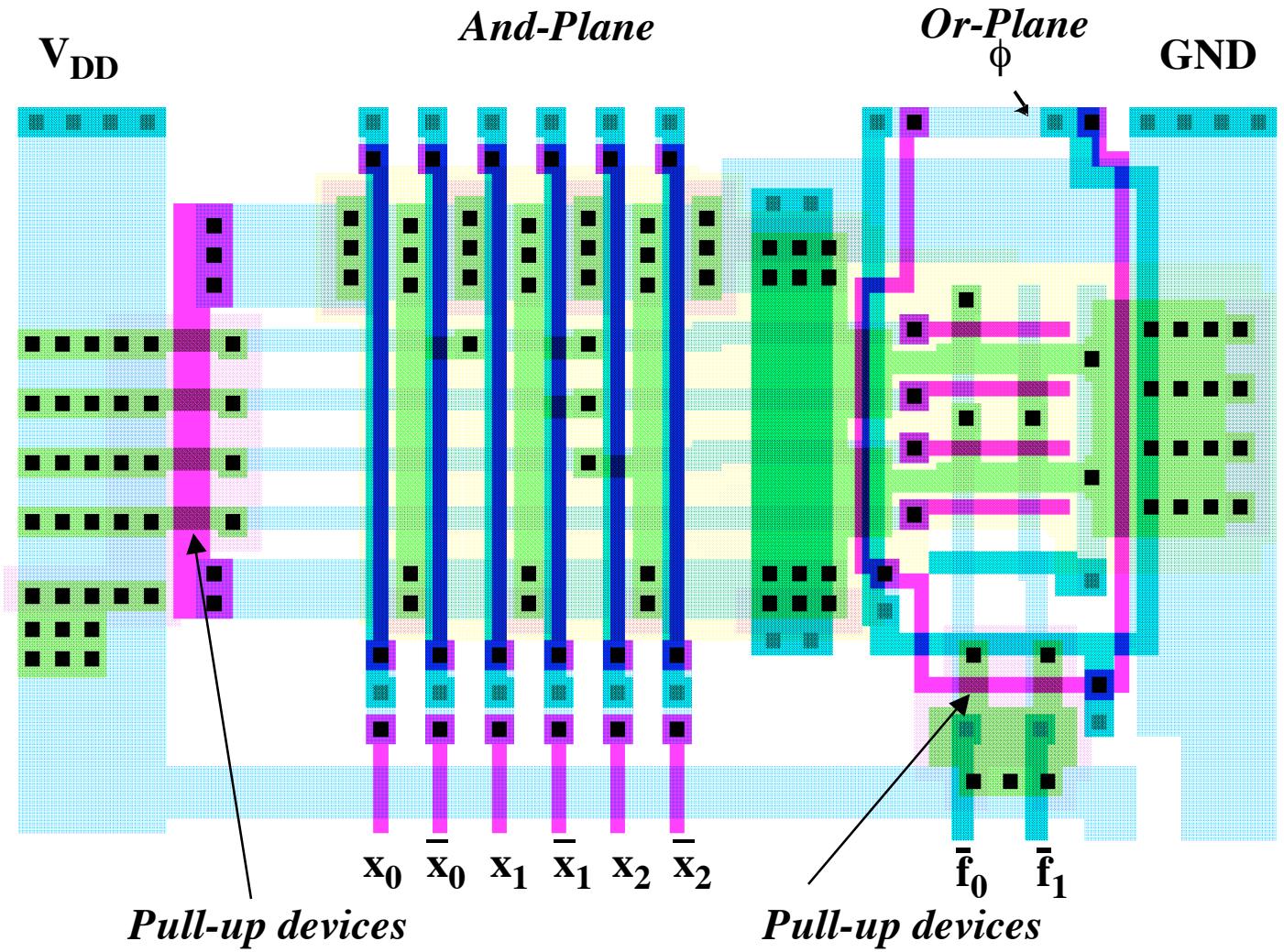
PLA Layout



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State Machine Design

- Other Control Implementation
  - Microcode (ROM)
  - Multilevel Logic

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Next class

- HW5 due March 29th
- Clocking
- Read Chapter 10

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