Topics

– Verification and Test

Parts of this lecture were adapted from Bushnell and Agrawal testing class notes, Rutgers University

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Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

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Verification and Testing

- 2 types of errors that we need to test for
  - Design defects (verification)
    - Logic Design
    - Schematic
    - Layout
  - Manufacturing defects (testing)
    - Permanent faults
    - Transient faults
    - Aging faults

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Verification vs. Test

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

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Design Defects

- Testing using simulation
  - Verification of design
  - Usually design to schematic/layout transition is defect-free if using automated tools
- Testing using functional verification
  - Much more difficult problem, but potentially faster
- Performance simulation
- Full system simulation - e.g. boot up an OS on a processor in the simulator
- *"If you don't test it, it doesn't work"*

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Manufacturing defects

- Physical Defects
  - Silicon substrate defects
  - Mask contamination
  - Photolithographic errors
  - Oxide abnormalities

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Manufacturing defects

- Electrical Faults
  - Shorts
  - Opens
  - Transistor stuck-on
  - Excess resistance
  - Excess current

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Manufacturing defects

- Logical Faults
  - Stuck-at-0
  - Stuck-at-1
  - Delay fault
  - Bridging fault

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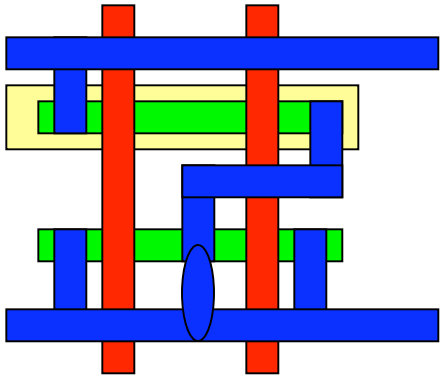
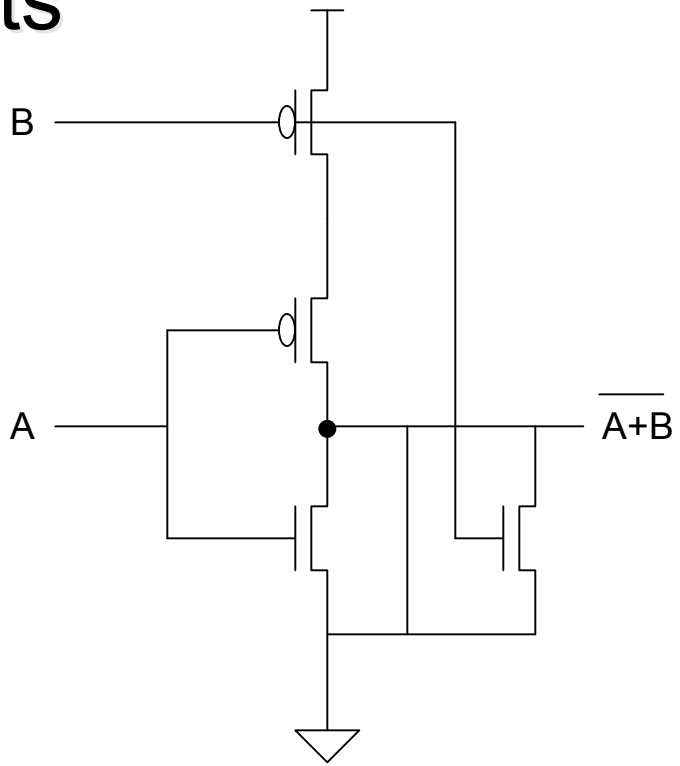
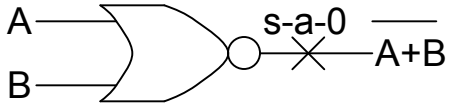
Manufacturing defects







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Manufacturing defects

- Wafer-level probe testing
  - Most manufacturing defects are caught at this point
- Package level testing
  - Pin-Pad bond faults
  - Damage due to handling
  - Performance related errors

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Manufacturing defects

- Board-level probe testing
  - Package damage
  - Infant mortality
  - Burn-in testing
- User testing
  - Transient faults
  - Defects that appear due to aging
    - Metal migration
    - Device Breakdown
  - Environmental errors

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Sub-types of Tests

- ***Parametric*** **– measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap**
- ***Functional*** **– used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive**

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Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

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Real Tests

- Based on analyzable fault models, which may not map to real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

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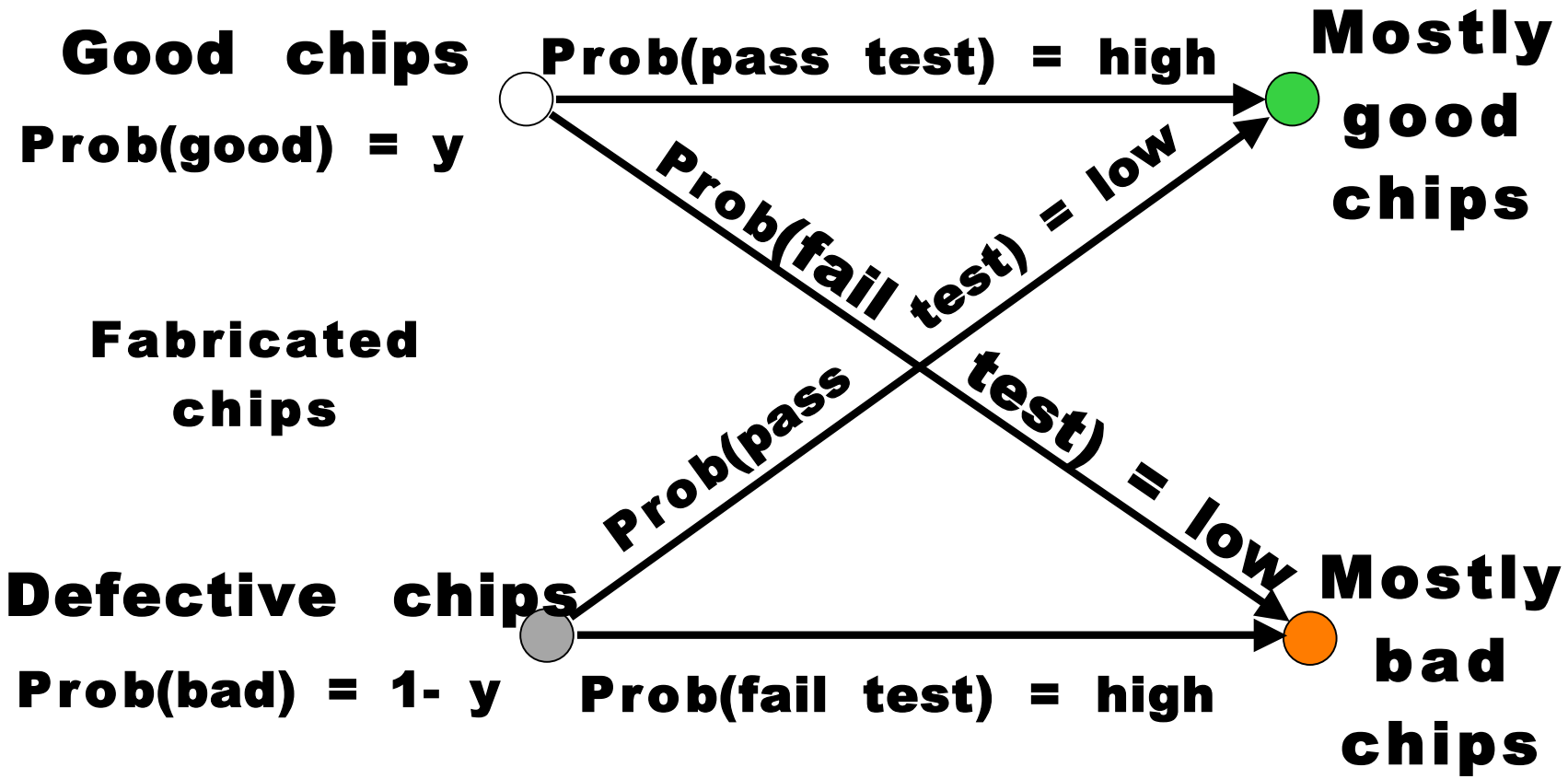
Testing as Filter Process



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Test Generation

- N inputs - 2^N test vectors
- Testers are not fast - 1us per vector
- 32 inputs can take over an hour
- 64 inputs can take over a million years
- Solutions
  - At-speed testing
  - Intelligent test pattern selection
- Single-stuck-at fault model
  - Covers most cases

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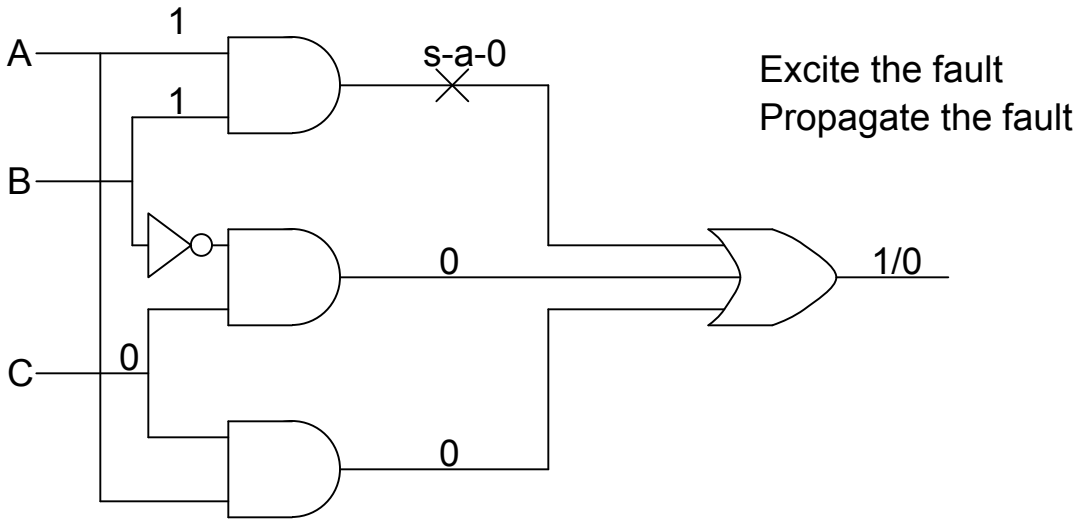
Test Generation



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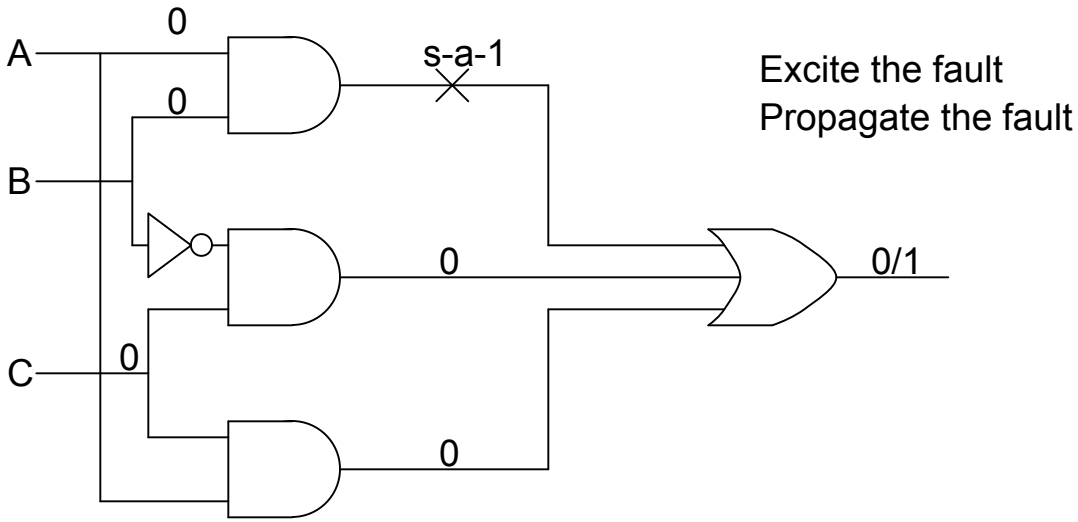
Test Generation



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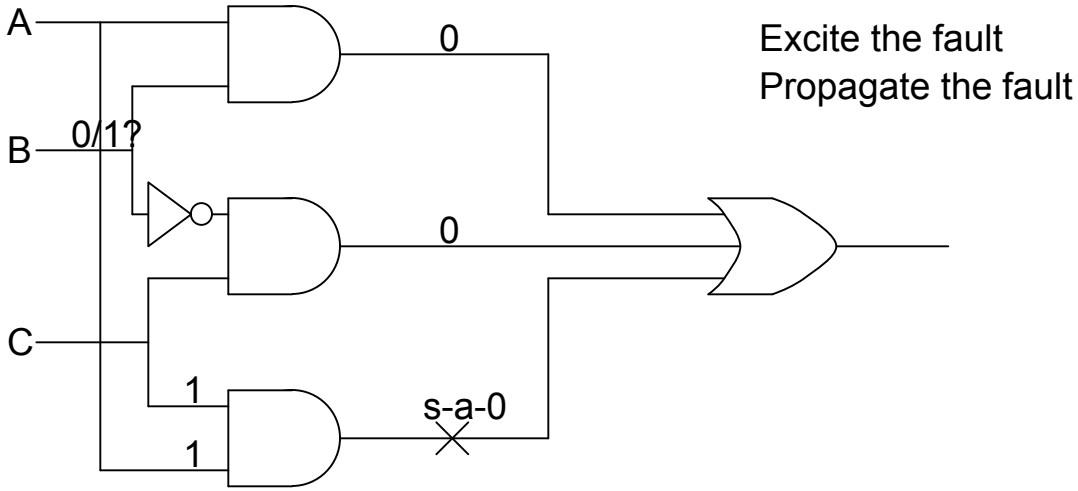
Test Generation

- Untestable faults because of redundancy



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Costs of Testing

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

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LTX FUSION HF ATE

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Cost of Manufacturing Testing in 2000

- 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price
  - = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = $0.854M + $0.085M + $0.5M
  - = $1.439M/year
- Test cost (24 hour ATE operation)
  - = $1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

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Roles of Testing

- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

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Fault Diagnosis

- Once you've determined there is a fault, can you isolate where the fault is?
- Useful for repair - but not always practical, because of the expense of repairing wafers
- Can be used to activate redundant circuitry if present

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Design for Testability

- Sequential circuit initialization
- Ability to disable clock
- Remove redundancies
- No asynchronous logic
- No delay-dependent logic
- Introduce more observability points

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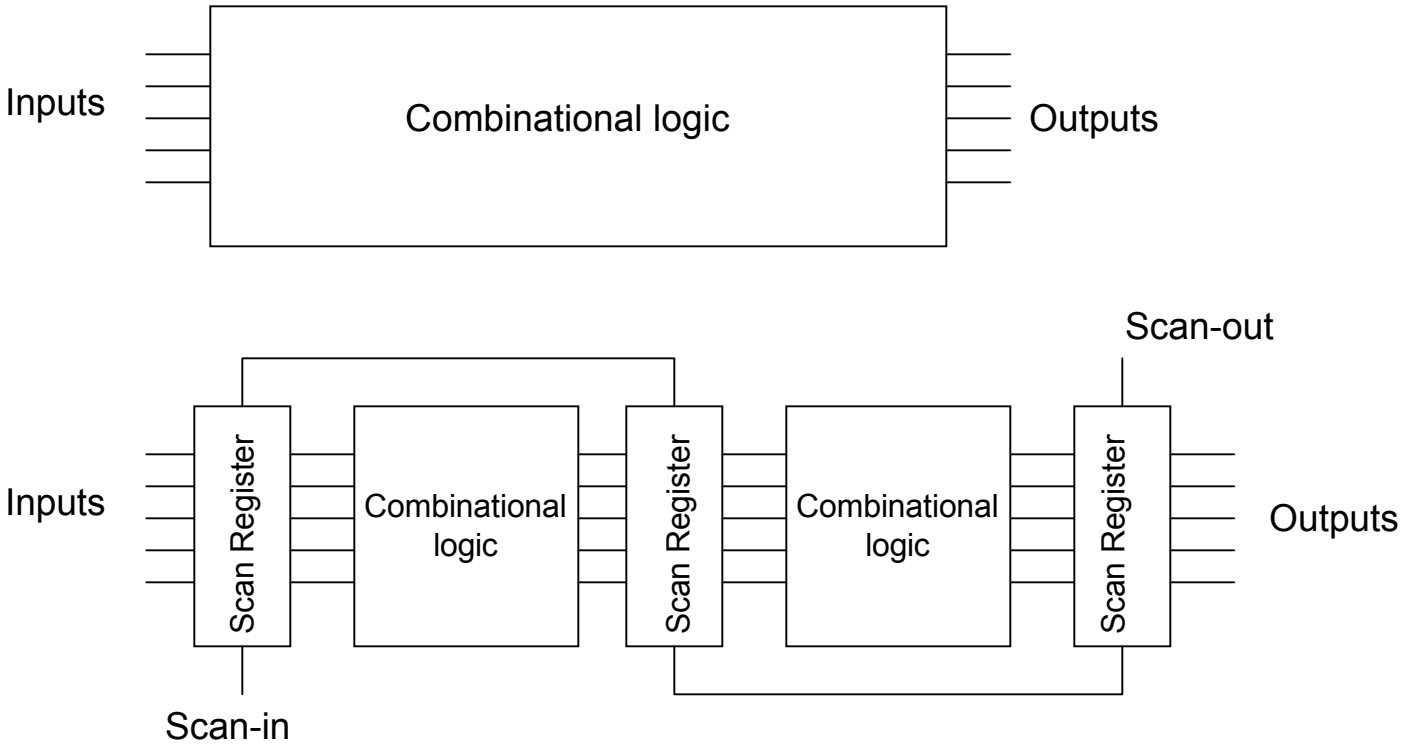
Design for Testability

- Scan-based techniques



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Design for Testability

- Built-in Self Test (BIST)
- Instead of loading scan registers from an off-chip tester, we load them on-chip
- Use a random test pattern generator with a fault dictionary

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IDDQ Testing

- Bridging fault detection
- Measure quiescent current from VDD when the CMOS logic is not switching - the current should be minimal
- IDDQ Testing DFT guidelines
  - Must be able to disable pseudo nMOS and analog circuitry if present
  - No active pull-ups or pull-downs
  - No degraded voltages - I.e. $V_{OH} = V_{DD}$ and $V_{OL} = 0$

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Exam 2 topics

- Lectures 11-21
- Chapters 6.3, 7, 8, 10-12
- Power Consumption/Low Power Design
- CMOS Design Strategies
- Clocking
- Memory Design

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CMOS Design Strategies

- Pass Transistor Logic
- Dynamic CMOS
- Zipper CMOS

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Clocking

- Register Design
- Clocking strategies
- State Machine design

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Memory Design

- RAM design
- ROM design
- Column and row decoders

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Next class

- Exam 2 April 12th
  - Lectures 11-21
  - HW 4-6
  - Chapters 6.3, 7,8, 10-12
- No class until April 28th

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