

ECE 249 Spring 2005

VLSI Design and Simulation

TuTh 3:30-4:20 ITE125

W 2-4, 4-6 ITEB C25

Course Description: *Four Credits. Prerequisite: ECE215.* Design of MOS transistors, including short channel effects in sub-micron devices; scaling laws; fabrication technologies. Layout of NMOS and CMOS logic gates; power-delay calculations. Design of static and/or dynamic memories. Laboratory emphasizes schematic capture, simulation, timing analysis; layout of custom IC's; use of VHDL; scaling laws and design of 0.5 micron circuits.

Instructor:

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Text: *Digital Integrated Circuits*, J. M. Rabaey, A. Chandrakasan, B. Nikolic

Grading Policy:

Exams	35%
Homeworks	10%
Labs	20%
Final Project	35%

Two exams tentatively scheduled for February 22nd and April 7th. There will be 5-6 homeworks and 6-7 lab assignments. A significant part of the course will be your final project which will be in teams of 2 or 3.

Rules:

Participation in class discussion is strongly encouraged.

Homework is due at the beginning of class on the due date. No extensions.

Tentative Schedule:

Week	Date	Tuesday	Wednesday	Thursday
1	1/18-20	Lec1: Introduction	No Lab	Lec2: MOS Transistor Theory
2	1/25-27	Lec3: Noise Margin, Static Load Inverters	Lab 1	Lec4: CMOS Processing Technology
3	2/1-3	Lec5: Performance Characterization	Lab 2	Lec6: Performance Characterization
4	2/8-10	Lec7: Performance Characterization, CMOS Design	Lab 3	Lec8: CMOS Design
5	2/15-17	Lec9: CMOS Logic Delays	Lab 4	Lec10: Layout Styles
6	2/22-24	Exam 1	Lab 5	Lec11: Power Dissipation
7	3/1-3	Lec12: CMOS Logic Structures	Lab 5	Lec13: Dynamic CMOS
8	3/8-10	Spring Break		
9	3/15-17	Lec14: Sequential Design	Lab 6	Lec15: Memory
10	3/22-24	Lec16: Control Logic	Lab 6	Lec17: Clocking
11	3/29-31	Lec18: I/O	Lab 7	Lec19: Design Strategies
12	4/5-7	Lec20: Testing & Verification	Final Project	Exam 2
13	4/12-14	No class	Final Project	No class
14	4/19-21	No class	Final Project	No class
15	4/26-28	Project Demonstrations	Project Demonstrations	Project Demonstrations