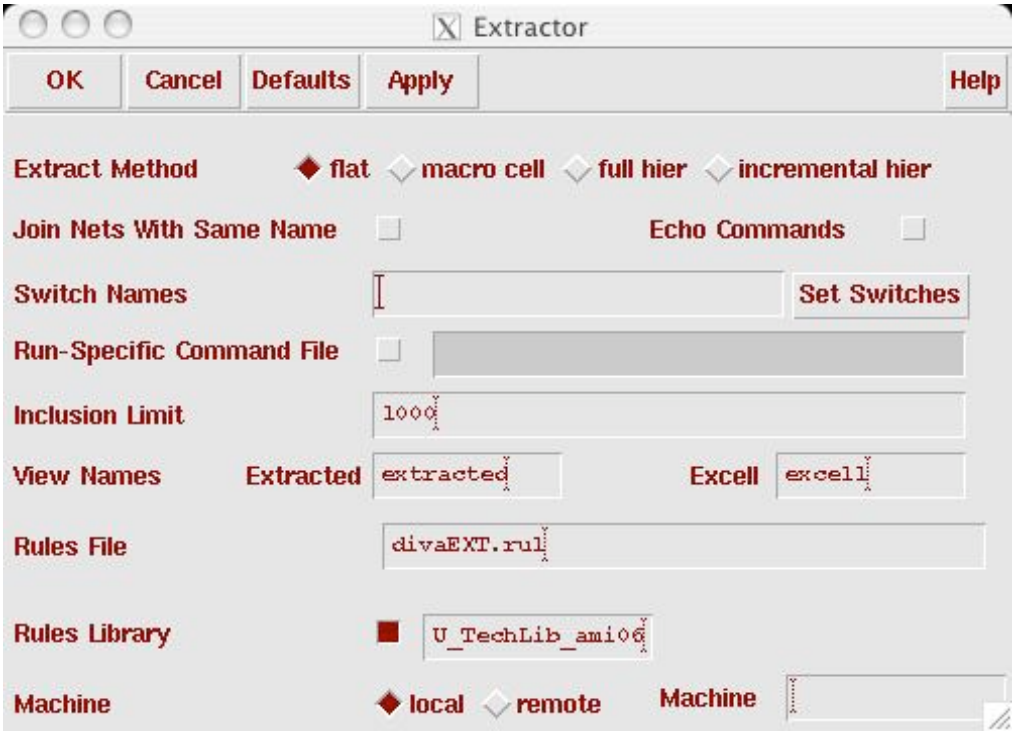
Layout extraction and Layout Versus Schematic (LVS)

Adapted from Princeton Cadence Page (http://www.ee.princeton.edu/~cadence/usr/lvs.html)

Once you have created the layout as well as the schematic for a design, how do we know they represent the same circuit? One way to verify this is by generating a circuit netlist from the layout and comparing it with the netlist for the schematic. This is the essence of the LVS tool. Thus in order to use the LVS tool, we have to first extract the layout to the netlist.

Layout extraction

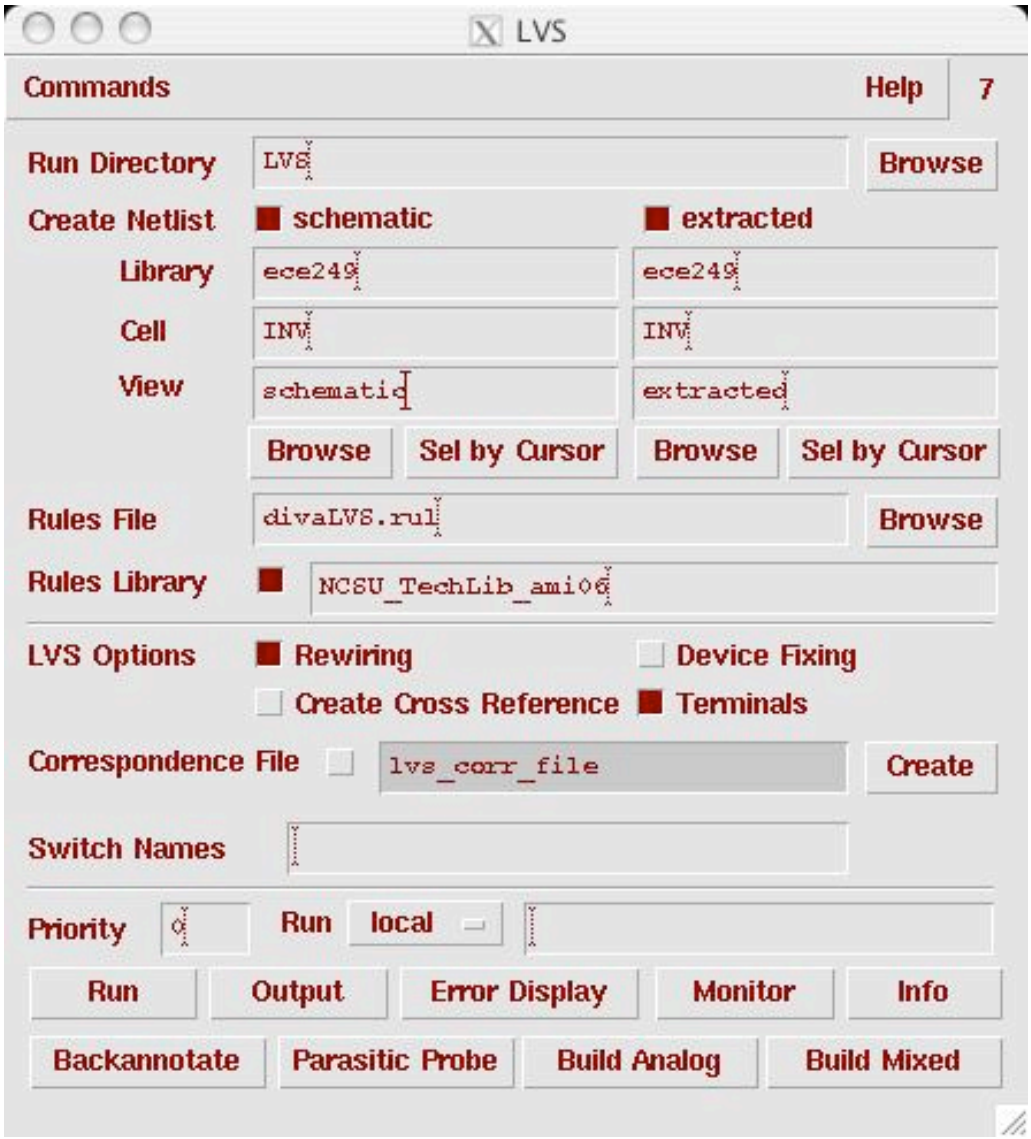
In the layout window, click on NCSU -> Modify LVS Rules... . Select "Compare FET Parameters". In the layout window, click on Verify -> Extract... . The following dialog box pops up.



Leave Switch Names empty and click on OK. Check the CIW window to make sure the layout extraction process runs through sucessfully. After the process is done, check the cell in the library manager and you will see an extracted view. Open the extracted view and a new layout window appears.

Layout Versus Schematic

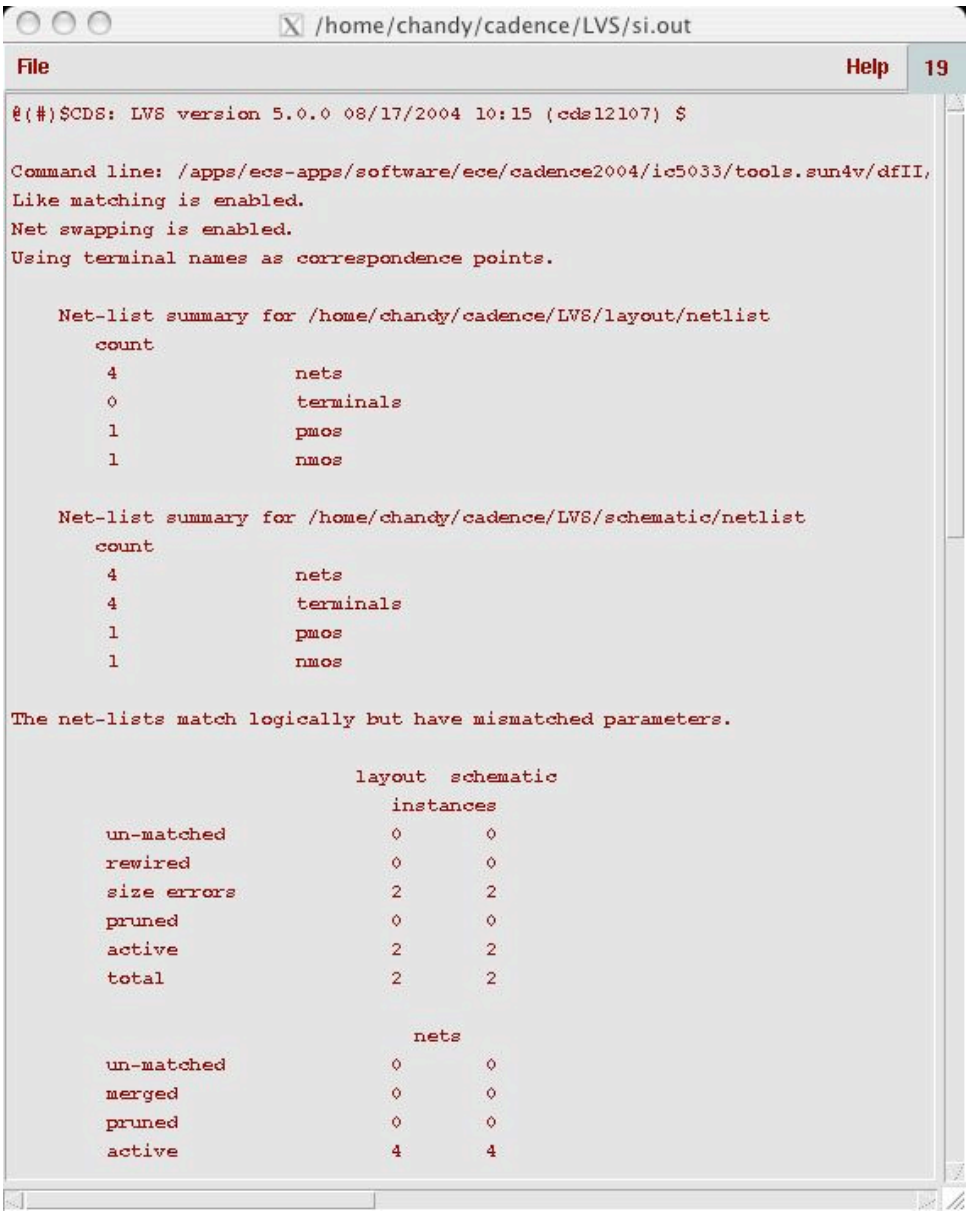
From the layout window, choose Verify -> LVS... . The following dialog box appears.



Specify the Run Directory as well as the cell and views you want to compare. If you are running LVS on a very large layout, it is better to create a run directory under /tmp so that LVS won't run out of disk space. Make sure that you have put the correct Rules File and Library. If you already have executed an LVS under the specified directory before, a window will pop-up which might say The selected LVS rule directory does not match the run form . Just click on Form contents and OK.

Click on the Run button. The LVS process may take a while to complete. To see if the job is still running, you can click on the Job Monitor... button in the LVS window and a pop up menu will appear to tell you the status of the current process. If the process is not successful, you can click on Info in the LVS window. A "Display Run Information" window appears. You can check the log file to figure out the run time problem for LVS.

When the LVS finishes running, a window will popup letting you know that the LVS has completed. If the LVS runs through successfully, click on Output in the LVS window and the result is displayed.



In this case, the LVS reports that there is no difference between the extracted circuit and the schematic netlists. However, there are mismatched parameters because of differences in transistor sizing in the schematic and layout. You can click on the Error Display button in the LVS window to identify where in the layout the errors are.

In the Error Display window, click on First and other buttons to display the current or all the errors in the extracted layout window. The errors are highlighted by a green dot. To get more information about the error, click on the Explain button. Modify the layout or schematic appropriately and rerun the LVS till your design is perfectly matched.