Simulation with Verilog-XL

Adapted from Princeton Cadence Page (http://www.ee.princeton.edu/~cadence/usr/verilog.html)

Until now, we have been using the Analog Environment to do simulations. This simulator allows us to do very detailed SPICE level simulations of the circuit in order to provide us with delay and timing information. However, in order to perform just logic level simulation, Analog Environment is too slow. Instead, we will use Verilog-XL to simulate our designs at logic level. In other words, we can only check if our design if functionally correct by using Verilog simulation. We will not be able to know, for example, the transient behavior of the circuit.

Still, Verilog simulation is very important. A circuit has to be verified to be functionally correct before we look into its transient behavior. This section talks about how to write a Verilog "testbench" for the inverter circuit and simulate its behavior. In order to use this tool, only minimal knowledge of Verilog is required (basically on how to supply the stimuli during the simulation).

As with Analog Environment simulation, with Verilog, you will have to create a test cell. This is only necessary if the circuit that you are testing does not already have connections to Vdd and Gnd. In the test cell, connect the test circuit to vdd and gnd parts from the analogLib as shown in Figure 1. Connect the input and outputs to appropriate pins – there is no need to connect any vpulse or vdc parts.

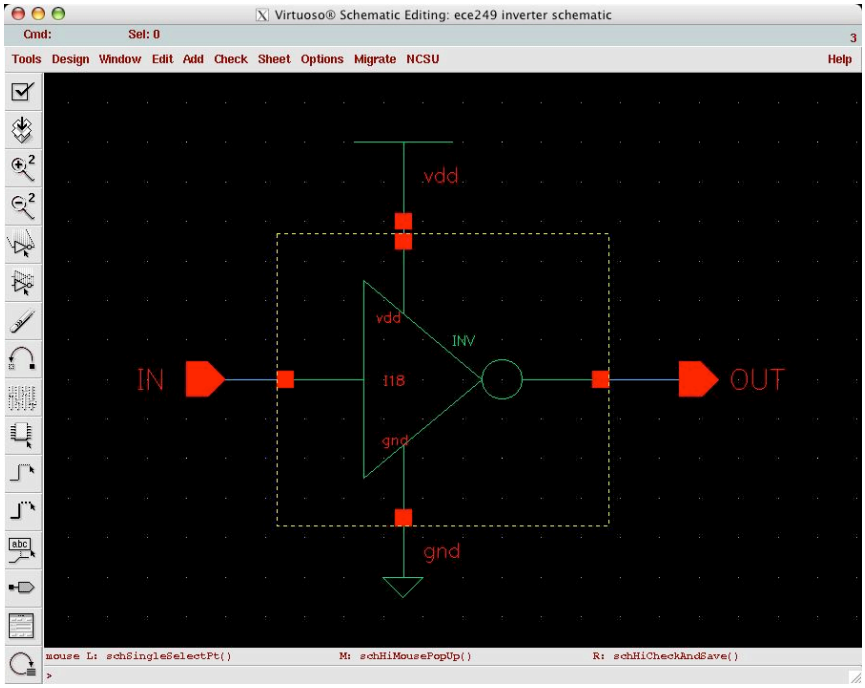


Figure 1. Inverter schematic

Start Verilog-XL

In the schematic design window, click on Tools-> Simulation->Verilog-XL to start Verilog-XL. A pop up dialogue box will appear.

Use the default settings to create a directory named inverter.run1 under the cadence run directory for the verilog simulation. You can specify another path if needed. In this case, we use the default settings. Now a Verilog simulation window appears as shown in Figure 2.

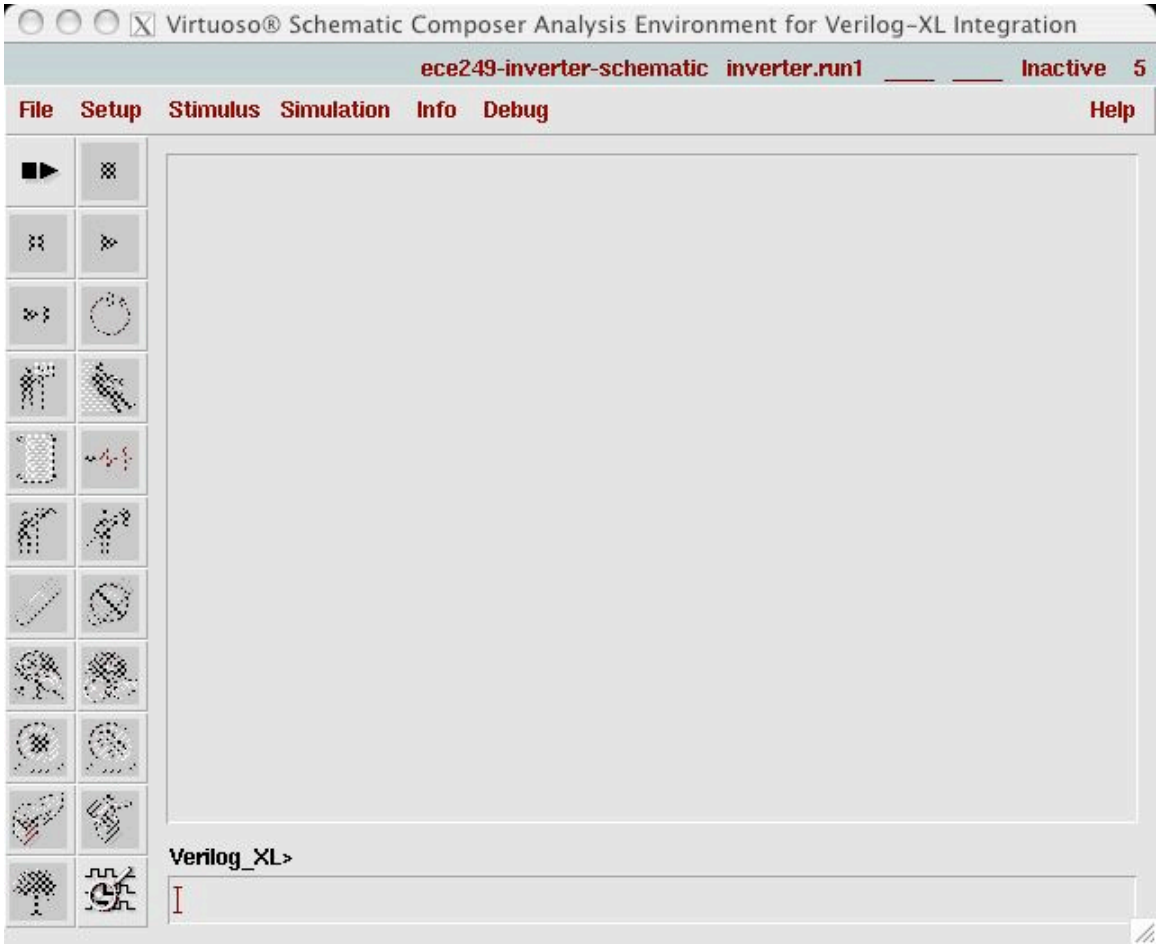
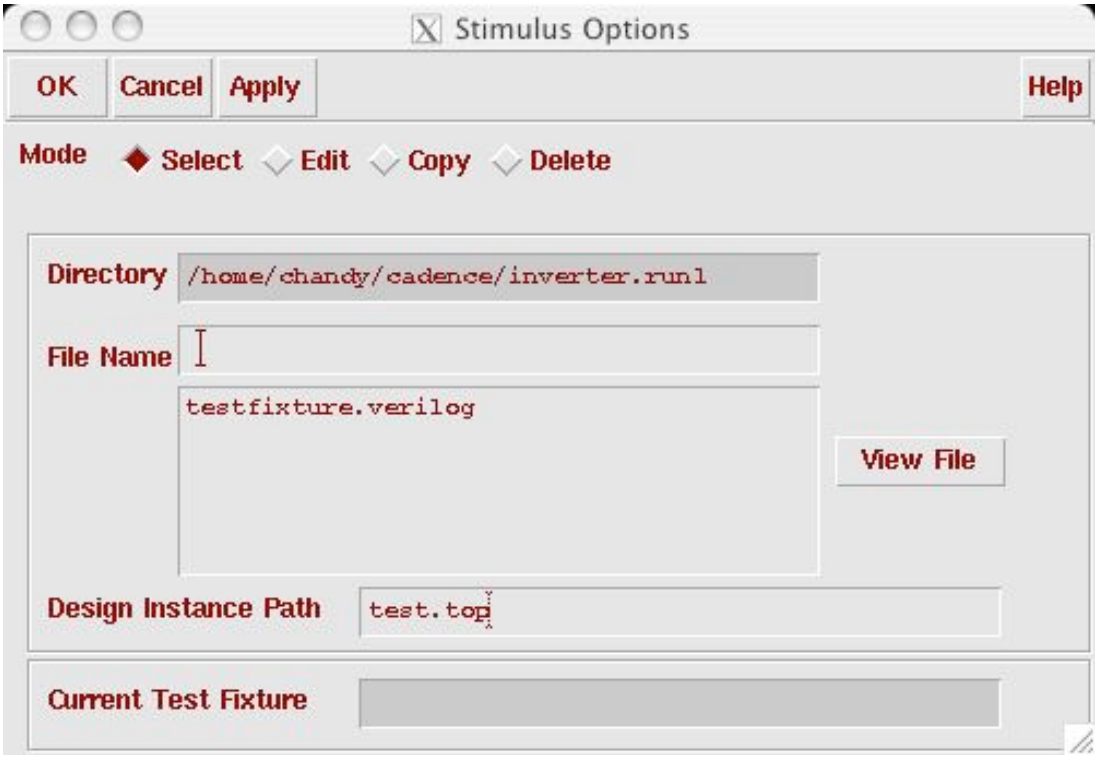


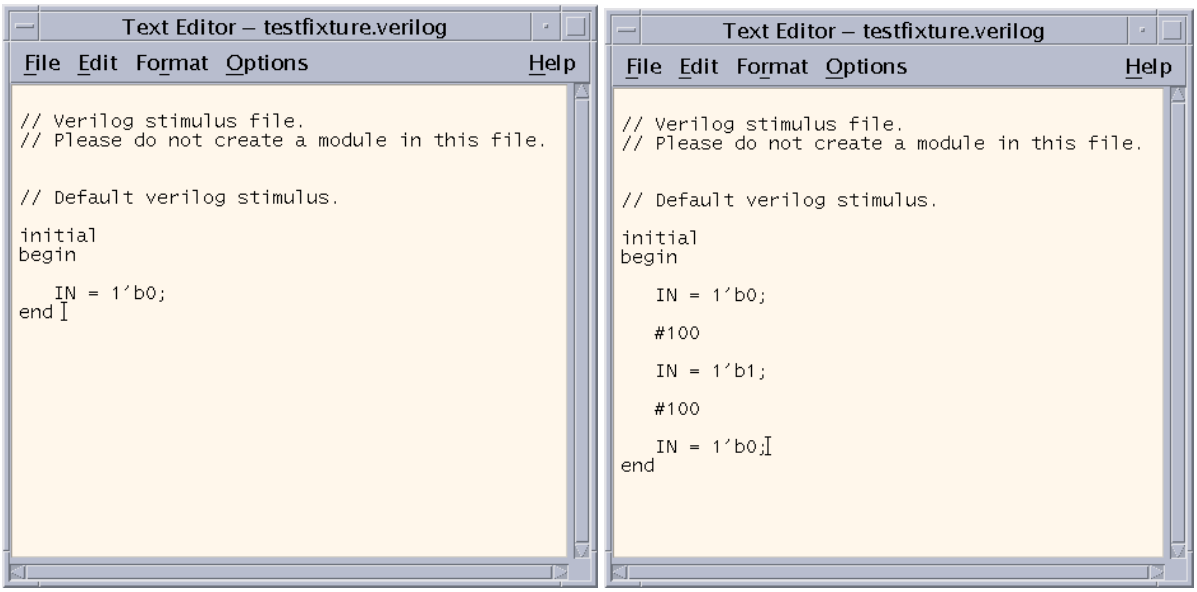
Figure 2. Verilog simulation window

Create stimulus file

Now in this Verilog simulation window, click on Stimulus->Verilog..., a pop up message box appears. For the first run, since we do not have a stimulus file yet, we click on Yes. A template file named testfixture.verilog has been created for us and a new pop up window appears.



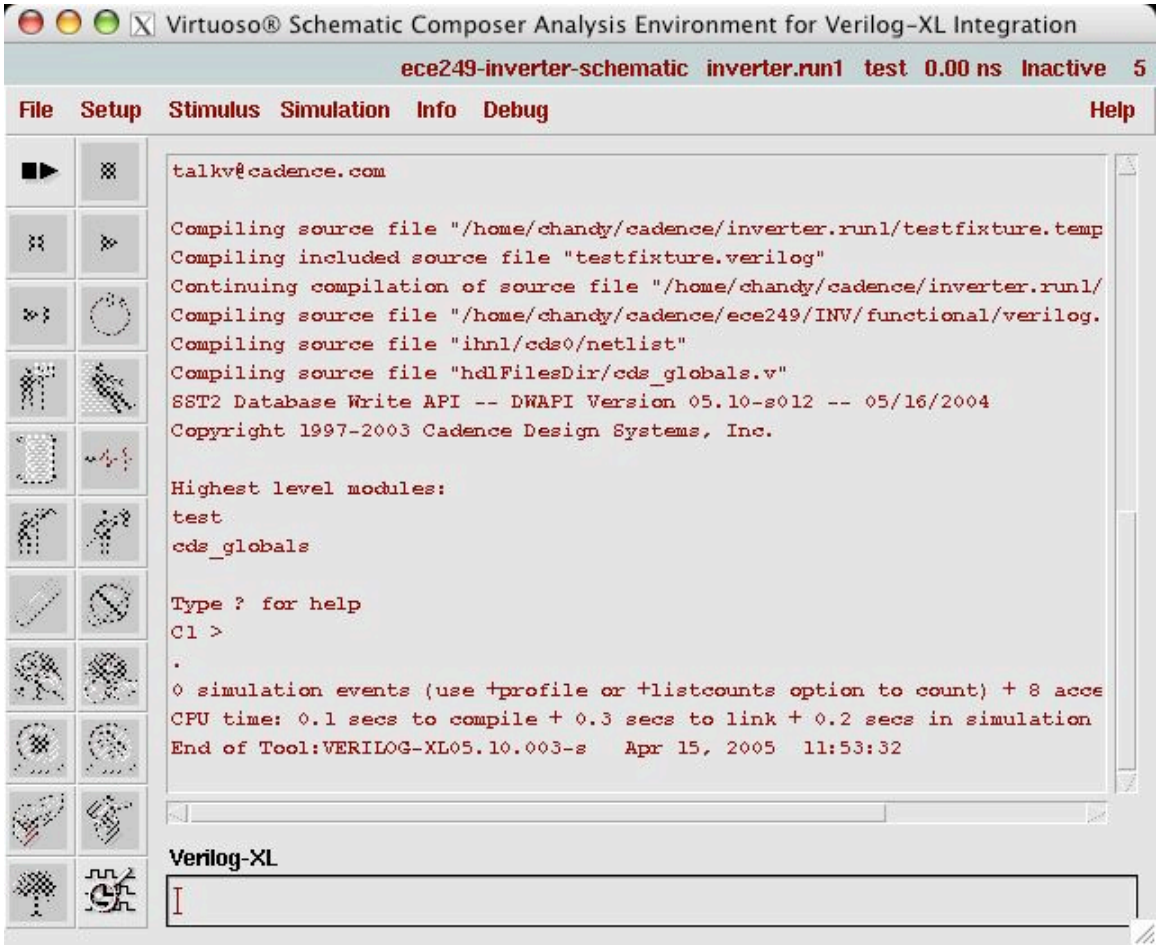
Choose testfixture.verilog as our stimulus file. Now we can modify this file to supply the stimuli during the simulation. Use any text editor to edit this file under the simulation directory (~/cadence/inverter.run1/testfixture.verilog in this example). The orginal file is shown in the left window below. Now we create a square wave for the input by letting inv_in to be "1" at 100ns and "0" again at 200ns. The modified simulation file is shown in the right window below.



Simulate

Before we start simulation, we should record all the signals that we want to display later. Click on Setup->Record Signals and save All signals in simulation history file so that we can record all the signals during the simulation to help debug our designs. Leave the waveform display package as Simvision

Now click on Simulation->Start Interactive in the simulation window. The simulation initiates. Click on Simulation->Continue to complete simulation. The simulation window should look like below when it completes.

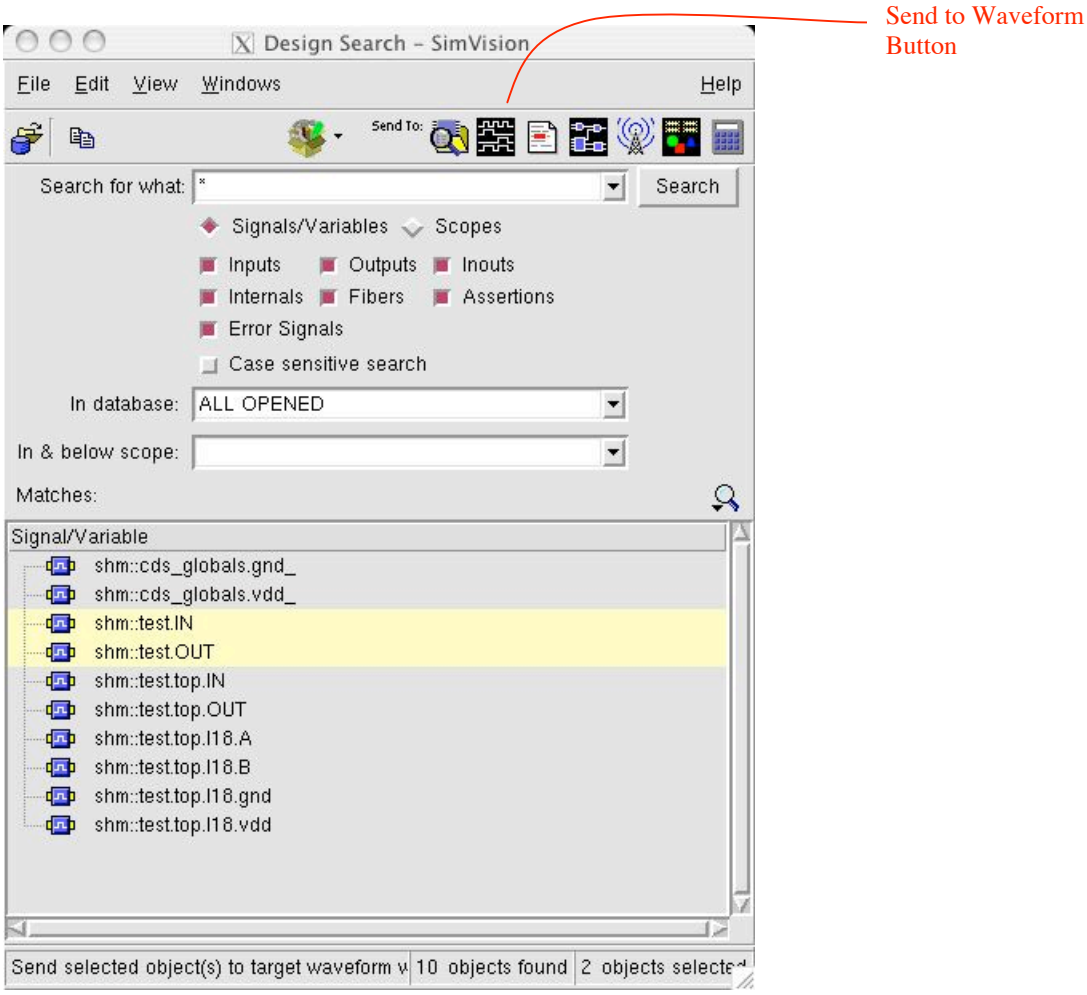


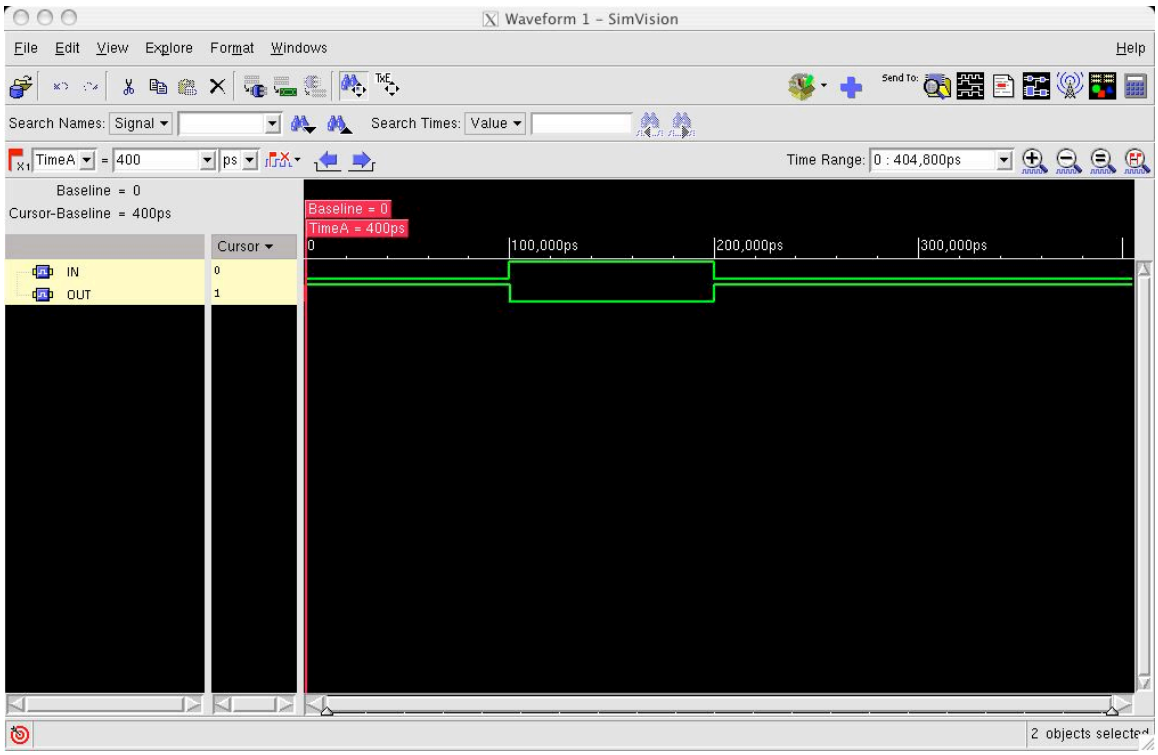
If we run into any problem in the simulation, we can check the si.log in the simulation directory (~/cadence/inverter.run1 in this example.)

View Waveforms

We can use a tool called "SimVision" to view the results in a waveform format. Click on Debug->Utilities->View Waveform in the simulation window. The waveform window appears.

In the waveform tool window, click on Windows->Tools->Design Search, and a design search window pops up. Note that because of the limited colormap on some of the workstations you may not be able to see the menubar titles. Make sure you don't have any web browser windows open before you start Cadence and this problem will be limited. In the search window, click the Search button and all the signals in your design will show up in the bottom of the search window. You can limit the signals that show up by typing your search parameters in the search text input. Select all the signals you are interested (in this example both shm::test.IN and shm::test.OUT). Finally Click on Send to Waveform button to display the waveforms in the waveform window. The Send To Waveform button is the second button in the group of buttons at the top right of the Search window.




Waveform 1 – SimVision
File Edit View Explore Format Windows Help
Search Names: Signal
Search Times: Value
TimeA = 400 ps
Time Range: 0 : 404,800ps
Baseline = 0
Cursor-Baseline = 400ps
Cursor
IN
OUT
0
1
Baseline = 0
TimeA = 400ps
0
100,000ps
200,000ps
300,000ps
2 objects selected