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# University Program Software Selection

Americas University Program 2012

## Custom Integrated Circuits Bundle

### The Custom IC Bundle Software Reference List:

| *Product* | *Product No.* | *Release Stream* |
|---|---|---|
| **Design Environment** | | |
| Virtuoso® Simulation Environment | 206 | IC615 |
| Virtuoso® AMS Designer Environment | 70000 | IC615 |
| Virtuoso® Analog Design Environment - XL | 95210 | IC615 |
| Virtuoso® Analog Design Environment - GXL | 95220 | IC615 |
| Virtuoso® Analog VoltageStorm Option | 34570 | IC610 |
| **Design Entry** | | |
| Cadence® SKILL Development Environment | 900 | IC615 |
| Virtuoso® Schematic VHDL Interface | 21060 | IC615 |
| Virtuoso® Schematic Editor Verilog® Interface | 21400 | IC615 |
| Virtuoso® Schematic Editor - XL | 95115 | IC615 |
| Virtuoso® Analog Oasis Run-Time Option | 32100 | IC615 |
| **Layout** | | |
| Virtuoso® Layout Suite - GXL[1] | 95321 | IC615 |
| Cadence® Chip Assembly Router[2] | 3300 | IC615 |
| **Circuit Simulation** | | |
| Virtuoso® Schematic Editor HSPICE Interface[3] | 276 | IC615 |
| Virtuoso® Analog Design Environment - GXL | 95220 | IC615 |
| Virtuoso® Spectre® Circuit Simulator | 38500 | MMSIM111 |
| Virtuoso® UltraSim Simulator | 33400 | MMSIM111 |
| Virtuoso® Multi-mode Simulation Power Option | 91400 | MMSIM111 |
| Virtuoso® Spectre® RF Simulation Option for 38500 | 38520 | MMSIM111 |
| Virtuoso® RelXpert | 33580 | MMSIM111 |
| Virtuoso® Analog HSPICE Interface Option[1] | 32760 | IC615 |
| AMS Designer with Flexible Analog Simulation | 70020 | INCISIV111 |
| Virtuoso® Multi-mode Simulation with AP Simulator | 90003 | MMSIM111 |

[1] includes CIF reader/writer and Virtuoso Stream Interface
[2] includes GDSII/EDIF and LEF/DEF interfaces
[3] requires additional licenses that must be obtained from Synopsys

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**The Custom IC Bundle Software Reference List, continued**

| ***Product*** | ***Product No.*** | ***Release Stream*** |
|---|---|---|
| **Physical Verification** | | |
| Dracula® Graphical User Interface | 365 | IC615 |
| Dracula® Physical Verification and Extractor Suite | 70520 | IC615 |
| Diva® Physical Verification and Extractor Suite | 71520 | IC615 |
| Assura™ Design Rule Checker | 72110 | ASSURA41 |
| Assura™ Layout vs. Schematic Verifier | 72120 | ASSURA41 |
| Virtuoso® QRC Extraction - L | QRCX100 | PVE111 |
| Virtuoso® QRC Extraction - XL | QRCX300 | PVE111 |
| Virtuoso® Advanced Analysis GXL option | QRCX310 | PVE111 |
| Cadence® QuickView Layout and Mask Data Viewer | K2200 | PVE111 |
| Cadence® Physical Verification System Design Rule Checker XL | 96210 | PVE111 |
| Cadence® Physical Verification System Layout vs. Schematic Checker XL | 96220 | PVE111 |
| Cadence® Physical Verification System Results Manager | 96240 | PVE111 |
| Cadence® Physical Verification System graphic LVS Debugger | 96250 | PVE111 |
| Cadence® Physical Verification System Constraint Validator | 96300 | PVE111 |
| Assura™ Graphical User Interface Option | 72140 | ASSURA41 |
| Assura™ Multiprocessor Option | 72150 | ASSURA41 |
| Pcell Generator | PASPCG | PAS31 |
| Graphical Technology Editor | PASGTE | PAS31 |
| Generator for Assura™ compatible verification decks | PASASG | PAS31 |
| Generator for Diva® compatible verification decks | PASDIG | PAS31 |
| Generator for Dracula® compatible verification decks | PASDRG | PAS31 |
| Error Cell Generator | PASECG | PAS31 |
| **RF System-In-Package (SIP)**[1] | | |
| Cadence® SiP RF Architect – XL | SIP410 | SPB165 |
| Cadence® SiP Layout – XL | SIP225 | SPB165 |
| **Interfaces** | | |
| Virtuoso® EDIF 200 Reader | 940 | IC615 |
| Virtuoso® EDIF 200 Writer | 945 | IC615 |
| Cadence® Design Framework Integrator's Toolkit | 12141 | IC615 |

[1] must be installed with Virtuoso

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## Digital Integrated Circuits Bundle

### The Digital IC Bundle Software Reference List

| ***Product*** | ***Product No.*** | ***Release Stream*** |
|---|---|---|
| **Place & Route and Timing** | | |
| Virtuoso® Layout Suite - GXL | 95321 | IC615 |
| Cadence® Chip Assembly Router | 3300 | IC615 |
| **Design for Manufacturing** | | |
| Virtuoso® Power System – L | VPS100 | IC615 |
| Virtuoso® Power System – XL | VPS200 | IC615 |
| VoltageStorm (transistor) | VST1 | ANLS62 |
| Encounter Power System - L | EPS100 | ETS110 |
| Encounter Power System - XL | EPS200 | ETS110 |
| EPS Advanced Analysis GXL Option | EPS201 | ETS110 |
| **Signal Integrity** | | |
| Encounter™ Timing System - XL | FE725 | ETS110 |
| PacifIC Static Noise Analyzer for Custom Digital ICs | CM00100 | PACIFIC61 |
| Encounter™ Timing System - L | FE625 | ETS110 |
| ETS Advanced Analysis GXL Option | FE830 | ETS110 |
| Encounter™ Library Characterizer- XL | ELC200 | ETS110 |
| **Silicon Virtual Prototyping** | | |
| Encounter™ Digital Implementation System - XL | EDS200 | EDI110 |
| Encounter™ Low Power GXL Option | EDS10 | EDI110 |
| Encounter™ Advanced Node GXL option | EDS30 | EDI110 |
| Encounter™ Mixed Signal GXL Option | EDS20 | EDI110 |
| **Test** | | |
| Architect Advanced Option to RC | ET021 | ET111 |
| Encounter™ True Time Test Advanced | ET023 | ET111 |
| Encounter™ Diagnostics Engine - XL | ET009 | ET111 |

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**The Digital IC Bundle Software Reference List, continued**

| | | |
|---|---|---|
| **Digital System-In-Product (SIP)**[1] | | |
| Cadence® SiP Digital Architect – GXL | SIP125 | SPB165 |
| Cadence® SiP Digital SI - XL | SIP215 | SPB165 |
| Cadence® Chip Integration Option | SIP625 | SPB165 |
| **Formal Verification** | | |
| Encounter™ Conformal - GXL | CFM300 | CONFRML111 |
| Encounter™ Conformal Low Power - XL | CFM500 | CONFRML111 |
| **Synthesis** | | |
| Encounter™ RTL Compiler - XL | RC200 | RC111 |
| Encounter™ RTL Compiler - GXL option | RC300 | RC111 |
| Encounter™ RTL Compiler with physical | RC400 | RC111 |
| C-to-Silicon Compiler – L | CTS102 | CTOS112 |
| **Chip Planning** | | |
| Cadence® InCyte Chip Estimator L | CPS100 | CICE42 |
| Cadence® InCyte Chip Estimator XL | CPS200 | CICE42 |

[1] must be installed with Encounter

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# University Program Software Selection

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## Verification Bundle

### The Verification Bundle Software Reference List

| *Product* | *Product No.* | *Release Stream* |
|---|---|---|
| **Functional Verification** | | |
| Incisive Enterprise Simulator - L | 29610 | INCISIV111 |
| Cadence® Simulation Analysis Environment (SimVision) | 25010 | INCISIV111 |
| Verifault – XL Simulator | 26500 | INCISIV111 |
| Incisive™ Enterprise Simulator | 29651 | INCISIV111 |
| Enterprise Simulator - XL Interface for MTI | 29661 | INCISIV111 |
| Enterprise Simulator - XL Interface for VCS | 29671 | INCISIV111 |
| Incisive™ Formal Verifier | 23560 | INCISIV111 |
| Incisive™ Enterprise Verifier – XL | IEV101 | INCISIV111 |
| Incisive™ Software Extensions | ISX100 | INCISIV111 |
| Virtuoso® AMS Designer Verification Option | 70030 | INCISIV111 |
| Cadence® System Creator | CSC100 | INCISIV111 |
| Cadence® Software Developer | CSD100 | INCISIV111 |
| **Verification Process Automation** | | |
| Incisive™ Enterprise Manager | EMG100 | INCISIV111 |
| **Pre-verified, Re-usable Verification IP Components** | | |
| Incisive VIP Portfolio | VIP100 | VIPP92 |

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# University Program Software Selection

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## Silicon-Package-Board Bundle

### The Packaging & Board Bundle Software Reference List

| *Product* | *Product No.* | *Release Stream* |
|---|---|---|
| **PCB Design and Layout** | | |
| Allegro® PCB Designer | PA3100 | SPB165 |
| Allegro® PCB High-Speed Option | PA3110 | SPB165 |
| Allegro® PCB Miniaturization Option | PA3120 | SPB165 |
| Allegro® Design Authoring High-Speed Option | PA1410 | SPB165 |
| Allegro® PCB Routing Option | PS3500 | SPB165 |
| Allegro® PCB Librarian - XL | PX3500 | SPB165 |
| Allegro® 2 FPGA System Planner Option | PA8250 | SPB165 |
| **PCB High-Speed Analysis** | | |
| Allegro® PCB SI - XL | PX3100 | SPB165 |
| **IC Packaging** | | |
| Cadence® SiP Layout – XL | SIP225 | SPB165 |
| **Simulation** | | |
| Allegro® AMS Simulator[1] | PS2200 | SPB165 |

[1] superset of Pspice and Advanced Analysis Option

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# University Program Software Selection

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## New products added in 2011

RC400 - Encounter™ RTL Compiler with physical
IEV101 - Incisive™ Enterprise Verifier – XL
PA8210 - Allegro® FPGA System Planner – L
PA8215 - Allegro® FPGA System Planner Two FPGA Option - L
VPS100 - Virtuoso® Power System – L
VPS200 - Virtuoso® Power System – XL
FE830 - ETS Advanced Analysis GXL Option
EPS201 - EPS Advanced Analysis GXL Option
CTS102 - C-to-Silicon Compiler – L
CFM500 – Encounter Conformal Low Power - XL

## Changes made in 2012:

| Discontinued products | Replacement |
|---|---|
| 33500 - Virtuoso® UltraSim Full-chip Simulator | 33400 – Virtuoso® UltraSim Simulator |
| 33500 - Virtuoso® UltraSim Full-chip Simulator | 91400 – Virtuoso® Multi-mode Simulation Power Option |
| PX3700 - Allegro® PCB Design HDL - XL | PA3100 - Allegro® PCB Designer |
| PX3710 - Allegro® PCB Design CIS - XL | PA3100 - Allegro® PCB Designer |
| PA8210 – Allegro® FPGA System Planner-L | PA8250 – Allegro 2 FPGA System Planner Option |
| PA8215 – Allegro® 2 FPGA System Planner | PA8250 – Allegro 2 FPGA System Planner Option |

## New products added in 2012

34570 - Virtuoso® Analog Voltagestorm Option
33400 – Virtuoso® UltraSim Simulator
91400 – Virtuoso® Multi-mode Simulation Power Option
PA3100 - Allegro® PCB Designer
PA3110 - Allegro® PCB High-Speed Option
PA3120 - Allegro® PCB Miniaturization Option
PA1410 - Allegro® Design Authoring High-Speed Option
PS3500 - Allegro® PCB Routing Option
CSC100 – Cadence® System Creator
CSD100 – Cadence® Software Developer
K2200 - Cadence® QuickView Layout and Mask Data Viewer
96210 - Cadence® Physical Verification System Design Rule Checker XL
96240 - Cadence® Physical Verification System Results Manager
96300 - Cadence® Physical Verification System Constraint Validator
EDS20 - Encounter™ Mixed Signal GXL Option
96220 - Cadence® Physical Verification System Layout vs. Schematic Checker XL
96250 - Cadence® Physical Verification System graphic LVS Debugger