# Topics

- Clocking





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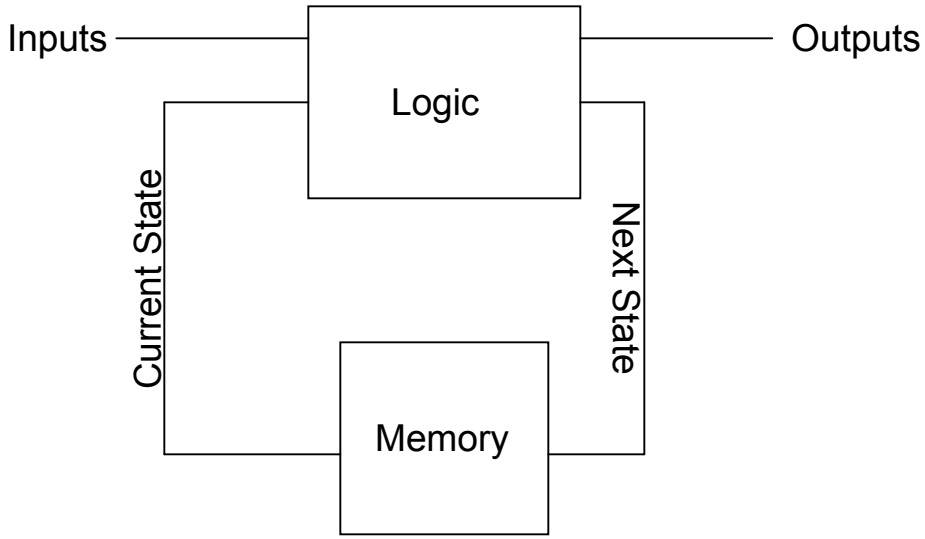
# Finite State Machine







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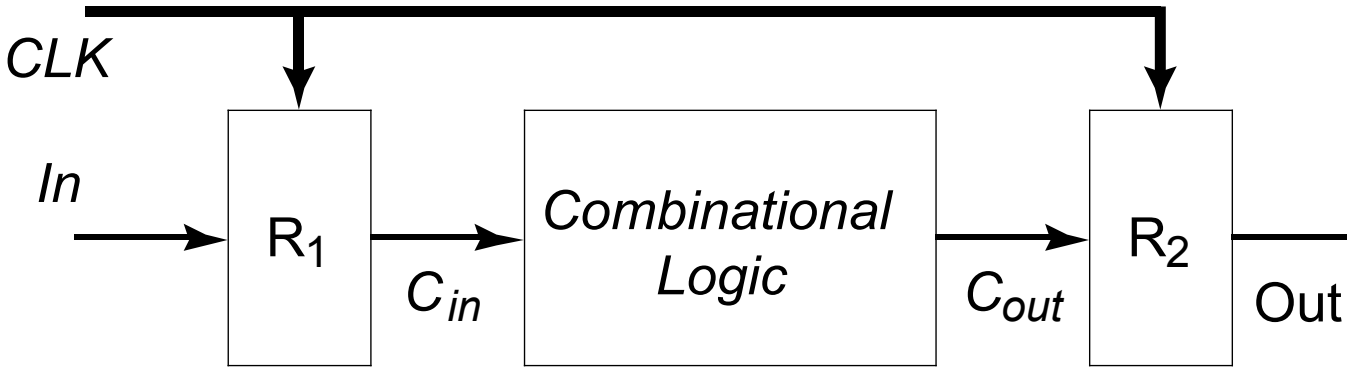
# Synchronous Timing







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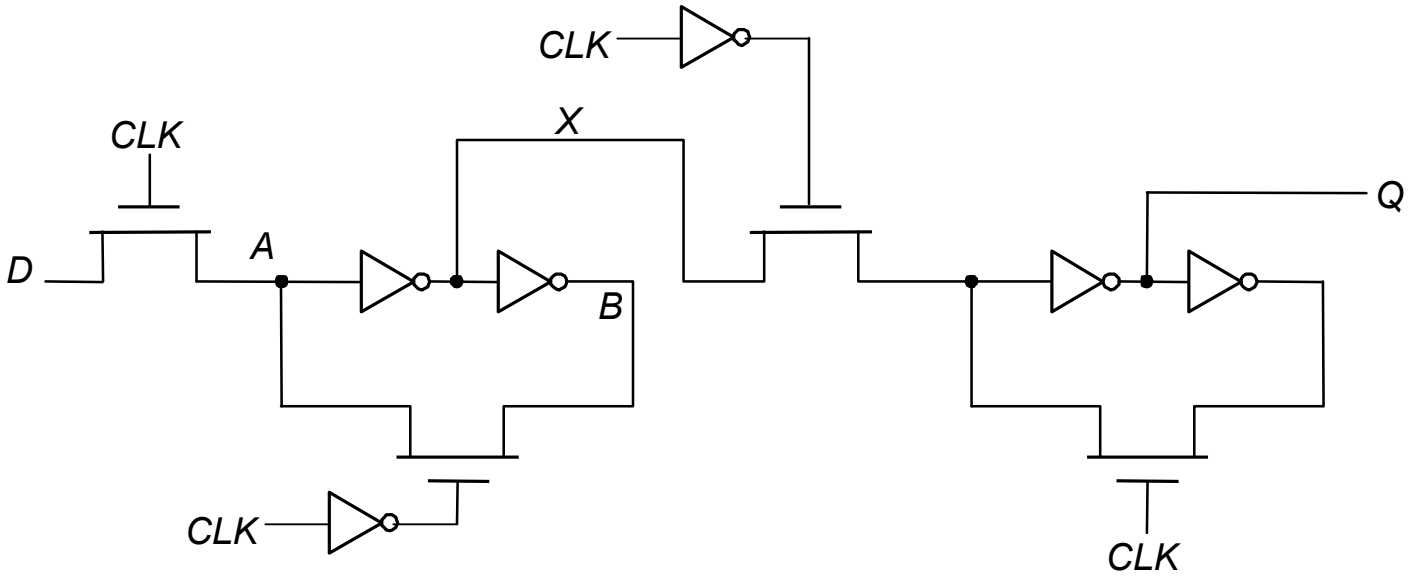
# Register Design







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# Register Design

- Inverted clock is not ideal
- Causes delays on the clock
- Overlapping clock pair




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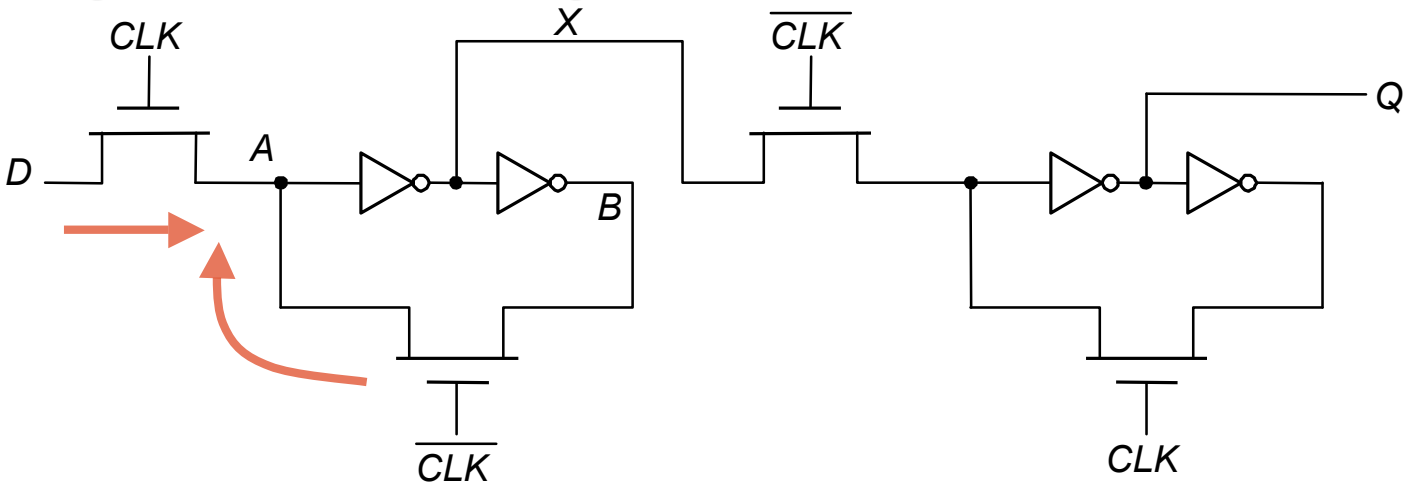
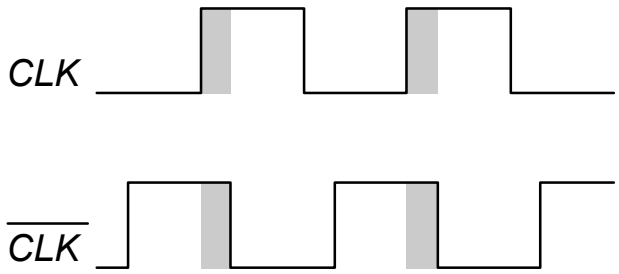
# Register Design




(a) Schematic diagram




(b) Overlapping clock pairs

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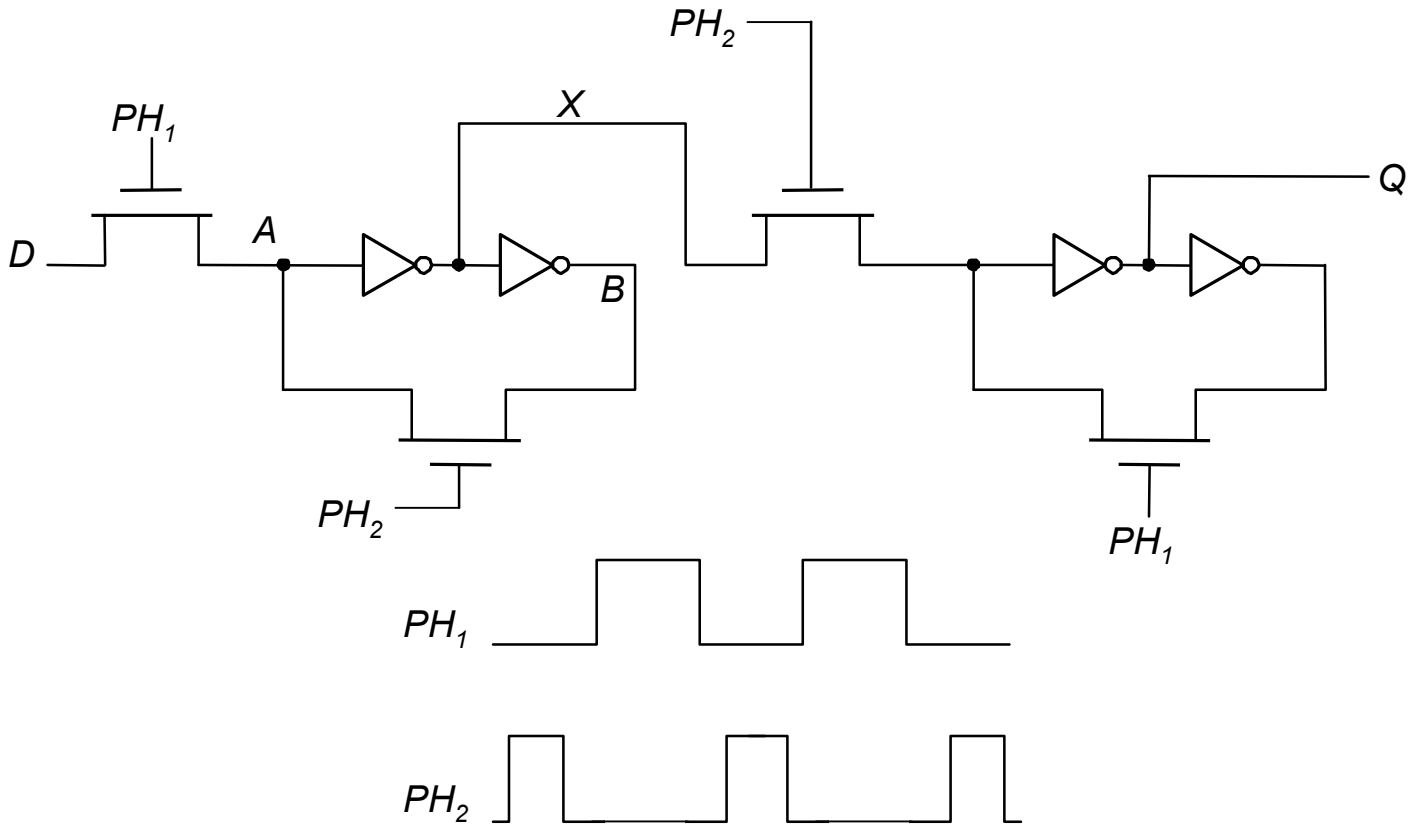
# Register Design

- Use non-overlapping clocks







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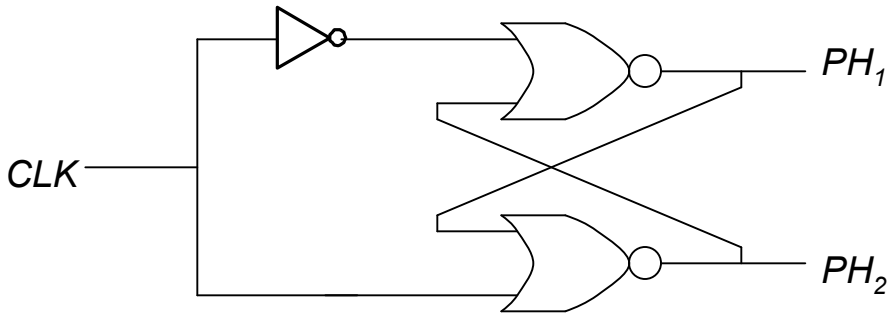
# Register Design

- Generating non-overlapping clocks







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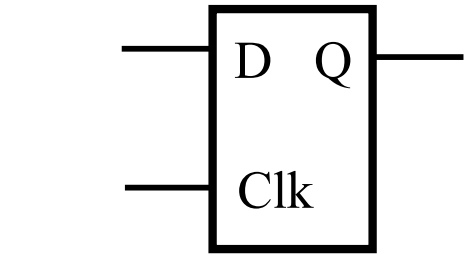
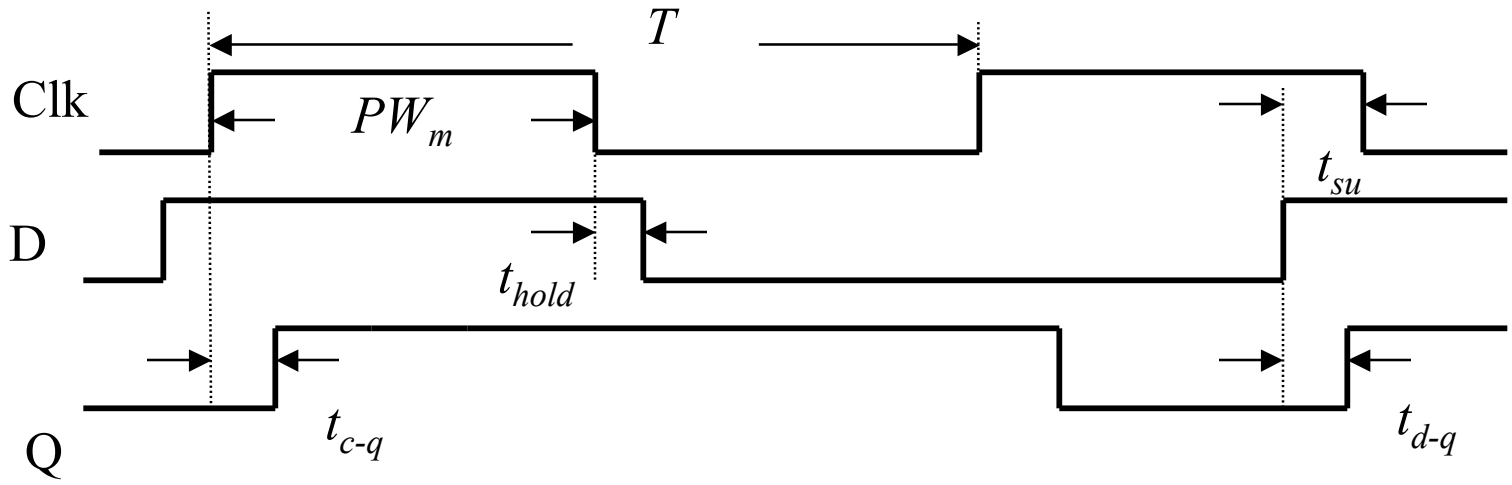
# Latch Parameters







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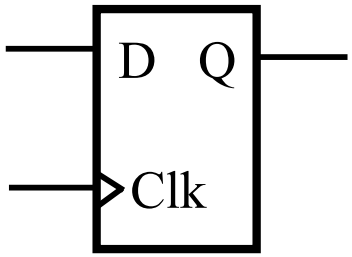
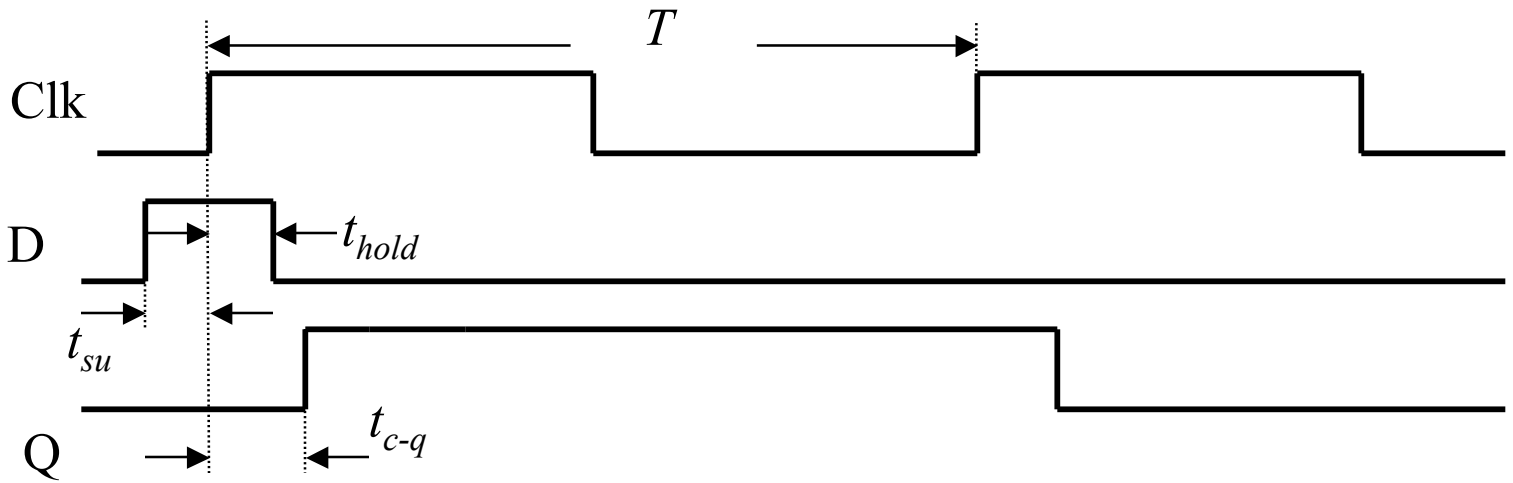
# Register Parameters







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# Clock Nonidealities

- Clock Skew
  - Spatial variations in equivalent clock edges
  - Mostly deterministic
- Clock Jitter
  - Temporal variations in consecutive clock edges
  - Mostly random
- Pulse Width Variation




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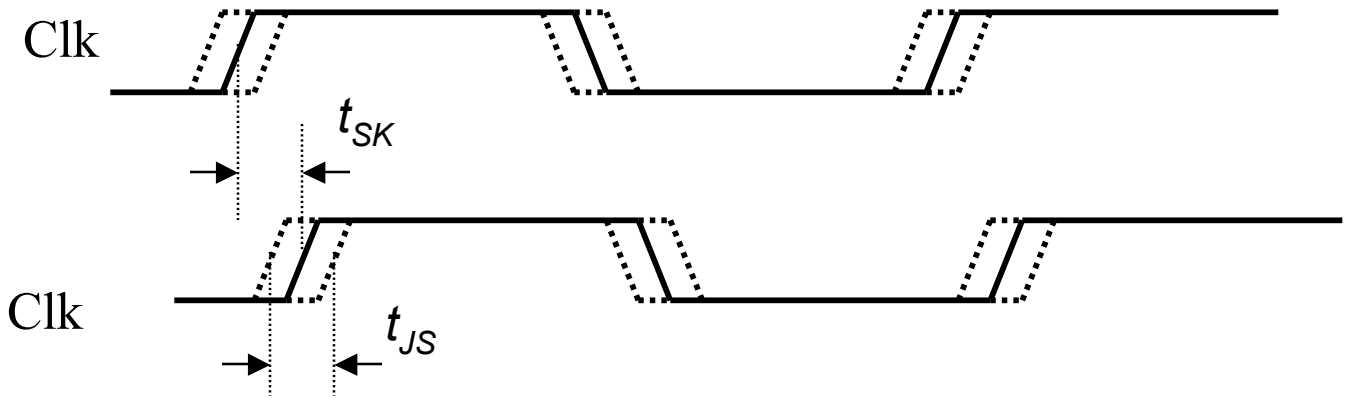
# Clock Skew and Jitter




- Skew and jitter can affect the cycle times
- Clock skew can cause race conditions

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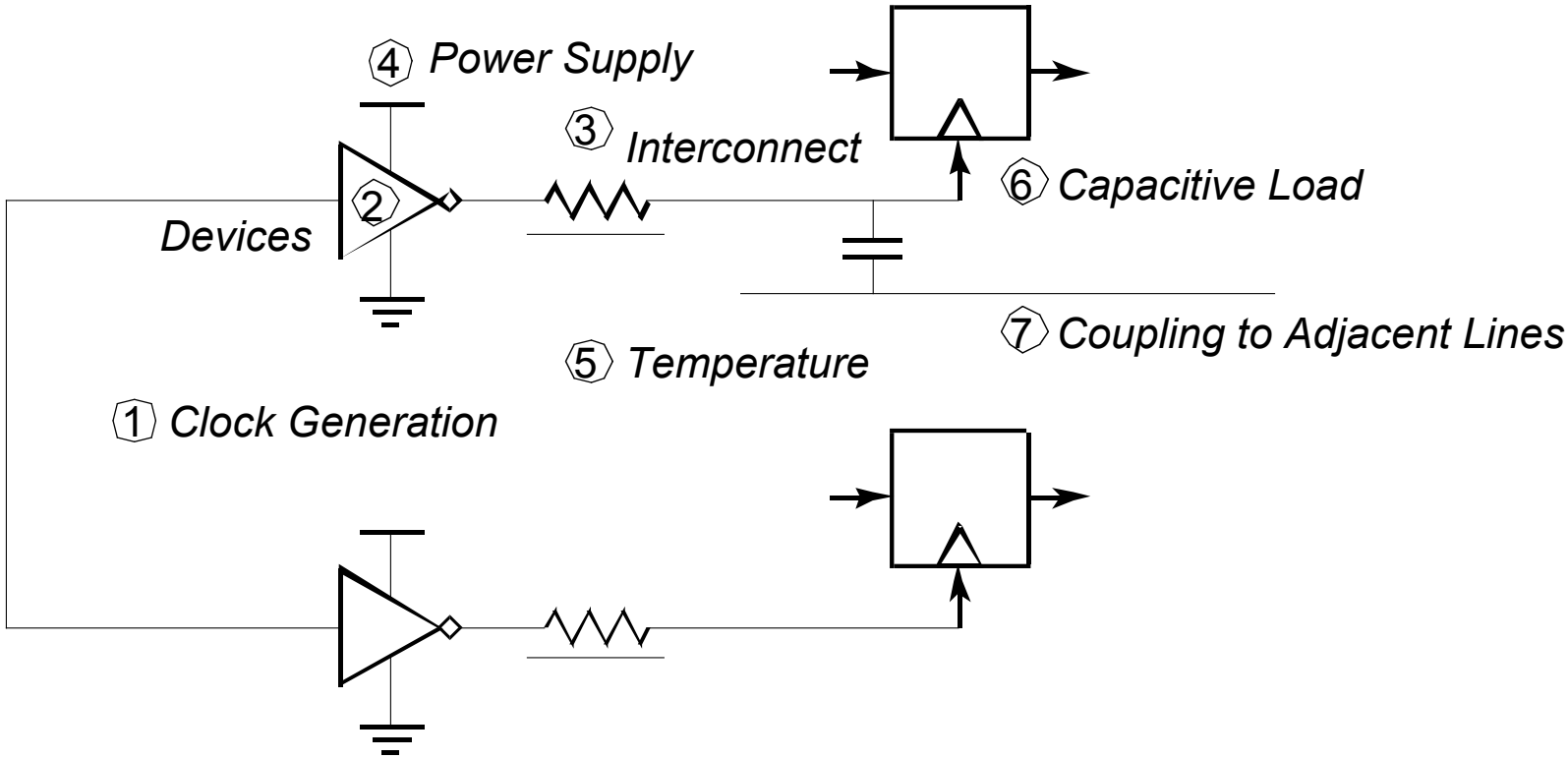
# Clock Uncertainties







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# Clock Uncertainties

- Clock Signal Generation
  - Analog circuit sensitive to noise
  - Causes jitter
  - Difficult to model
- Device Manufacturing
  - Process variations
  - Causes static skew
  - Can be partially modeled




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# Clock Uncertainties

- Interconnect variations
  - Causes skew on different paths
  - Different inter-layer dielectric thickness
  - Can be somewhat predictable based on process
- Temperature
  - Dependent on switching activity
  - Parts of a chip may see different temperatures
  - Contributes to clock jitter




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# Clock Uncertainties

- Power supply variations
  - Dependent on switching activiity
  - Causes jitter
- Capactive coupling
  - Between clock and adjacent lines
  - Transitions on adjacent lines can cause varying coupling effects
  - Net effect is jitter on the clock




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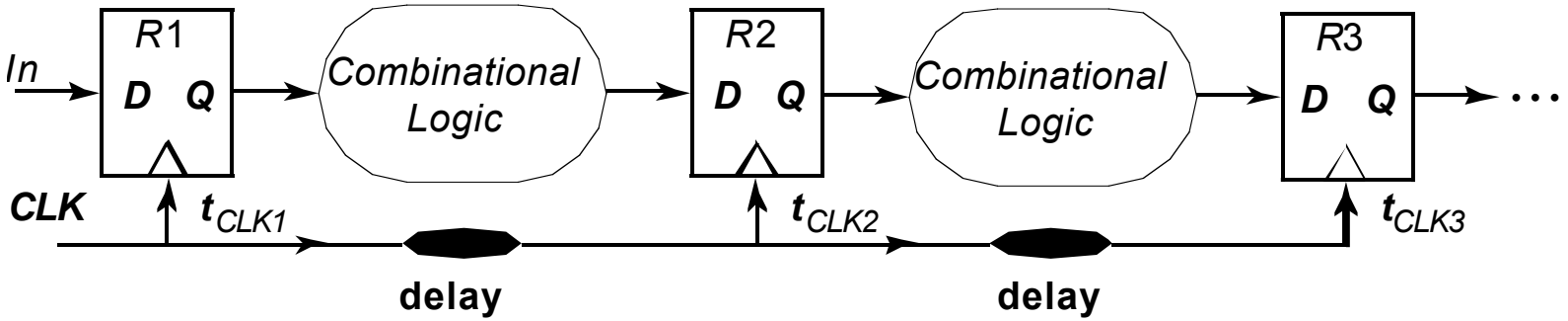
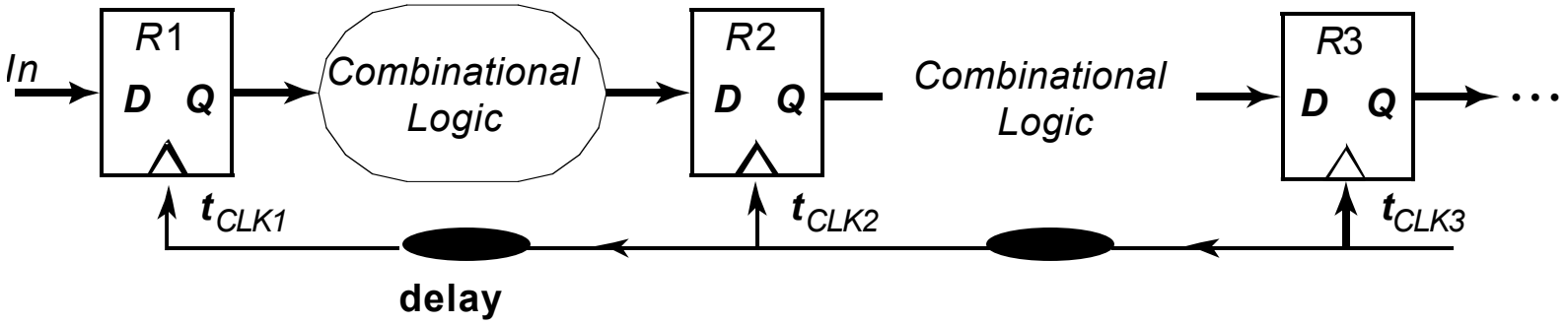
# Positive and Negative Skew




(a) Positive skew




(b) Negative skew

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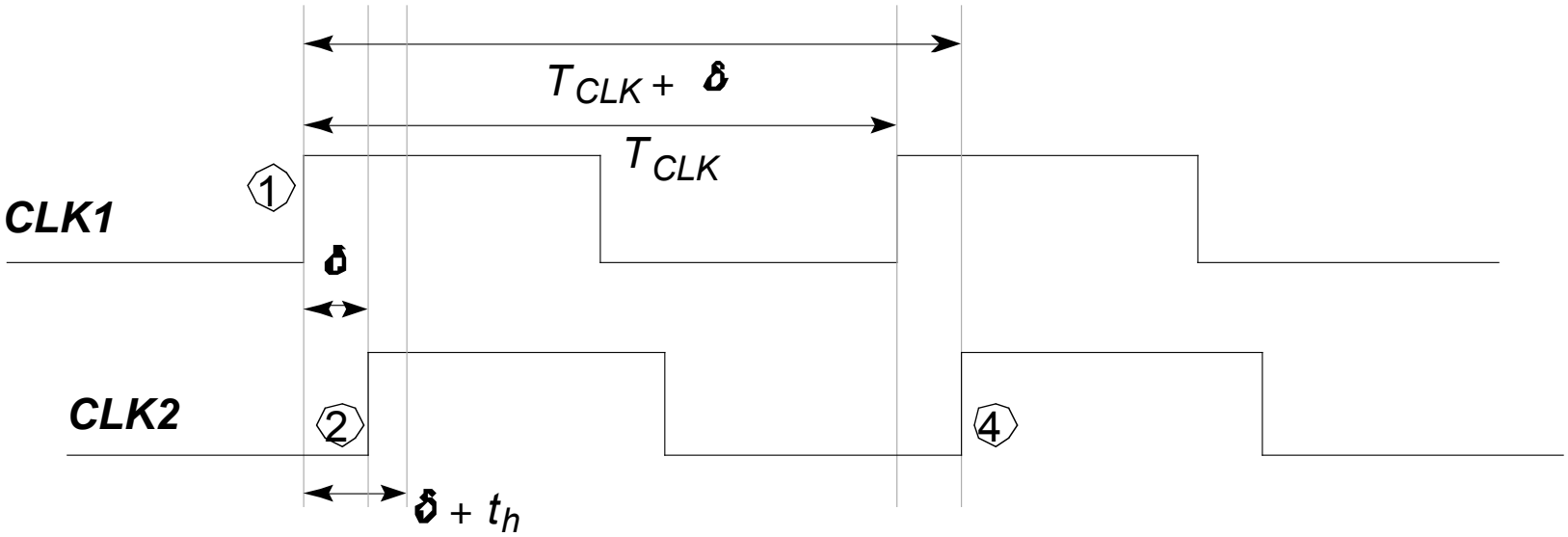
# Positive Skew




*Launching edge arrives before the receiving edge*

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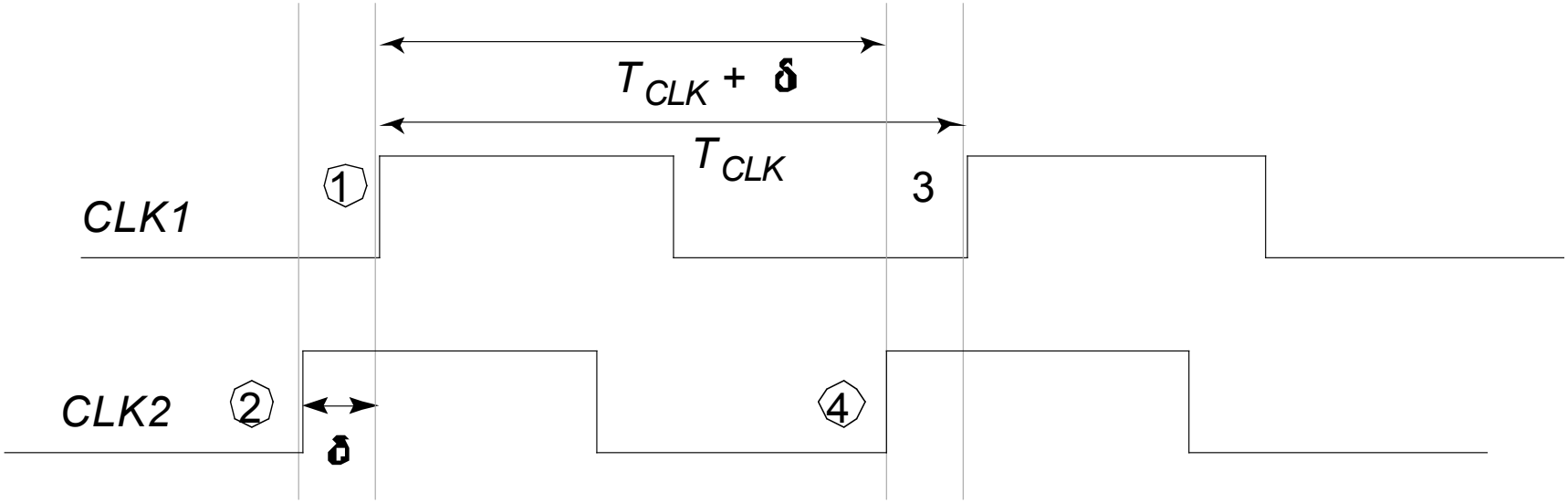
# Negative Skew




*Receiving edge arrives before the launching edge*

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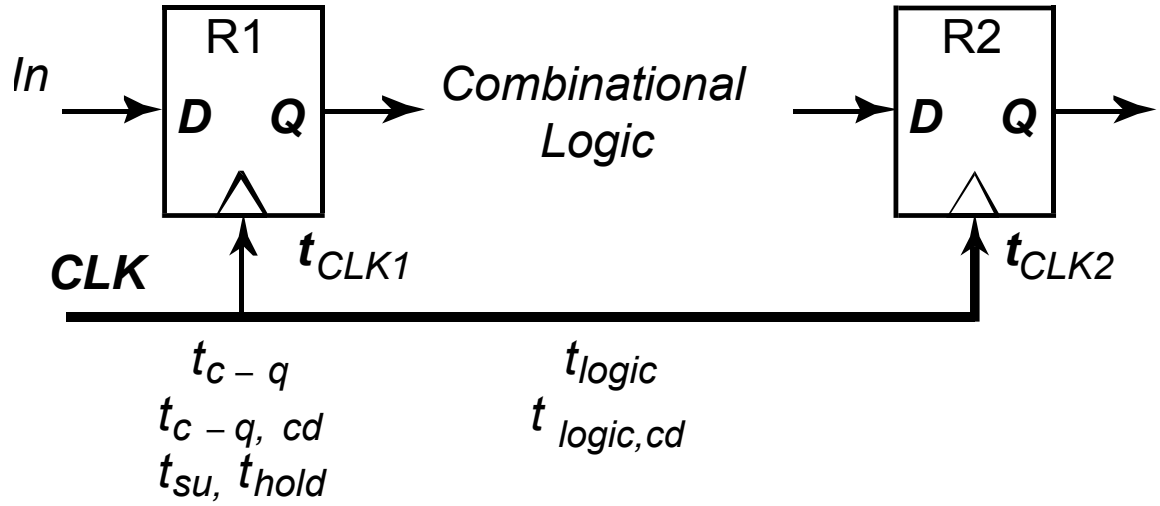
# Timing Constraints




*Minimum cycle time:*

$$T + \delta \geq t_{c\text{-}q} + t_{su} + t_{logic}$$



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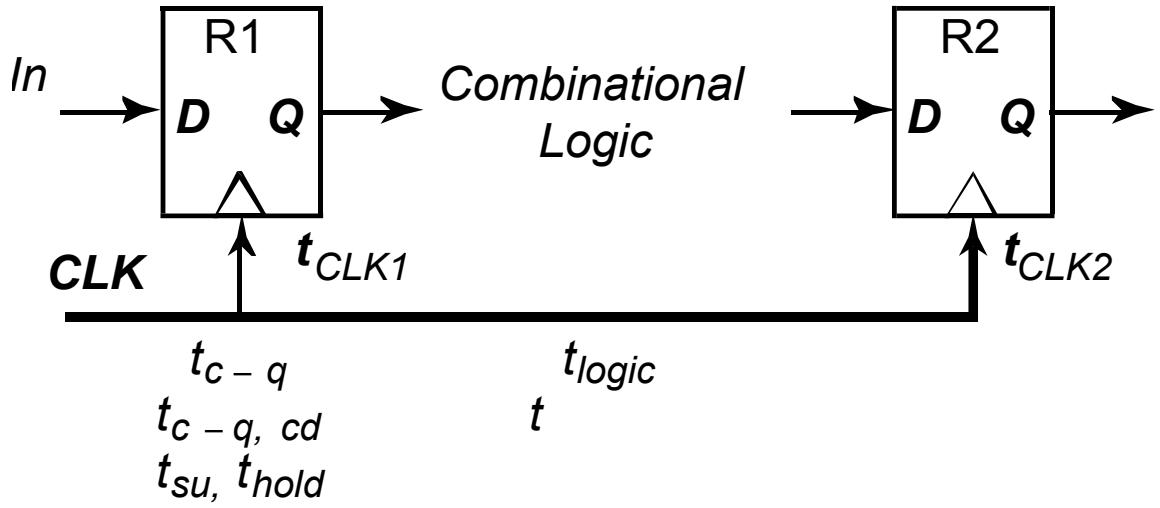
# Timing Constraints




*Hold time constraint:*

$$t_{(c\text{-}q,\ cd)} + t_{(logic,\ cd)} > t_{hold} + \delta$$

*Race between data and clock*



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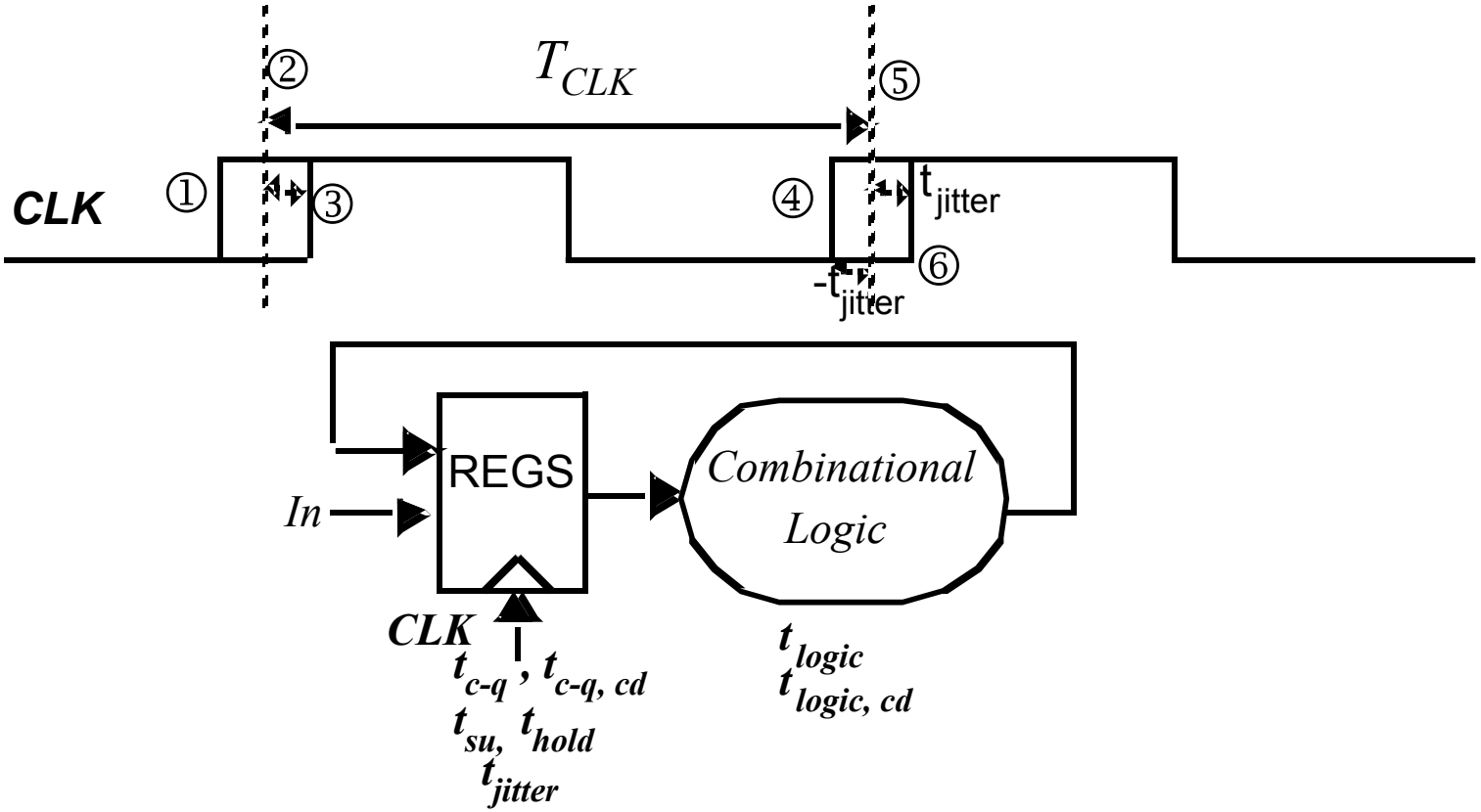
# Clock Jitter




$$T - 2t_{jitter} \geq t_{c\text{-}q} + t_{logic} + t_{su}$$



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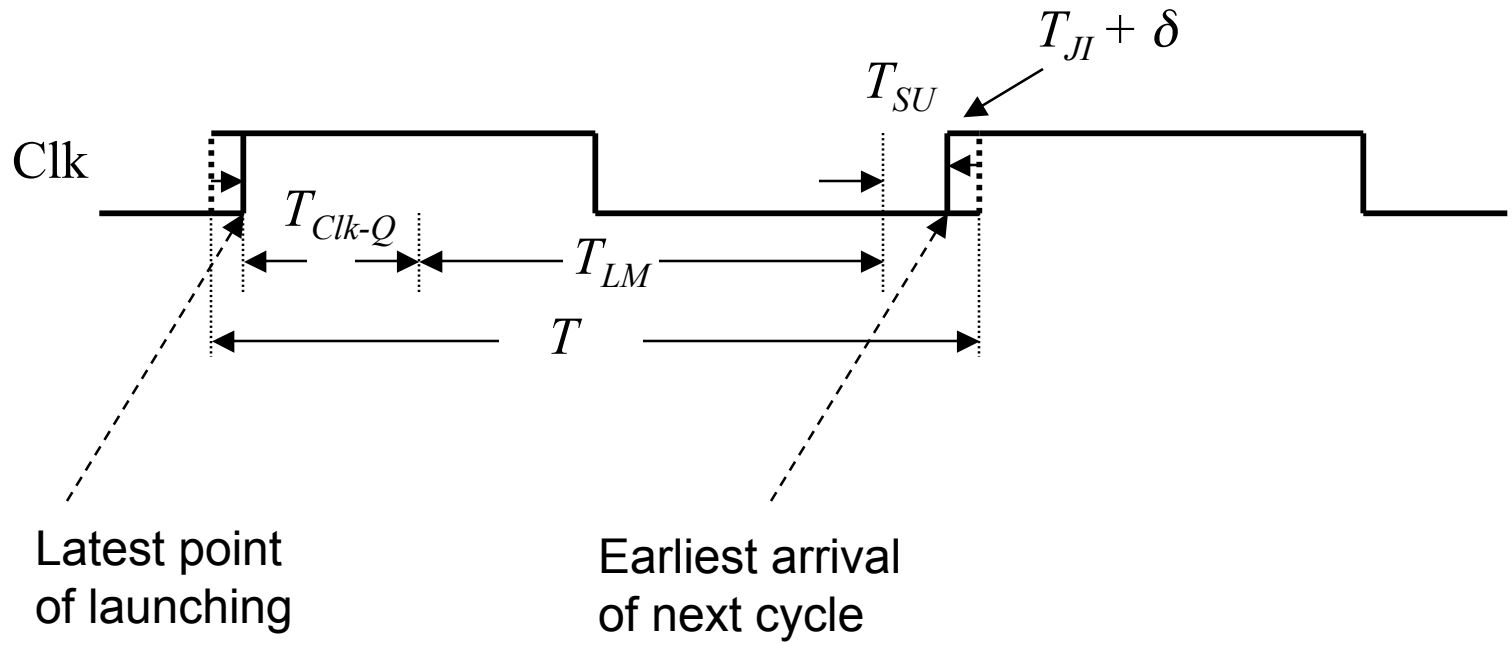
# Longest Logic Path in Edge-Triggered Systems







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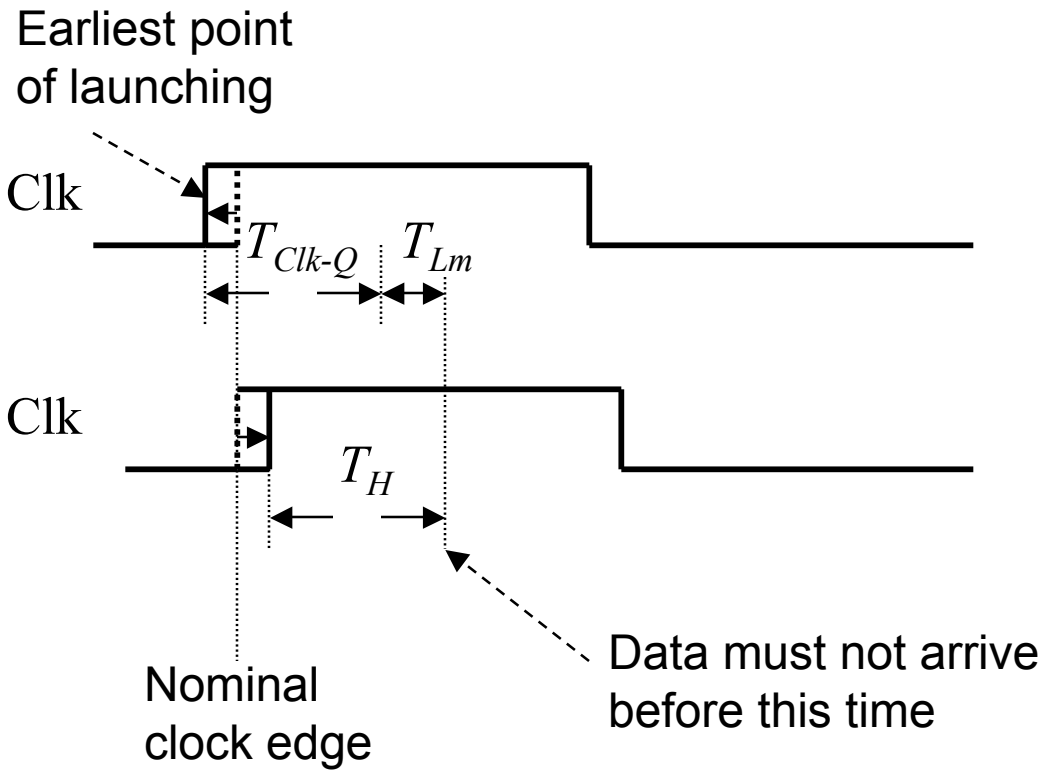
# Shortest Path







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# Clock Skew and Jitter

- Minimum clock cycle

$$T > t_{c\text{-}q} + t_{logic} + t_{su} - \delta + 2t_{jitter}$$

- Minimum logic delay

$$t_{logic} + t_{c\text{-}q} > t_{hold} + \delta + 2t_{jitter}$$




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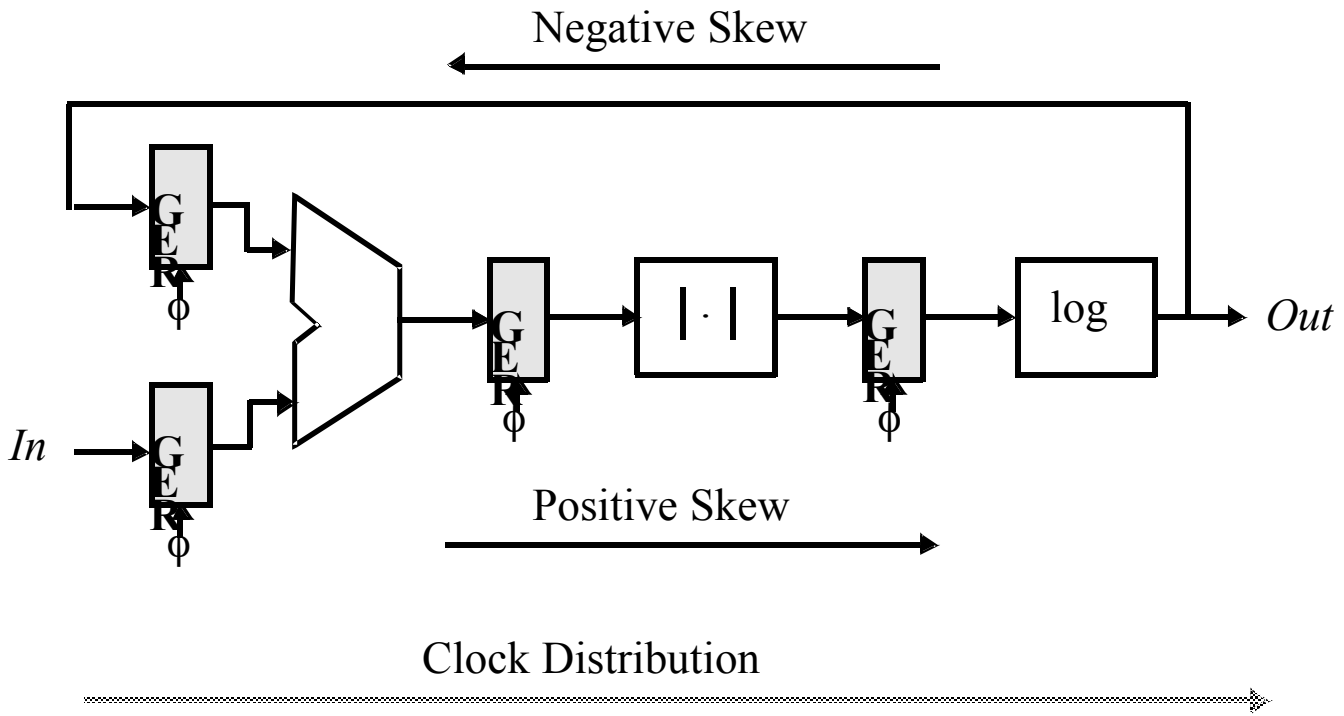
# Clock Skew in systems with feedback




**Data and Clock Routing**

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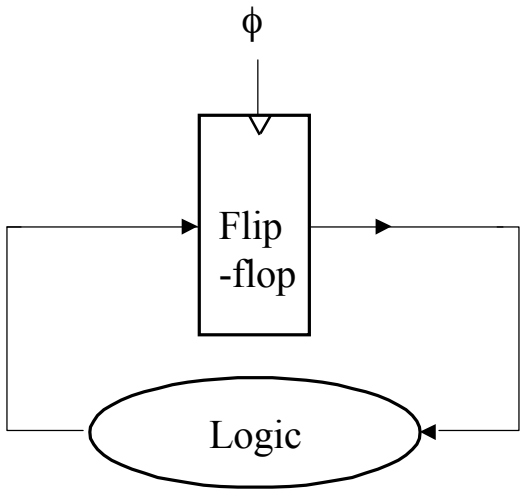
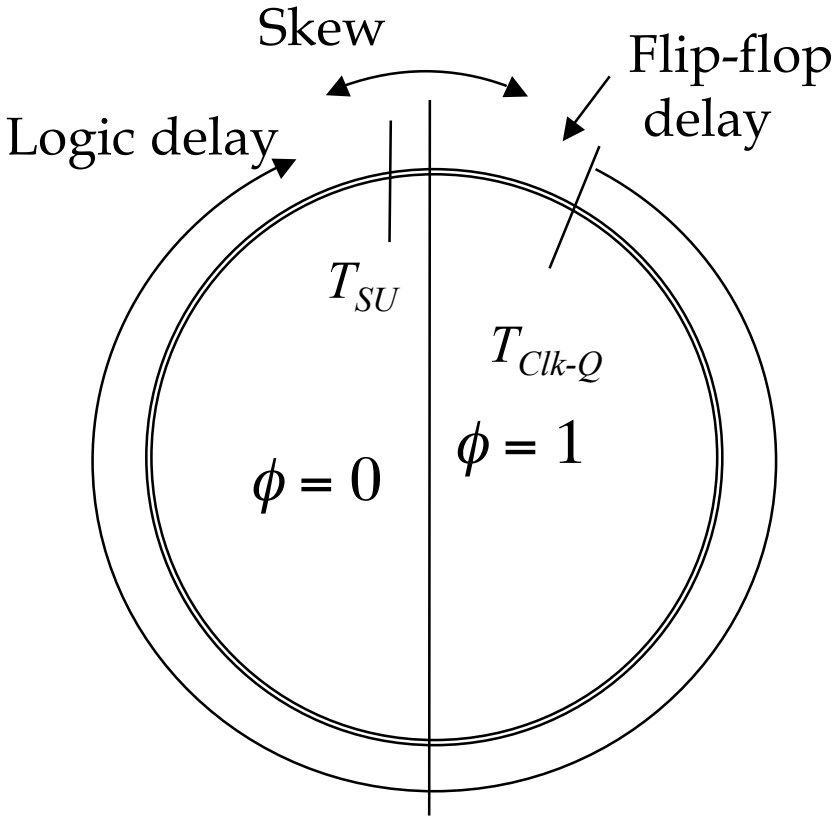
# Flip-Flop – Based Timing




*Representation after*
*M. Horowitz, VLSI Circuits 1996.*

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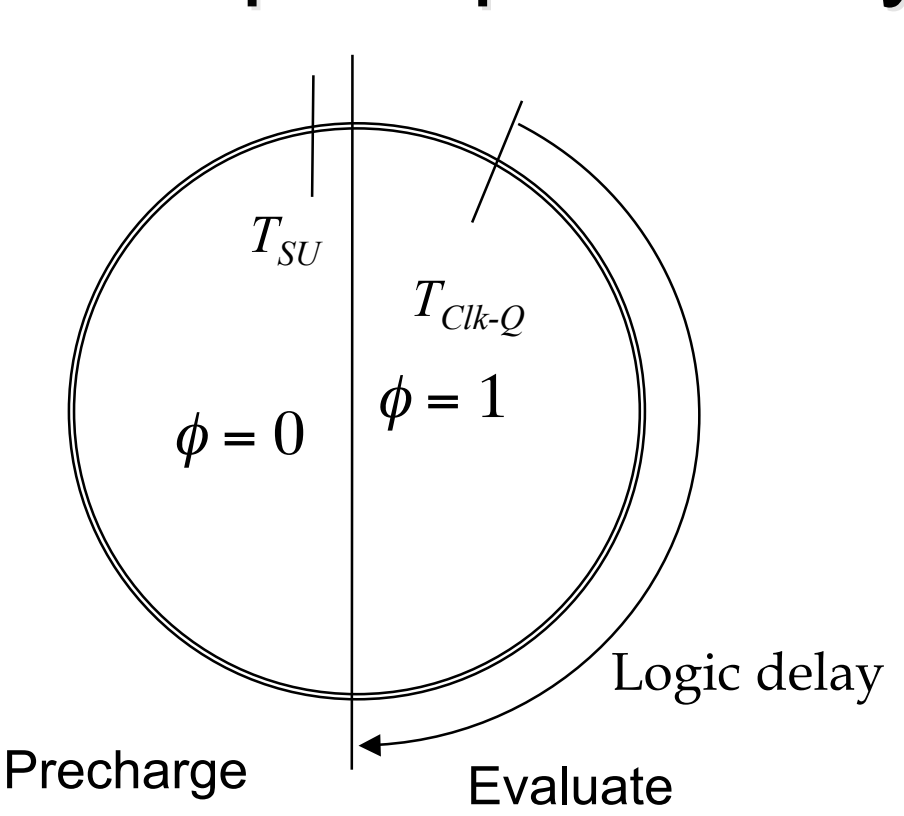
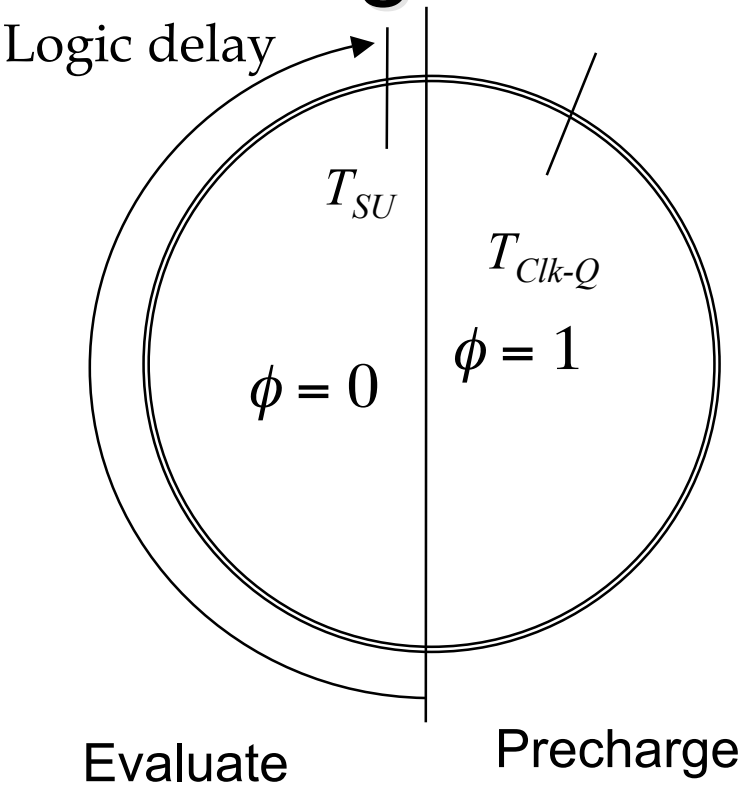
# Flip-Flops and Dynamic Logic




Flip-flops are used only with static logic

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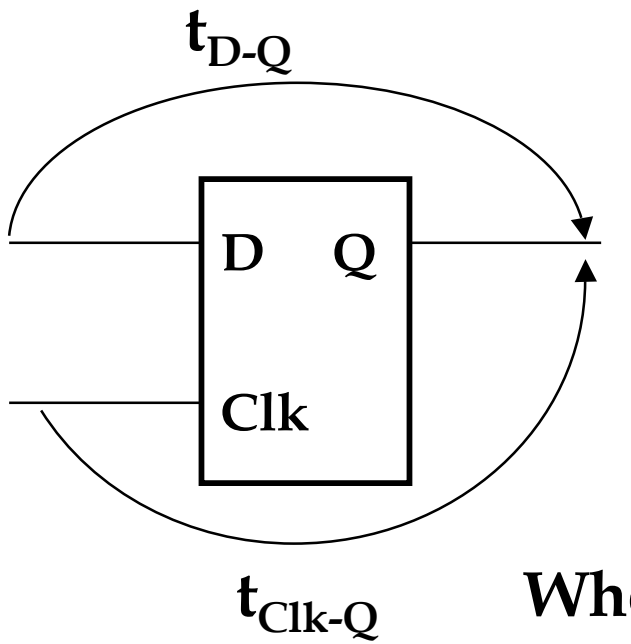
# Latch timing




**When data arrives to transparent latch**

**Latch is a 'soft' barrier**

**When data arrives to closed latch**

**Data has to be 're-launched'**

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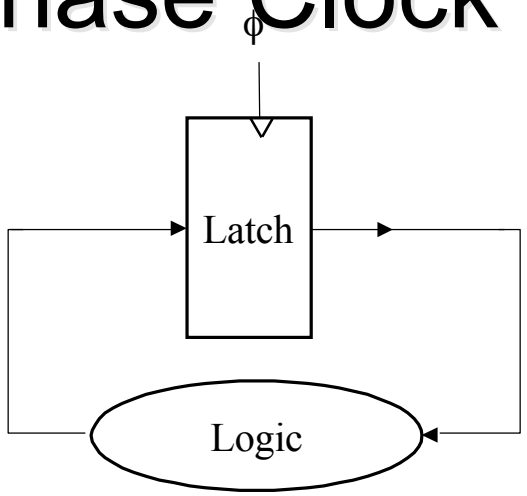
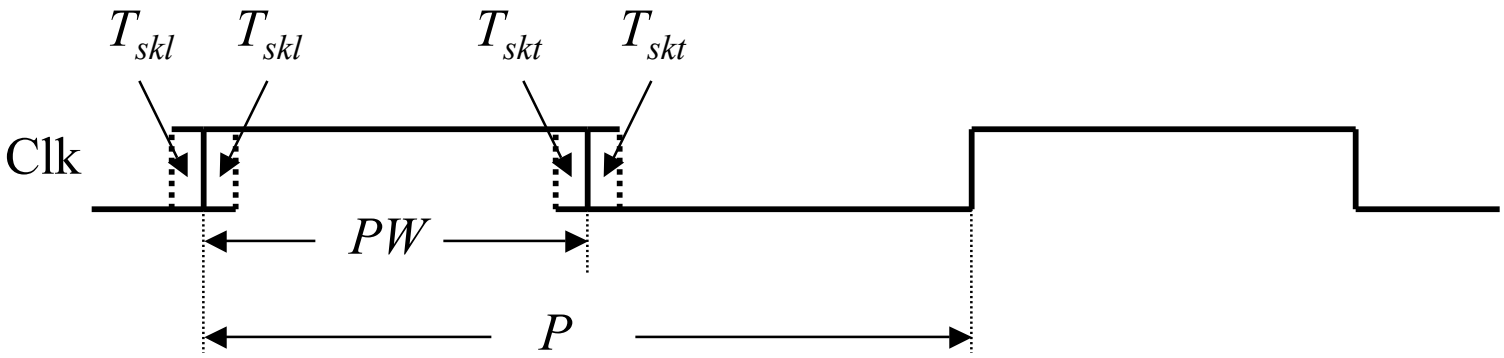
# Single-Phase Clock with Latches







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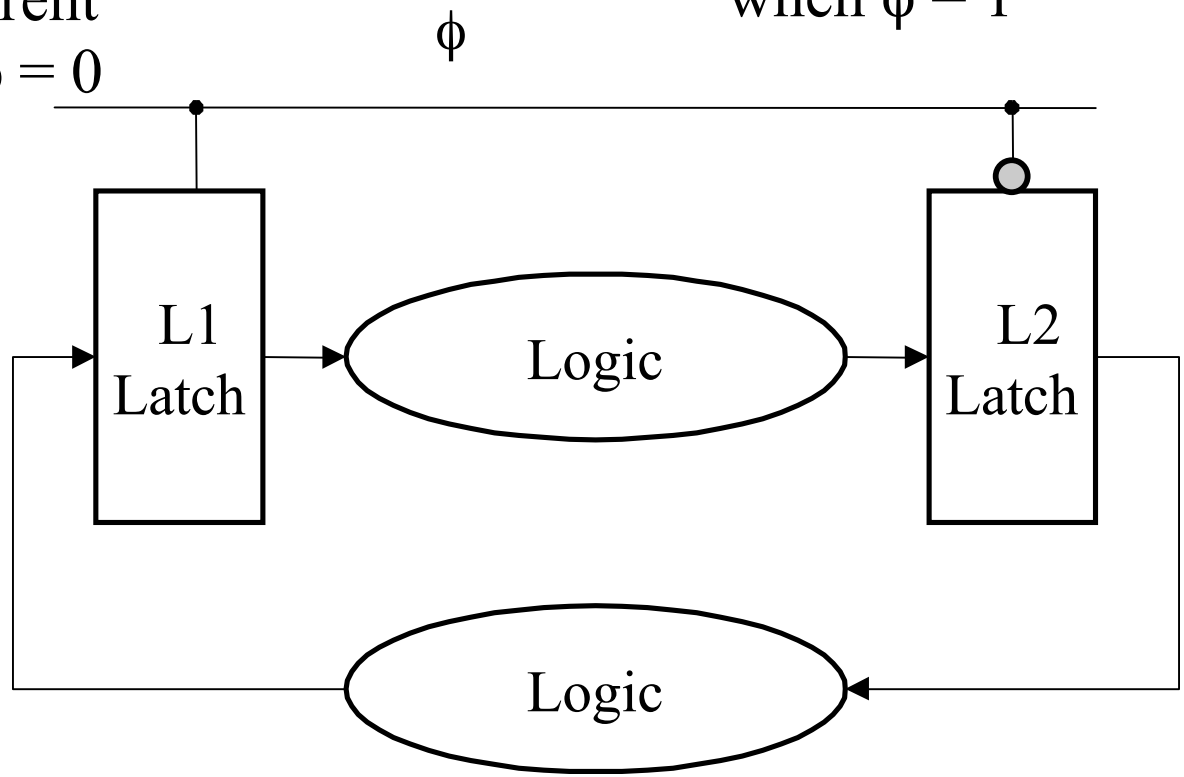
# Latch-Based Design

L1 latch is transparent when $\phi = 0$

L2 latch is transparent when $\phi = 1$







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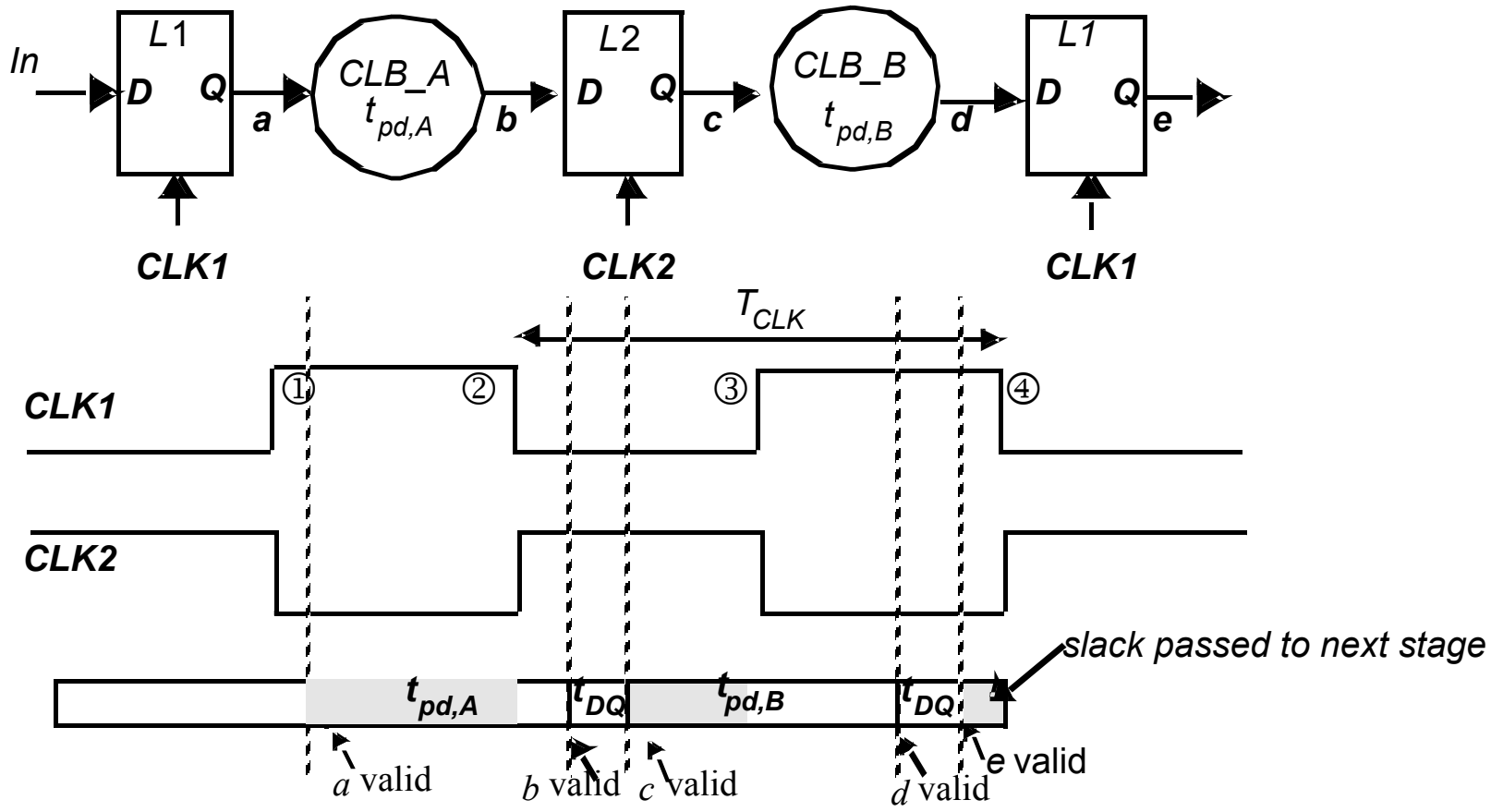
# Slack-borrowing









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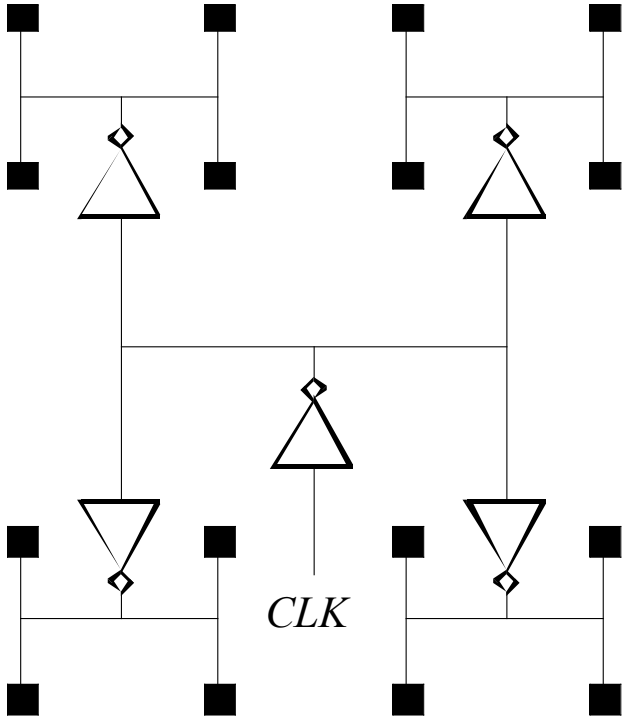
# Clock Distribution

- Distribute clock in a tree fashion
- H-Tree







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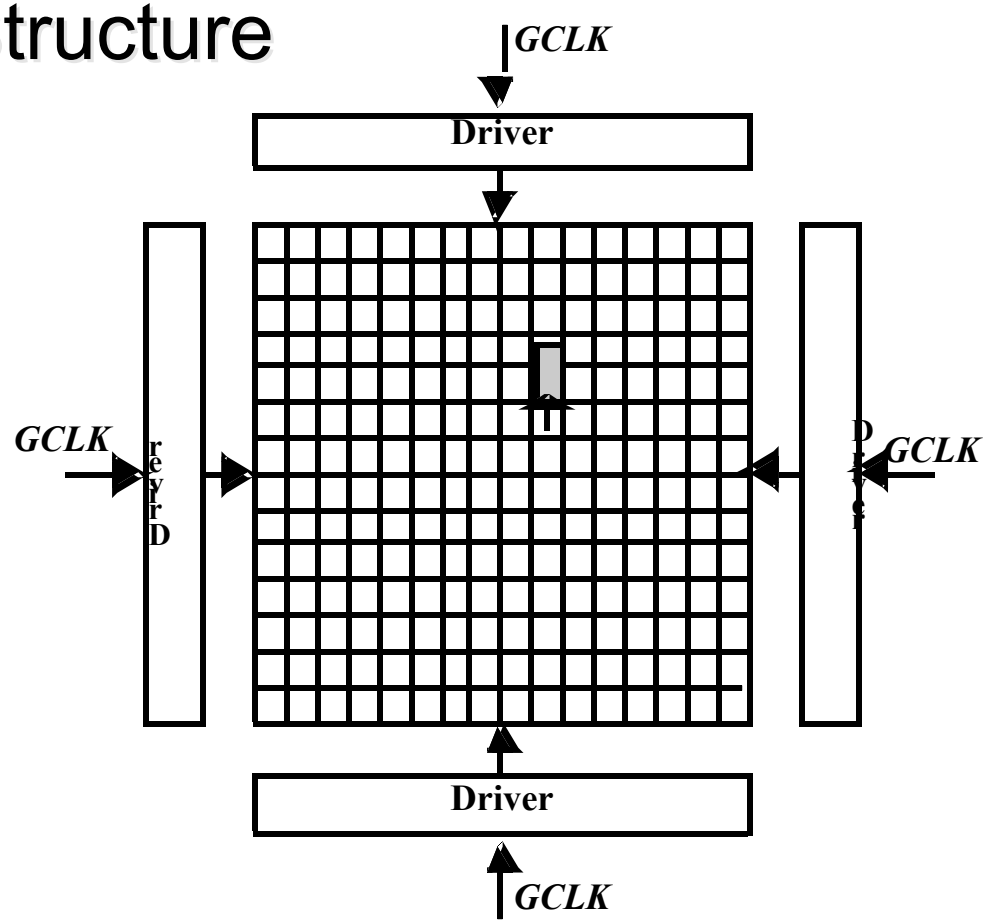
# Clock Distribution

- Grid Structure







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# Clock Distribution

- Alpha 21064
  - 200 MHz clock, 5 levels of buffering
  - Clock load - 3.25nF
  - Clock drivers account for 40% of the switched capacitance
  - 200 ps maximum skew
- Alpha 21164
  - 300 MHz clock
  - Clock load - 3.75 nF
  - Clock distribution - 20W power dissipation - 40% of total power of processor




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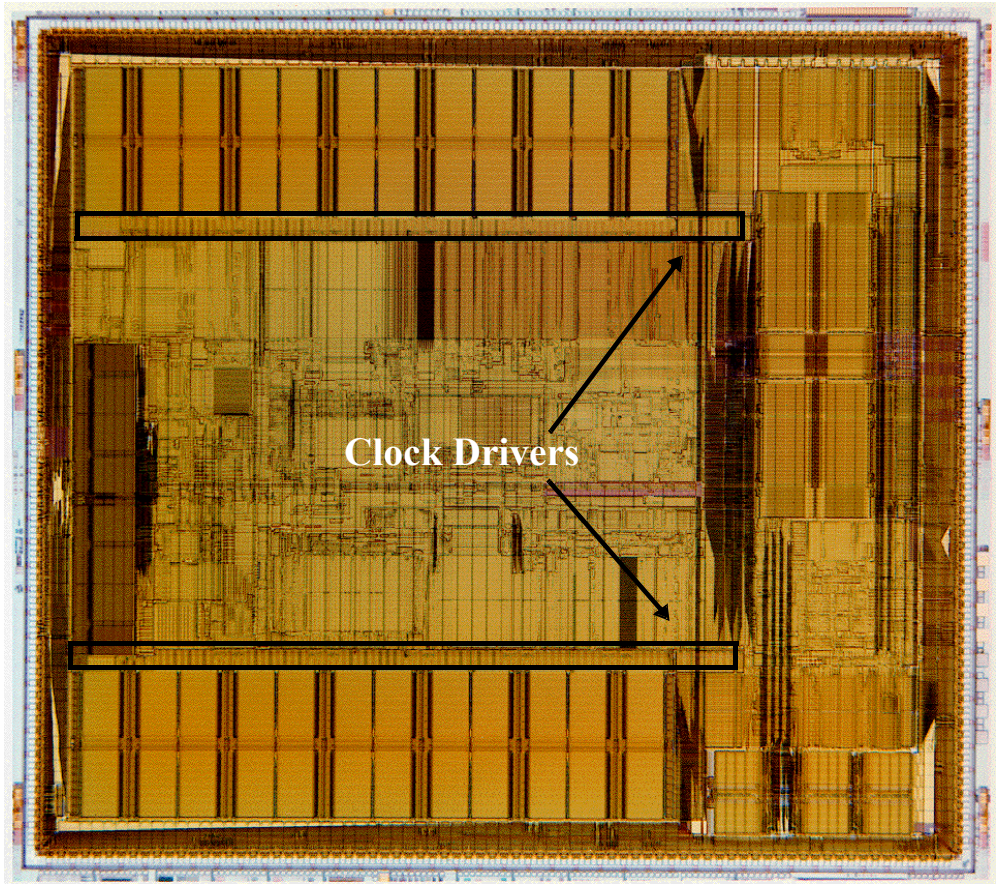
# Clock Distribution

- Alpha 21164







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# Clock Distribution

- Pentium III
  - Clock Jitter - 10% of cycle
  - Clock Skew - 7% of cycle
- Pentium IV
  - Clock Jitter - 5% of cycle
  - Clock Skew - 3% of cycle
  - Used regional clock buffers with adjustable delay




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# Dealing with Clock Skew and Jitter

- Balance clock paths (Tree distribution)
- Don’t use gated clocks
- Use negative skew to eliminate race conditions (at the cost of performance)
- Shield clock signals to avoid coupling
  - Route clock next to VDD and GND
- Use dummy fills to have uniform interlayer dielectric thickness




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# Next class

- I/O




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