

ECE 3421: Very Large Scale Integrated Circuit (VLSI) Design and Simulation

Credits and contact hours: 4 Credits (Two 60-minute lectures per week, and one 2-hour laboratory session per week)

Instructor: Lei Wang

Textbook: CMOS VLSI Design: A Circuits and Systems Perspective, N.H.E. Weste and D. Harris (2010)

Other supplemental materials: Class Notes – Topics not covered in the text (e.g., technology scaling)

Specific course information:

- a. *Catalog Description:* Design of MOS transistors, including short channel effects in sub-micron devices; scaling laws; design rules. Layout of NMOS and CMOS logic gates; power-delay calculations. Design of static and/or dynamic memories. Laboratory emphasizes schematic capture, simulation, timing analysis and testing; layout of custom IC's; use of VHDL.
- b. *Prerequisite:* ECE 3221
- c. *Required, elective, or selected elective:* Required (CMPE), Selected elective (EE)

Specific goals for the course:

- a. *Specific outcomes of instruction:* Students will be able to
 - Apply the concepts of short-channel effects, device scaling, and scaling laws in MOSFETS to design and analyze MOSFETs, and use them for CMOS, NMOS and dynamic logic gates and memory circuits.
 - Run simulation to obtain propagation delays and power/energy consumption in gates and access time in memories
 - Describe design methodologies for PLAs, and full custom as well as standard cell VLSI circuits
 - Conduct laboratory work for schematic capture, simulation, layout, and power/energy analysis of CMOS gates using Cadence design tools. (The project focuses on design, and power/performance tradeoff analysis of a subsystem consisting of logic gates and memory circuits.)
- b. *EAC Criterion 3 Student Outcomes addressed by the course:*
 - (1) **an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics**
Students learn to apply differential equations and probability theory to calculate propagation delays, access time etc. Students also learn fundamental algorithms used in computer-aided design (CAD) such as logic synthesis and testing of VLSI circuits.

- (2) **an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors**
Design of 0.25 micron and smaller dimension MOSFETs, their integration in logic gates and memory cells, and simulating their performance and power. This includes using a software package and theoretical analysis.
- (3) **an ability to communicate effectively with a range of audiences**
n/a
- (4) **an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts**
Individual work is promoted via the use of Cadence (commercial software) tool chain in laboratory and project work. It leads to the understanding of professional and ethical responsibility.
- (5) **an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives**
Project work involves a team of 3-5 students. The design project is tailored for the solution of an engineering problem.
- (6) **an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions**
Significant opportunity to synthesize circuits/subsystems using building blocks developed in the course.
- (7) **an ability to acquire and apply new knowledge as needed, using appropriate learning strategies**
The course teaches theory and design techniques for digital VLSI circuits that are evolving (as evidenced by the journal articles and chip clock rate etc.). This emphasizes the need to keep up with new technological developments that are required throughout one's professional career.

Topics covered:

- MOS device physics with emphasis on short channel effects, scaling laws, and fundamental limits.
- Design of MOSFETs and using them in logic gates and memory circuits.
- Calculation of propagation delays and energy/power for logic gates and wires.
- Design methodologies for PLAs, and VLSI circuits.
- Design of storage elements such as registers and random access memories.
- Schematic capture, simulation and layout of CMOS gates using Cadence software